Data Sheet | September 29, 2008 | FN6152.4

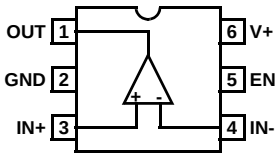
Ultra-Small, 800nA and 2.5µA Single Supply, Rail-to-Rail Input/Output (RRIO) Comparators

The ISL28196 and ISL28197 are micropower comparators optimized for low-power applications. The parts are designed for single-supply operation from 1.8V to 5.5V. The ISL28197 typically consumes 800nA of supply current and the ISL28196 typically consumes 2.5µA of supply current. Both parts feature rail-to-rail input and output swing (RRIO), allowing for maximum battery usage. The ISL28196 features a propagation delay of 150µs and the ISL28197 features a propagation delay of 0.6ms.

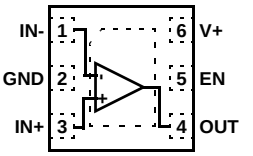
Equipped with an ENABLE pin (EN), both parts draw typically 2nA when off. The combination of small footprint, low power, single supply, and rail-to-rail operation makes them ideally suited for all battery operated devices.

Pinouts

ISL28196, ISL28197
(6 LD SOT-23)
TOP VIEW



ISL28196, ISL28197
(6 LD 1.6X1.6X0.5 µTDFN)
TOP VIEW



Features

- Typical Supply Current 800nA (ISL28197)
- Typical Supply Current 2.5µA (ISL28196)
- Ultra-Low Single-Supply Operation Down to +1.8V
- Rail-to-Rail Input/Output Voltage Range (RRIO)
- 150µs Typical Propagation Delay (ISL28196)
- 0.6ms Typical Propagation Delay (ISL28197)
- ENABLE Pin Feature
- Push-Pull Output
- -40°C to +125°C Operation
- Pb-Free (RoHS Compliant)

Applications

- 2-Cell Alkaline Battery-Powered/Portable Systems
- Window Comparators
- Threshold Detectors/Discriminators

Ordering Information

PART NUMBER	PART MARKING	PACKAGE Tape & Reel (Pb-Free)	PKG. DWG. #
ISL28196FHZ-T7* (Note 1)	GABM	6 Ld SOT-23	MDP0038
ISL28196FRUZ-T7* (Note 2)	M5	6 Ld 1.6x1.6x0.5 µTDFN	L6.1.6x1.6A
ISL28197FHZ-T7* (Note 1)	GABN	6 Ld SOT-23	MDP0038
ISL28197FRUZ-T7* (Note 2)	M6	6 Ld 1.6x1.6x0.5 µTDFN	L6.1.6x1.6A

*Please refer to TB347 for details on reel specifications.
NOTES:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020..

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage (V_+, V_-) 5.75V
Supply Turn On Voltage Slew Rate 1V/µs
Differential Input Current 5mA
Differential Input Voltage . . . . . V- - 0.5V to V+ + 0.5V
Input Voltage . . . . . V- - 0.5V to V+ + 0.5V
ESD Rating
Human Body Model 3kV
Machine Model 300V

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
6 Ld SOT-23 Package	230
6 Ld µTDFN Package	117.52

Output Short-Circuit Duration . . . . . .Indefinite
Ambient Operating Temperature Range . . . . . .-40°C to +125°C
Storage Temperature Range . . . . . .-65°C to +150°C
Operating Junction Temperature . . . . . .+125°C
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

3. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, Therefore $T_J = T_C = T_A$

Electrical Specifications

V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, T_A = +25°C, unless otherwise specified. **Boldface limits apply over -40°C to +125°C.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 4)	TYP	MAX (Note 4)	UNIT
V_{OS}	Input Offset Voltage		-2 **-2.5**	-0.1	2 **2.5**	mV
I_{OS}	Input Offset Current		-60 **-100**	10	60 **100**	pA
I_B	Input Bias Current		-80 **-150**	15	80 **150**	pA
CMIR	Common Mode Input Range	Established by CMRR test	0		5	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0.5V to 3.5V	70 **70**	100		dB
		V_{CM} = 0V to 5V	60			dB
PSRR	Power Supply Rejection Ratio	V_+ = 1.8V to 5.5V	70 **70**	100		dB
V_{OUT}	Maximum Output Voltage Swing R_L terminated to V+/2	Output low, R_L = 10kΩ		35	70	mV
		Output high, R_L = 10kΩ	4.930	4.950		V
$I_{S,ON}$	Supply Current, Enabled	ISL28196		2.5	4.0 **4.5**	µA
		ISL28197		0.8	1.6 **2.0**	µA
$I_{S,OFF}$	Supply Current, Disabled	EN = 0.4V		2	20 **50**	nA
V_{SUPPLY}	Supply Voltage Range		1.8		5.5	V
C_{IN}	Input Capacitance			5		pF
ENABLE INPUT						
V_{INH}	Enable Pin High Level		(V+)x(0.8)			V
V_{INL}	Enable Pin Low Level				0.4	V
I_{ENH}	Enable Pin Input Current	V_{EN} = 5V		30	150 **200**	nA
I_{ENL}	Enable Pin Input Current	V_{EN} = 0V		30	150 **200**	nA

Electrical Specifications $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, $T_A = +25°C$, unless otherwise specified. **Boldface limits apply over -40°C to +125°C. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 4)	TYP	MAX (Note 4)	UNIT
TIMING						
$t_{PD}\pm$	ISL28196 Propagation Delay Low to High and High to Low	C_L = 10pF, 20mV Overdrive		150	300	µs
$t_{PD}\pm$	ISL28197 Propagation Delay Low to High and High to Low	C_L = 10pF, 1.5V Overdrive		0.625	1.3	ms
t_R/t_F	ISL28196 Rise/Fall Time	C_L = 10pF		9	18	µs
	ISL28197 Rise/Fall Time	C_L = 10pF		35	70	µs

NOTE:

4. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, unless otherwise specified.

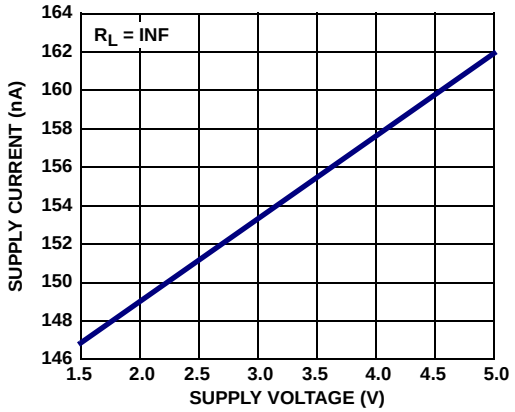


FIGURE 1. ISL28196 SUPPLY CURRENT vs SUPPLY VOLTAGE

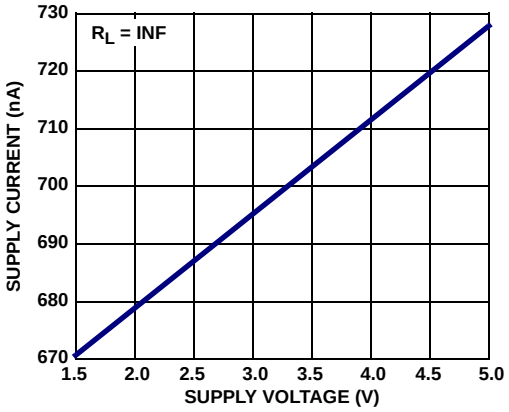


FIGURE 2. ISL28197 SUPPLY CURRENT vs SUPPLY VOLTAGE

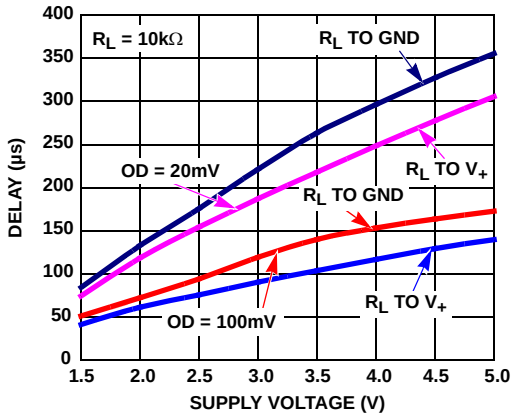


FIGURE 3. ISL28196 PROP DELAY vs SUPPLY VOLTAGE (RISING EDGE)

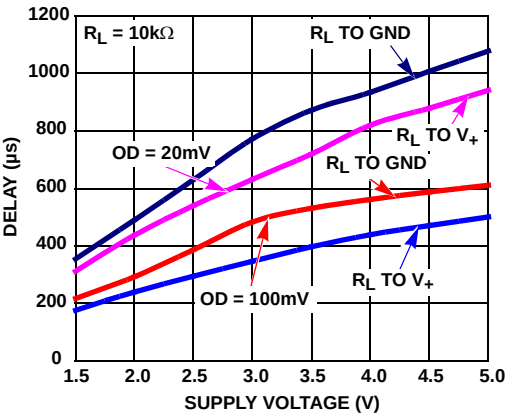


FIGURE 4. ISL28197 PROP DELAY vs SUPPLY VOLTAGE (RISING EDGE)

Typical Performance Curves $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, unless otherwise specified. **(Continued)**

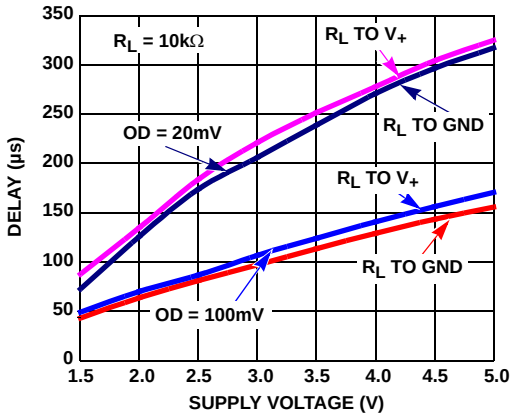


FIGURE 5. ISL28196 PROP DELAY vs SUPPLY VOLTAGE (FALLING EDGE)

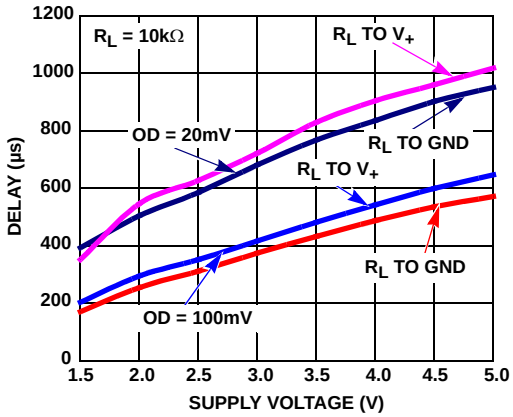


FIGURE 6. ISL28197 PROP DELAY vs SUPPLY VOLTAGE (FALLING EDGE)

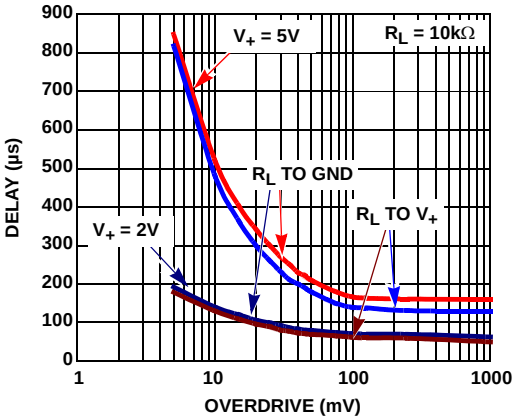


FIGURE 7. ISL28196 PROP DELAY vs OVERDRIVE (RISING EDGE)

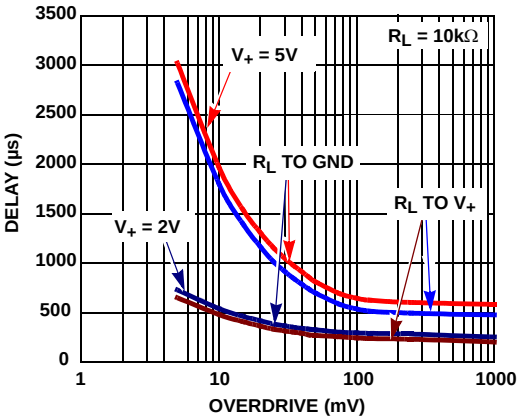


FIGURE 8. ISL28197 PROP DELAY vs OVERDRIVE (RISING EDGE)

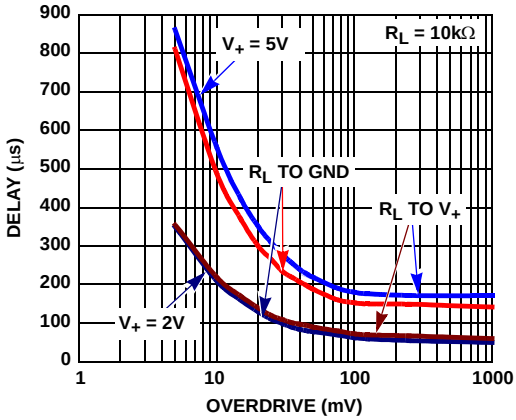


FIGURE 9. ISL28196 PROP DELAY vs OVERDRIVE (FALLING EDGE)

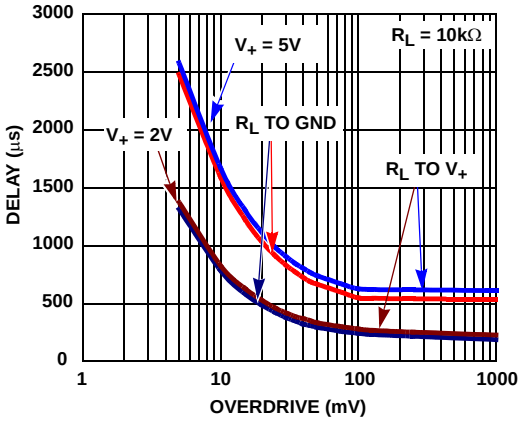


FIGURE 10. ISL28197 PROP DELAY vs OVERDRIVE (FALLING EDGE)

Typical Performance Curves $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, unless otherwise specified. **(Continued)**

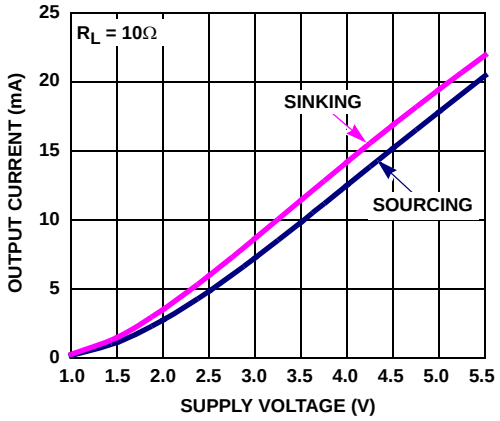


FIGURE 11. ISL28196 SHORT CIRCUIT CURRENT vs SUPPLY VOLTAGE

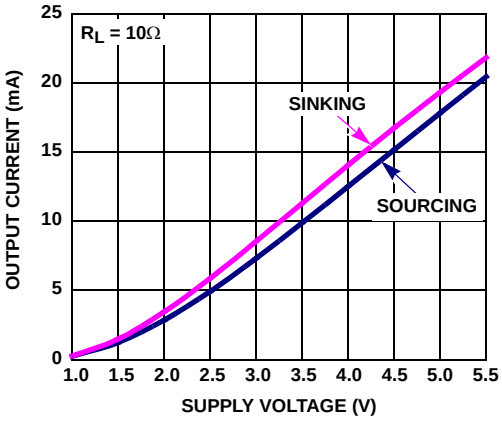


FIGURE 12. ISL28197 SHORT CIRCUIT CURRENT vs SUPPLY VOLTAGE

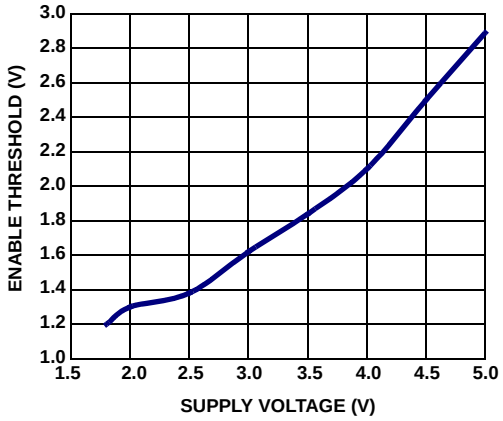


FIGURE 13. ISL28196 ENABLE THRESHOLD VOLTAGE vs SUPPLY VOLTAGE

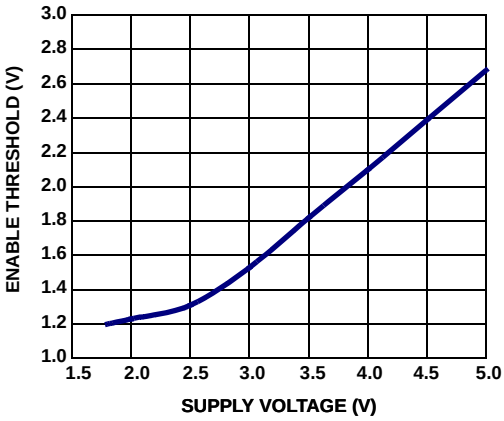


FIGURE 14. ISL28197 ENABLE THRESHOLD VOLTAGE vs SUPPLY VOLTAGE

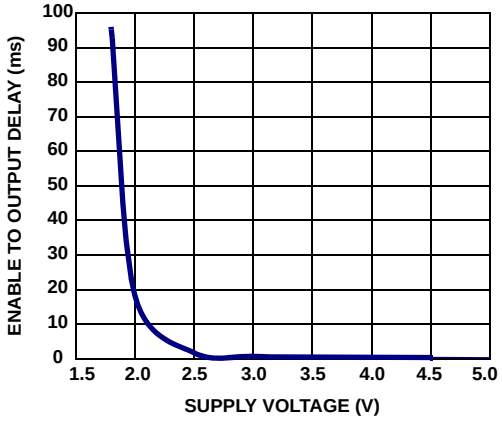


FIGURE 15. ISL28196 ENABLE TO OUTPUT DELAY TIME vs SUPPLY VOLTAGE

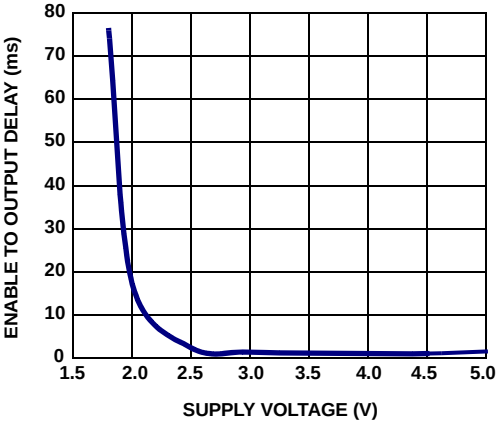


FIGURE 16. ISL28197 ENABLE TO OUTPUT DELAY TIME vs SUPPLY VOLTAGE

Typical Performance Curves $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, unless otherwise specified. **(Continued)**

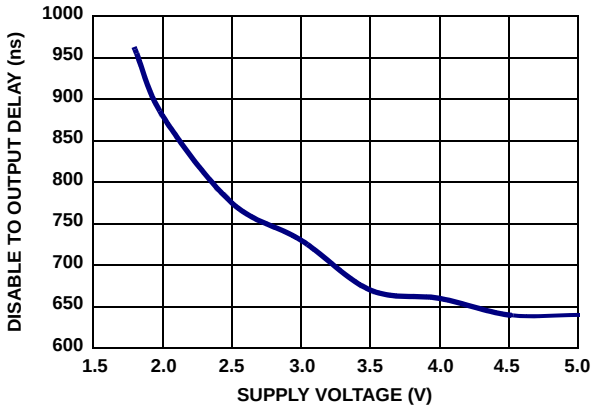


FIGURE 17. ISL28196 ENABLE LOW TO OUTPUT TURN-OFF TIME vs SUPPLY VOLTAGE

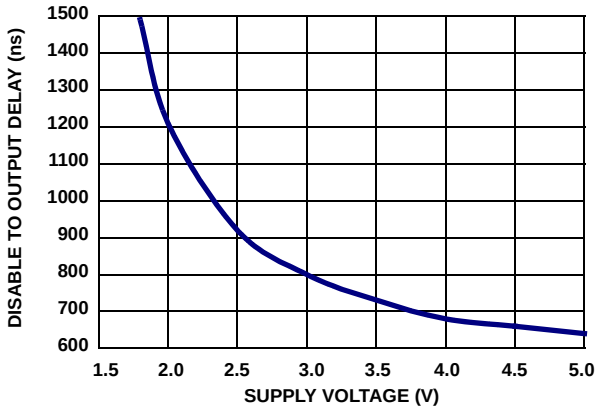


FIGURE 18. ISL28197 ENABLE LOW TO OUTPUT TURN-OFF TIME vs SUPPLY VOLTAGE

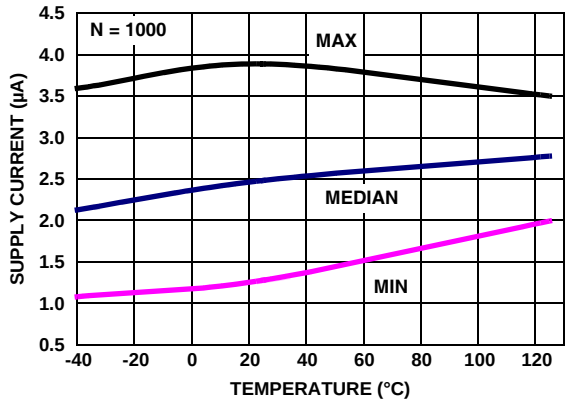


FIGURE 19. ISL28196 SUPPLY CURRENT vs TEMPERATURE, V_+, V_- = ±2.5V

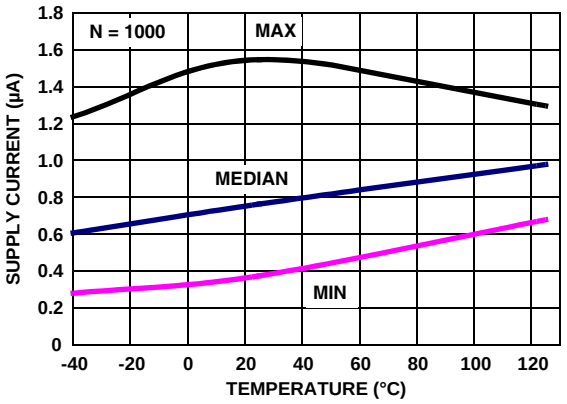


FIGURE 20. ISL28197 SUPPLY CURRENT vs TEMPERATURE, V_+, V_- = ±2.5V

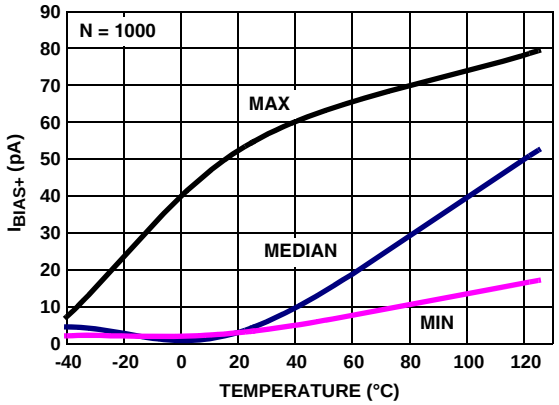


FIGURE 21. ISL28196 I_{BIAS+} vs TEMPERATURE, V_+, V_- = ±2.5V

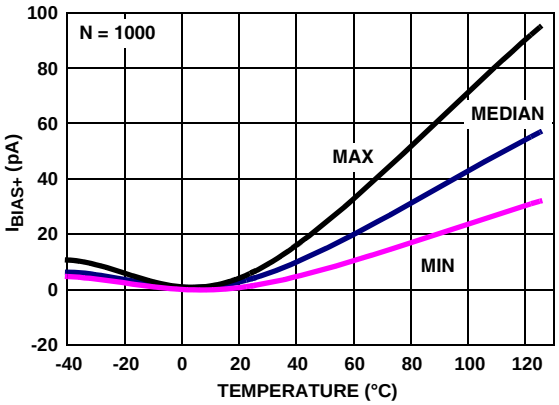


FIGURE 22. ISL28197 I_{BIAS+} vs TEMPERATURE, V_+, V_- = ±2.5V

Typical Performance Curves $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, unless otherwise specified. **(Continued)**

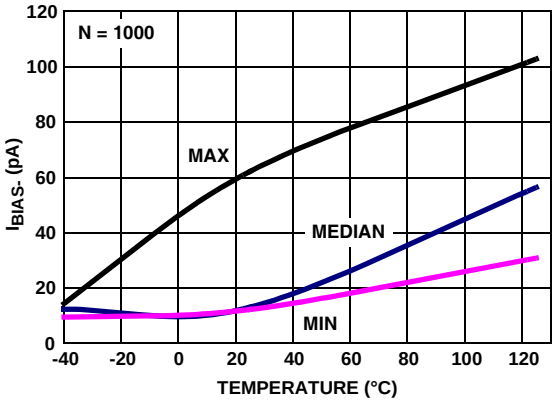


FIGURE 23. ISL28196 I_{BIAS-} vs TEMPERATURE, V_+, V_- = ±2.5V

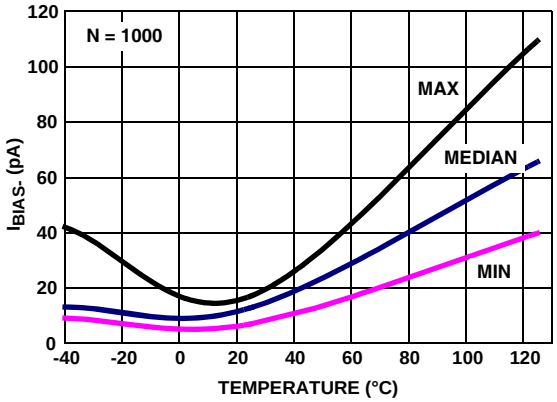


FIGURE 24. ISL28197 I_{BIAS-} vs TEMPERATURE, V_+, V_- = ±2.5V

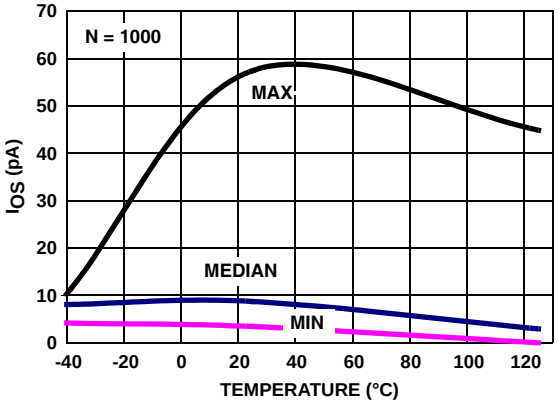


FIGURE 25. ISL28196 I_{OS} vs TEMPERATURE, V_+, V_- = ±2.5V

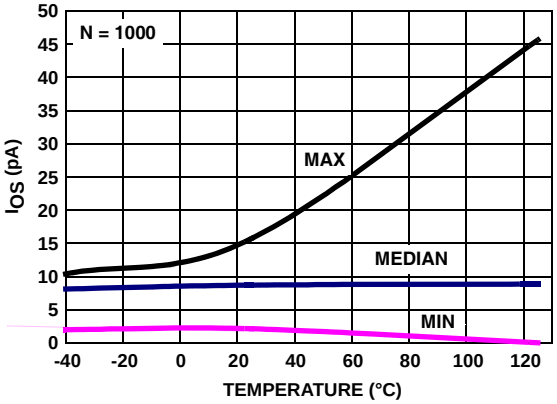


FIGURE 26. ISL28197 I_{OS} vs TEMPERATURE, V_+, V_- = ±2.5V

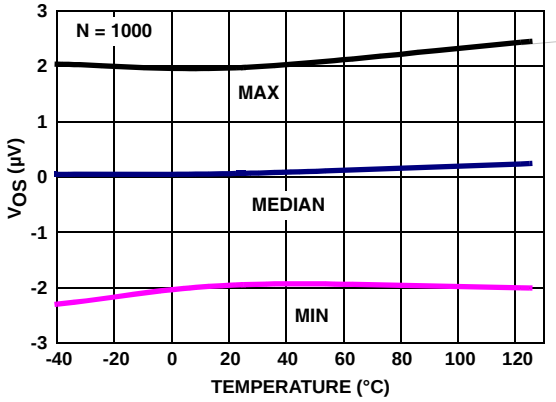


FIGURE 27. ISL28196 V_{OS} vs TEMPERATURE, V_+, V_- = ±2.5V V_{IN} = 2.5V

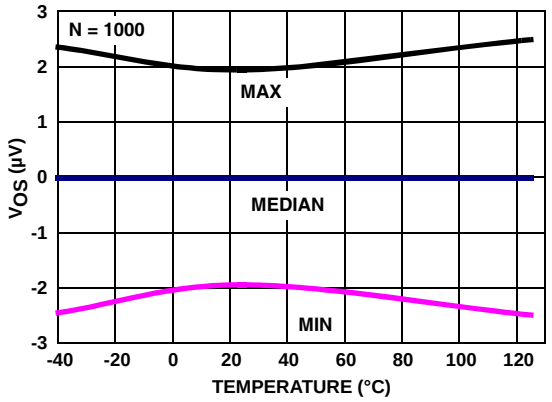


FIGURE 28. ISL28197 V_{OS} vs TEMPERATURE, V_+, V_- = ±2.5V V_{IN} = 2.5V

Typical Performance Curves $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, unless otherwise specified. **(Continued)**

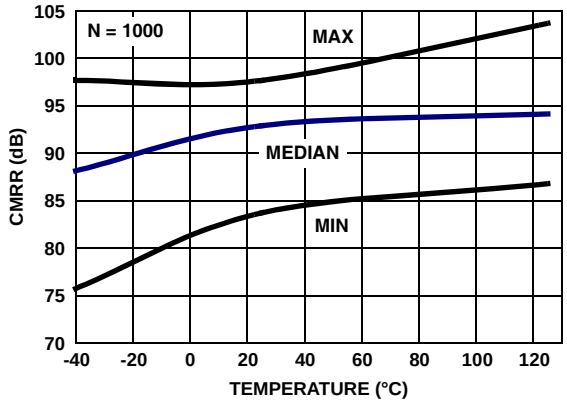


FIGURE 29. ISL28196 CMRR vs TEMPERATURE, VCM = 0.5V TO 3.5, V_+, V_- = ±2.5V

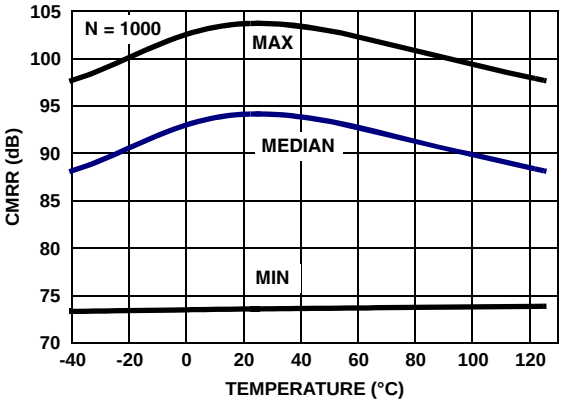


FIGURE 30. ISL28197 CMRR vs TEMPERATURE, VCM = 0.5V TO 3.5, V_+, V_- = ±2.5V

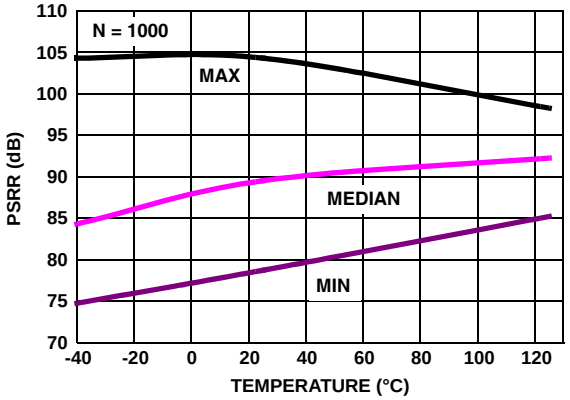


FIGURE 31. ISL28196 PSRR vs TEMPERATURE, V_+, V_- = ±0.9V TO ±2.5V

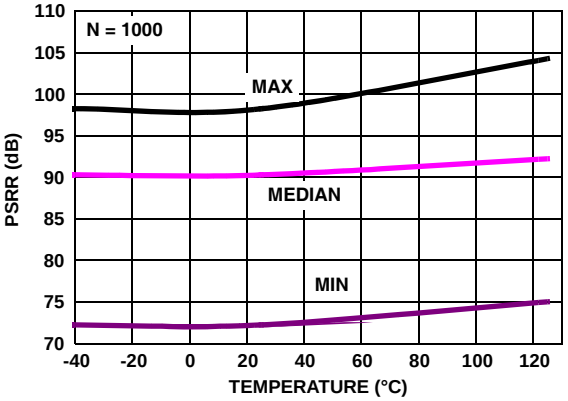


FIGURE 32. ISL28197 PSRR vs TEMPERATURE, V_+, V_- = ±0.9V TO ±2.5V

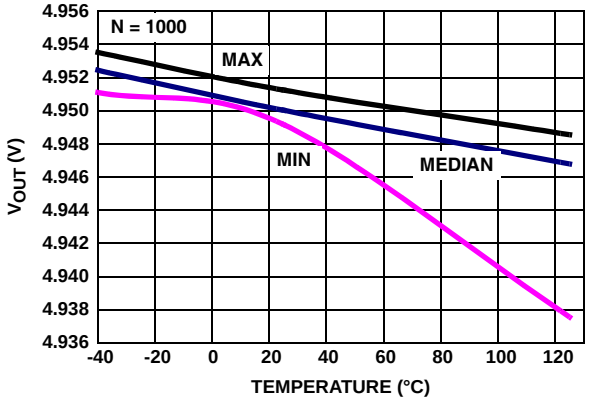


FIGURE 33. ISL28196 V_{OUT} HIGH vs TEMPERATURE, V_+, V_- = ±2.5V, R_L = 10k

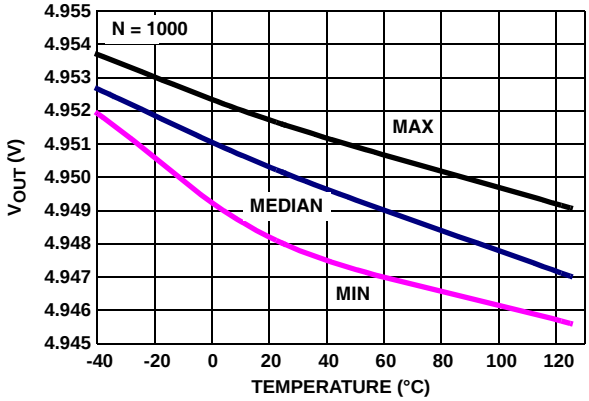


FIGURE 34. ISL28197 V_{OUT} HIGH vs TEMPERATURE, V_+, V_- = ±2.5V, R_L = 10k

Typical Performance Curves $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, unless otherwise specified. **(Continued)**

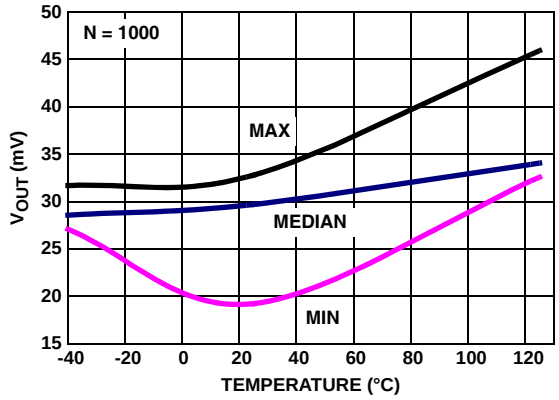


FIGURE 35. ISL28196 V_{OUT} LOW vs TEMPERATURE, V_+, V_- = ±2.5V, R_L = 10k

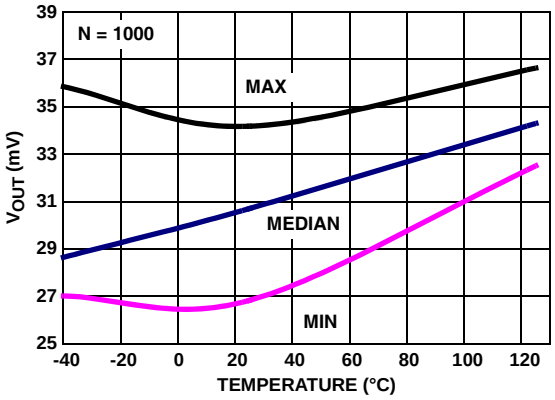


FIGURE 36. ISL28197 V_{OUT} LOW vs TEMPERATURE, V_+, V_- = ±2.5V, R_L = 10k

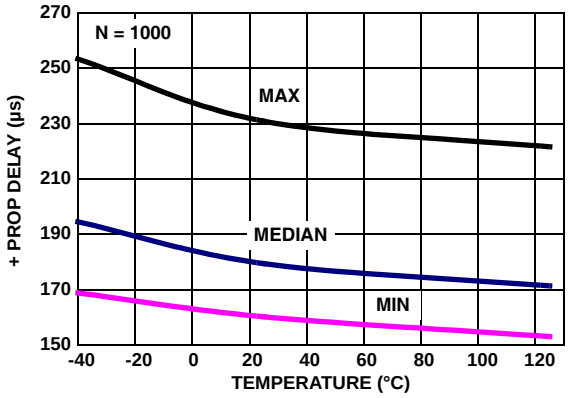


FIGURE 37. ISL28196 POSITIVE PROP DELAY vs TEMPERATURE 50% TO 20%, V_+ = 5V

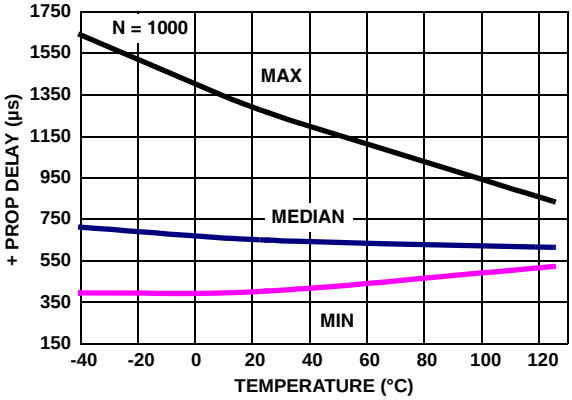


FIGURE 38. ISL28197 POSITIVE PROP DELAY vs TEMPERATURE 50% TO 20%, V_+ = 5V

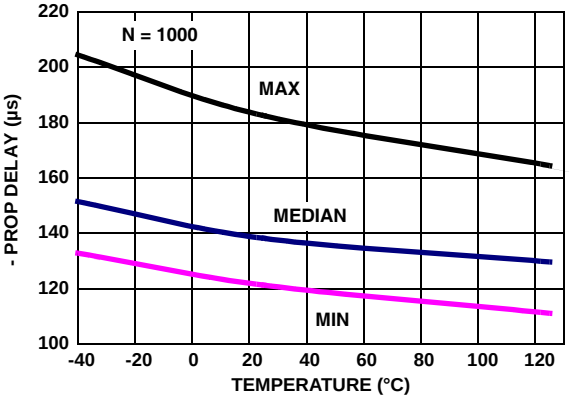


FIGURE 39. ISL28196 NEGATIVE PROP DELAY vs TEMPERATURE 50% TO 20%, V_+ = 5V

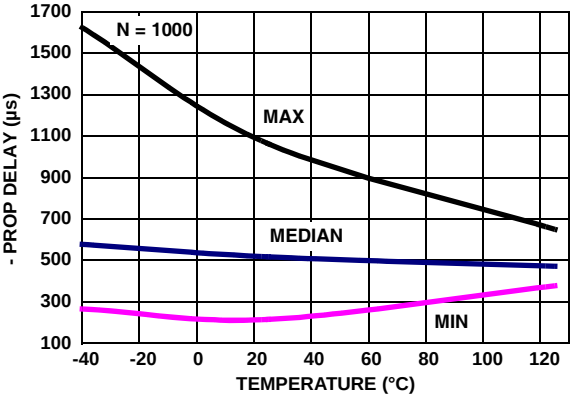


FIGURE 40. ISL28197 NEGATIVE PROP DELAY vs TEMPERATURE 50% TO 20%, V_+ = 5V

Typical Performance Curves V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, unless otherwise specified. **(Continued)**

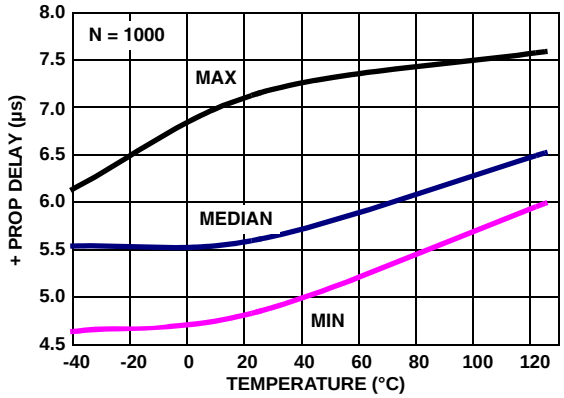


FIGURE 41. ISL28196 FALL TIME vs TEMPERATURE 20% TO 80%, V_+ = 5V

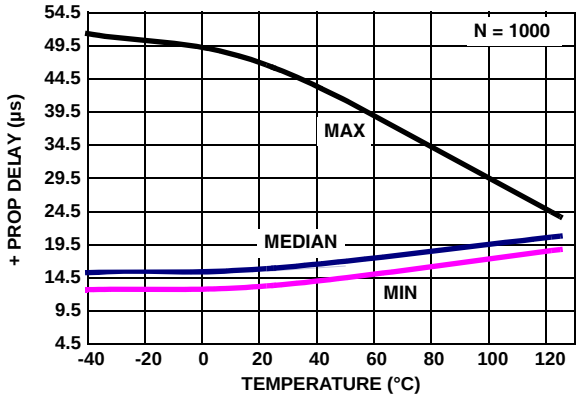
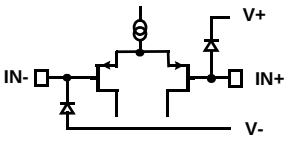


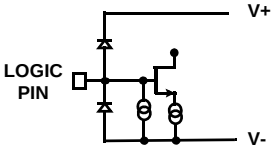
FIGURE 42. ISL28197 FALL TIME vs TEMPERATURE 20% TO 80%, V_+ = 5V

Pin Descriptions

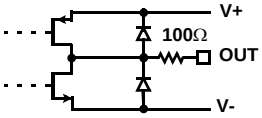
ISL28196, ISL28197 (6 LD SOT-23)	ISL28196, ISL28197 (6 LD µTDFN)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
1	4	OUT	Circuit 3	Comparator output
2	2	GND	Circuit 4	GROUND terminal
3	3	IN+	Circuit 1	Comparator non-inverting input
4	1	IN-	Circuit 1	Comparator inverting input
5	5	EN	Circuit 2	Comparator enable pin; Logic “1” selects the enabled state: Logic “0” selects the disabled state
6	6	V+	Circuit 4	Positive power supply



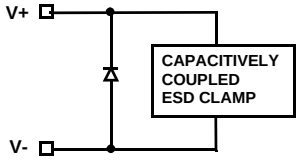
CIRCUIT 1



CIRCUIT 2



CIRCUIT 3



CIRCUIT 4

Applications Information

Introduction

The ISL28196 and ISL28197 are CMOS rail-to-rail input and output (RRIO) micropower comparators. These devices are designed to operate from single supply (1.8V to 5.5V) and have an input common mode range that extends to the positive rail and to the negative supply rail for true rail-to-rail performance. The CMOS output can swing within tens of millivolts to the rails. Featuring worst case maximum supply currents of only 4.5µA and 2µA for the ISL28196 and ISL28197 respectively, these comparators are ideally suited for solar and battery powered applications.

Input Protection

All input terminals have internal ESD protection diodes to both positive and negative supply rails, limiting the input voltage to within one diode beyond the supply rails. Both the ISL28196 and ISL28197 have a maximum input differential voltage that extends beyond the rails ($_+$V + 0.5V to $_-$V - 0.5V).

Rail-to-Rail Output

A pair of complementary MOSFET devices are used to achieve the rail-to-rail output swing. The NMOS sinks current to swing the output in the negative direction. The PMOS sources current to swing the output in the positive direction. The ISL28196 and ISL28197 with a 100kΩ load will swing to within 6mV of the positive supply rail and within 3mV of ground.

Break-Before-Make Operation of the Output

The output circuit has a break-before-make response. This means that the P-Channel turns off before the N-Channel turns on during a high to low transition of the output (reference Figure 43). Likewise, the N-Channel turns off before the P-Channel turns on during a low to high transition. This results in different propagation delay times depending upon where the output load resistor is tied to. If the load resistor is tied to ground, (Figure 44A) then the propagation delay is controlled by the P-Channel. For a high to low transition the propagation delay does not include the additional break-before-make time because the load resistor will pull the output low once the P-Channel has turned off.

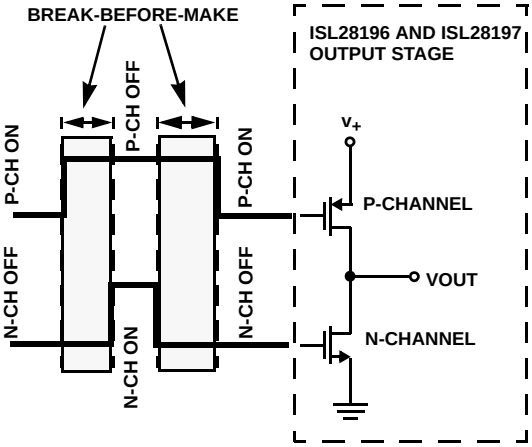


FIGURE 43. MAKE-BEFORE-BREAK ACTION OF THE OUTPUT STAGE

During the low to high transition, however, if the load resistor is tied to ground, then the additional break-before-make time is added to the propagation delay time because the output won't pull high until the P-Channel turns on.

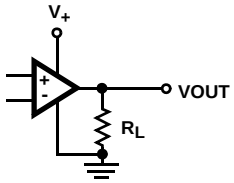


FIGURE 44A. R_L TO GND

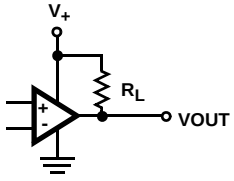


FIGURE 44B. R_L TO V+

FIGURE 44. CONNECTION OF R_L TO GND AND V+

If the load resistor is tied to V+ (Figure 44B) then the propagation delay is controlled by the N-Channel. For this condition, the additional delay time is added to the high to low transition because the output won't pull low until the N-Channel turns on. Figures 3 through 10 show the differences in propagation delay depending upon where the load is tied.

Propagation Delay

The input to output propagation delay has a dependency on power supply voltage, overdrive and whether the output is sourcing or sinking current. Figures 3 and 5 show a decreasing time propagation delay vs supply voltage for the ISL28196 and Figure 4 shows a similar behavior for the ISL28197. The output break-before-make mechanism results in a difference in propagation delay, depending on whether the output stage NMOS and PMOS are sourcing or sinking current. This delay difference is shown in the figures as a function of where the load is terminated (+V or -V) and also as a function of supply voltage. The dependence of propagation delay as a function of power supply voltage and input overdrive (from 5mV to 1V) is shown in Figures 7 and 9 for the ISL28196, and Figures 8 and 10 for the ISL28197.

Enable Feature

Both parts offer an EN pin, which enables the device when pulled high. The enable threshold is referenced to the -V terminal and has a level proportional to the total supply voltage (reference Figures 13 and 14 for EN Threshold vs Supply Voltage). The enable circuit has a delay time that changes as a function of supply voltage. Figures 23 through 26 show the effect of supply voltage on the enable and disable times. For supply voltages less than 3V, it is recommended that the user account for the increase enable/disable delay time.

In the disabled state (output in a high impedance state), the supply current is reduced to a typical of only 2nA. By disabling the devices, multiple parts can be connected together as a MUX. In this configuration, the outputs are tied together in parallel and a channel can be selected by the EN pin. The EN pin should never be left floating. The EN pin should be connnected directly to the V+ supply when not in use.

Proper Layout Maximizes Performance

To achieve the maximum performance of the high input impedance, care should be taken in the circuit board layout. The PC board surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board will reduce surface moisture and provide a humidity barrier, reducing parasitic resistance on the board. When input leakage current is a concern, the use of guard rings around the comparator inputs will further reduce leakage currents.

Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power-supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related in Equation 1:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} x PD_{MAXTOTAL}) \quad \text{(EQ. 1)}$$

where:

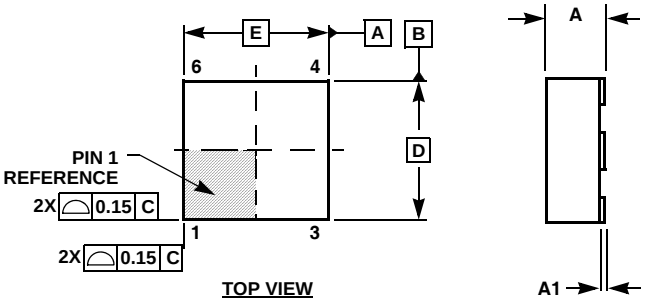
- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- PD_{MAX} for each amplifier can be calculated as shown in Equation 2:

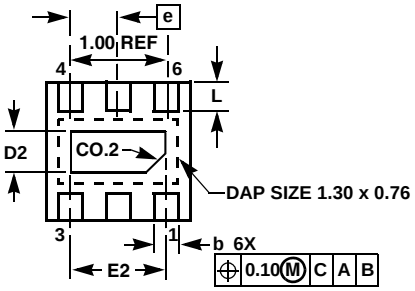
$$PD_{MAX} = 2*V_S \times I_{SMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 2)}$$

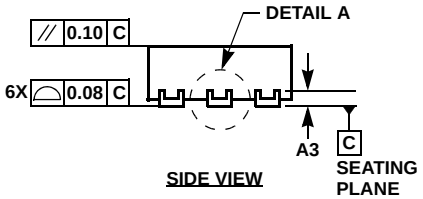
where:

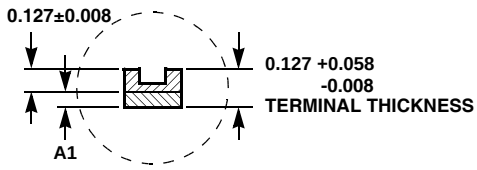
- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_S = Supply voltage (Magnitude of V_+ and V_-)
- I_{MAX} = Maximum supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application
- R_L = Load resistance

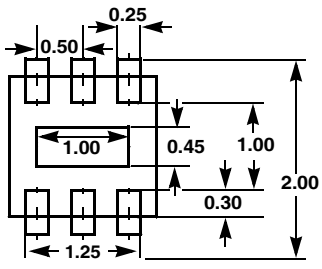
Ultra Thin Dual Flat No-Lead Plastic Package (UTDFN)











L6.1.6x1.6A

6 LEAD ULTRA THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.45	0.50	0.55	-
A1	-	-	0.05	-
A3		0.127 REF		-
b	0.15	0.20	0.25	-
D	1.55	1.60	1.65	4
D2	0.40	0.45	0.50	-
E	1.55	1.60	1.65	4
E2	0.95	1.00	1.05	-
e		0.50 BSC		-
L	0.25	0.30	0.35	-

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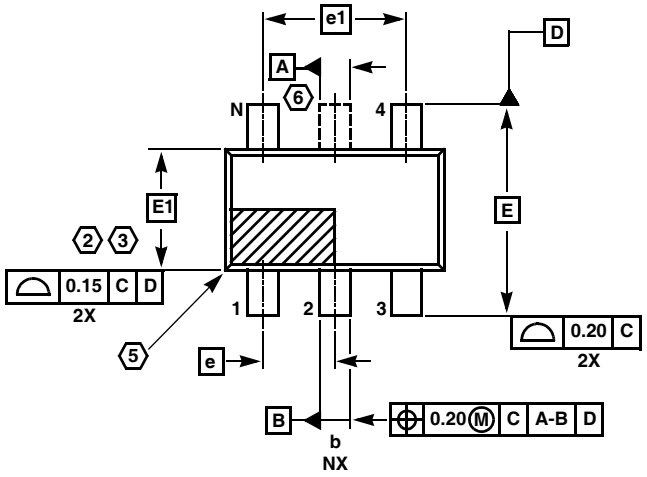
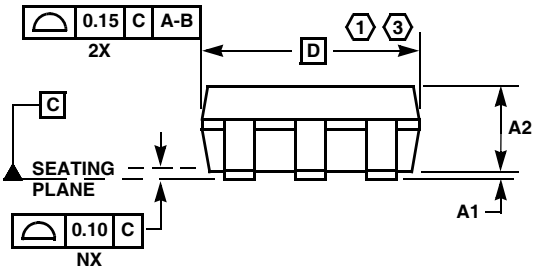
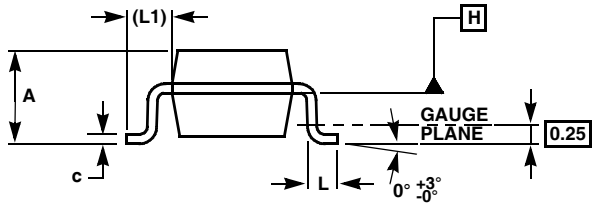
NOTES:

1. Dimensions are in mm. Angles in degrees.
2. Coplanarity applies to the exposed pad as well as the terminals. Coplanarity shall not exceed 0.08mm.
3. Warpage shall not exceed 0.10mm.
4. Package length/package width are considered as special characteristics.
5. JEDEC Reference MO-229.
6. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.

SOT-23 Package Family







MDP0038

SOT-23 PACKAGE FAMILY

SYMBOL	MILLIMETERS		TOLERANCE
	SOT23-5	SOT23-6	
A	1.45	1.45	MAX
A1	0.10	0.10	±0.05
A2	1.14	1.14	±0.15
b	0.40	0.40	±0.05
c	0.14	0.14	±0.06
D	2.90	2.90	Basic
E	2.80	2.80	Basic
E1	1.60	1.60	Basic
e	0.95	0.95	Basic
e1	1.90	1.90	Basic
L	0.45	0.45	±0.10
L1	0.60	0.60	Reference
N	5	6	Reference

Rev. F 2/07

NOTES:

1. Plastic or metal protrusions of 0.25mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. This dimension is measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Index area - Pin #1 I.D. will be located within the indicated zone (SOT23-6 only).
6. SOT23-5 version has no center lead (shown as a dashed line).

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