MAAL-011141-DIE

Low Noise Amplifier
DC - 28 GHz

Rev. V3

Features

- Ultra Wideband Performance
- Noise Figure: 1.4 dB @ 8 GHz
- High Gain: 17 dB @ 8 GHz
- Output IP3: 28 dBm @ 8 GHz
- Bias Voltage: V_{DD} = 5 - 6 V
- Bias Current: I_{DSQ} = 60 - 100 mA
- 50 Ω Matched Input / Output
- Positive Voltage Only
- Die Size: 2.99 x 1.5 x 0.1 mm
- RoHS* Compliant

Description

The MAAL-011141-DIE is an easy to use, wideband low noise distributed amplifier die. It operates from DC to 28 GHz and provides 17 dB of linear gain, 16 dBm of P1dB and 1.4 dB of noise figure at 8 GHz. The input and output are fully matched to 50 Ω with typical return loss >15 dB.

This amplifier employs an active termination circuit to achieve a lower noise figure at the lower end of the frequency range than is possible using traditional resistive termination techniques.

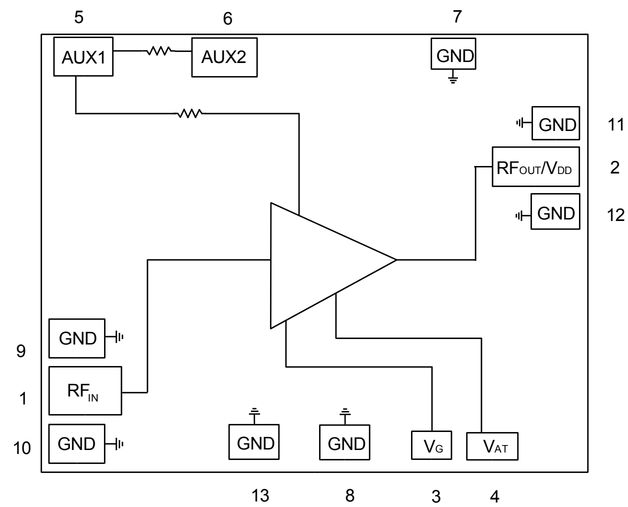
This product is fabricated using a GaAs pHEMT process which features full passivation for enhanced reliability.

The MAAL-011141-DIE can be used as a low noise amplifier stage or as a driver stage in higher power applications. This device is ideally suited for Test and Measurement, EW, ECM, and Radar applications.

Ordering Information

Part Number	Package
MAAL-011141-DIE	gel pack
MAAL-011141-DIESMB	wafer evaluation module

Functional Schematic[1]



1. Image not to scale.

Pin Configuration[2]

Pin #	Pin Name	Description
1	RF_{IN}	RF Input
2	RF_{OUT} / V_{DD}	RF Output / Drain Voltage
3	V_G	Gate Voltage
4	V_{AT}	Active Termination Voltage
5	AUX1	Auxiliary Drain Voltage 1
6	AUX2	Auxiliary Drain Voltage 2
7-13	GND	DC + RF Ground to Backside Via

2. Backside of die must be connected to RF, DC and thermal ground.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

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Electrical Specifications: T_A = +25°C, V_{DD} = 6 V, I_{DSQ} = 75 mA, V_{AT} = 5 V, Z_0 = 50 Ω

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	P_{IN} = -20 dBm 2.0 GHz 8.0 GHz 12.0 GHz 18.0 GHz 26.5 GHz	dB	16.5 — 15.0 — —	18.5 17.0 17.0 17.0 17.0	—
Output P1dB	2.0 GHz 8.0 GHz 12.0 GHz 18.0 GHz 26.5 GHz	dBm	—	17.0 16.0 16.0 15.0 12.5	—
OIP3	P_{IN} = -20 dBm / tone, 10 MHz Tone Spacing 2.0 GHz 8.0 GHz 12.0 GHz 18.0 GHz 26.5 GHz	dBm	—	29.5 28.0 26.5 26.0 22.5	—
Input Return Loss	P_{IN} = -20 dBm	dB	—	15	—
Output Return Loss	P_{IN} = -20 dBm	dB	—	15	—
Noise Figure	2.0 GHz 8.0 GHz 12.0 GHz 18.0 GHz 26.5 GHz	dB	—	2.5 1.4 1.6 2.4 4.0	3.0 — 2.2 — —
Isolation	P_{IN} = -20 dBm 2.0 GHz 8.0 GHz 12.0 GHz 18.0 GHz 26.5 GHz	dB	—	60 40 37 33 32	—
V_G	Adjusted to set I_{DSQ} = 75 mA	V	—	0.7	—
I_{AT}	V_{AT} = 5 V	mA	—	10	—

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Operating Conditions

Recommended biasing conditions are V_{DD} = 6 V, I_{DSQ} = 75 mA. Bias of 5 V must be applied to V_{AT} pin. I_{DSQ} is set by adjusting V_G after setting V_{DD} and V_{AT}. The drain bias voltage range, V_{DD}, is 5 to 6 V, and the quiescent drain current biasing is 60 to 100 mA. To maintain the best performance MACOM recommends using an active bias circuit for constant I_{DD}.

There are three possible bias methods:

1. The use of an external bias tee where the required V_{DD} is applied at RF_{OUT}/V_{DD} and V_G is set to provide a current bias (I_{DSQ}) of 60 to 100 mA. This provides wide band performance of DC - 28 GHz (depending on the bandwidth of the bias tee).

2. The direct application of V_{DD} to AUX1. Using this method provides for an operational frequency of 2 - 28 GHz. However, a voltage drop across an internal 17 Ω resistance must be accounted for. For example, with I_{DSQ} = 75 mA, 7.3 V must be applied at AUX1 for a V_{DD} of 6 V.

3. The direct application of V_{DD} to AUX2. Using this method provides for an operational frequency of DC - 28 GHz. However, a voltage drop across series 17 Ω and 32 Ω resistors must be accounted for. For example, with I_{DSQ} = 75 mA, 9.67 V must be applied at AUX2 for a V_{DD} of 6 V.

In all cases DC blocking is required on the RF input. Additionally options 2 or 3 require DC blocking on the RF output line. It should also be noted that when using the internal bias circuit (option 2 or 3) I_{DSQ} is limited to a maximum of 80 mA.

Regardless of bias method used, 2 bypass capacitors of 100 pF and 0.1 µF should be connected to AUX2. This provides for increased device stability margins and improved gain flatness below 2 GHz when required. The 100 pF cap is a single layer chip capacitor and should be positioned as close to the device as possible. The 0.1 µF SMT cap can be placed further away on the PCB.

The available evaluation board is configured for bias option 3 using AUX2 for the supply of V_{DD}.

Maximum Operating Conditions

Parameter	Operating Maximum
Input Power[3]	P_{IN} ≤1 dB compression level
Junction Temperature[4]	+150°C
Operating Temperature	-40°C to +85°C

3. MACOM does not recommend sustained operation at power levels above 1 dB gain compression.
4. Operating at nominal conditions with junction temperature ≤ +150°C will ensure MTTF > 1 x 10^6 hours.

Absolute Maximum Ratings[5,6]

Parameter	Absolute Maximum
Input Power	18 dBm
Drain Voltage	7 V
Gate Voltage	0.9 V
Active Termination Voltage	6 V
AUX1 Current	80 mA
AUX2 Current	80 mA
Junction Temperature[7]	+175°C
Storage Temperature	-65°C to +125°C

5. Exceeding any one or combination of these limits may cause permanent damage to this device.
6. MACOM does not recommend sustained operation near these survivability limits.
7. Junction temperature directly effects device MTTF, and should be kept as low as possible to maximize product lifetime.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1A devices.

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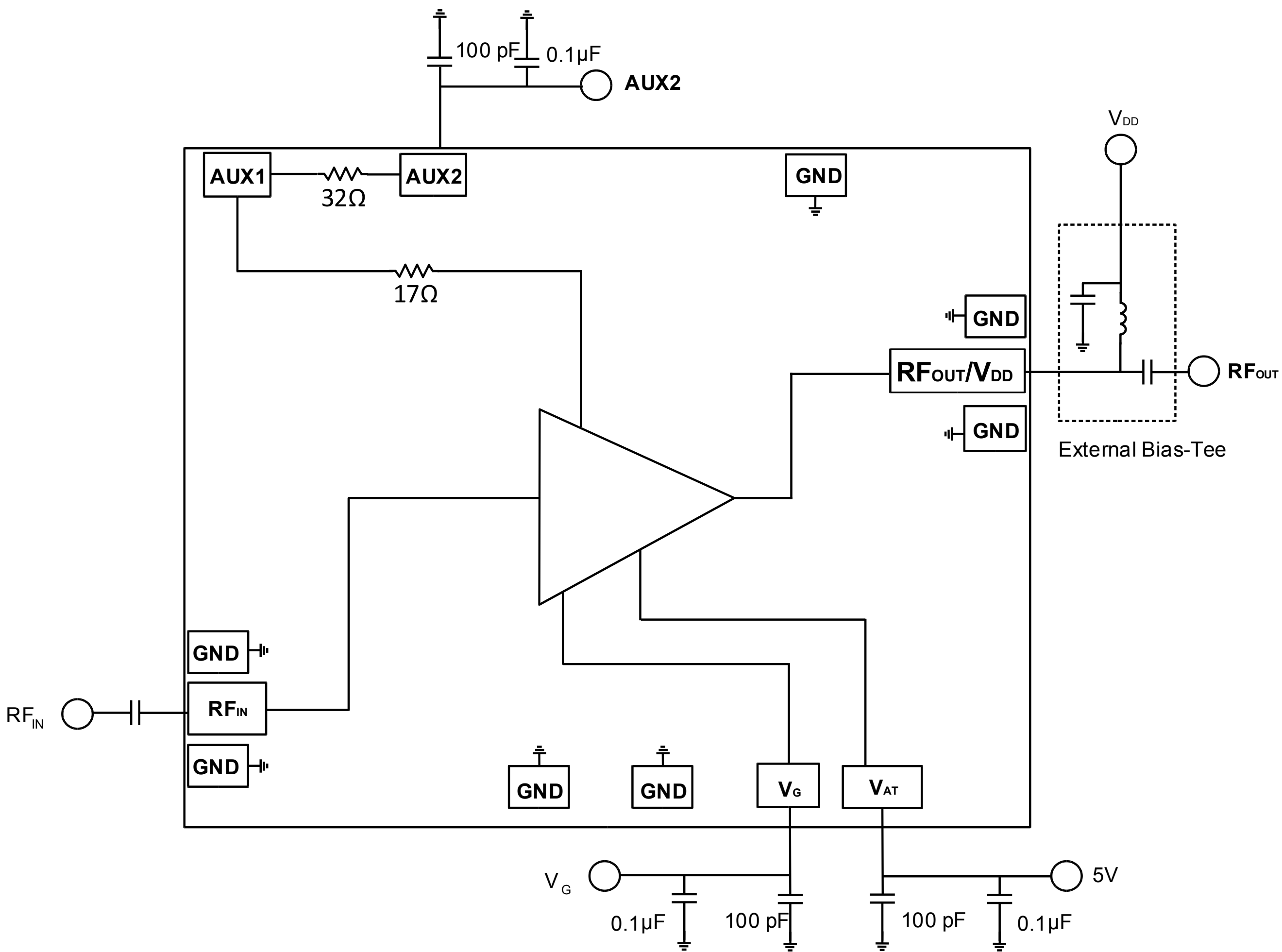
Application Schematic



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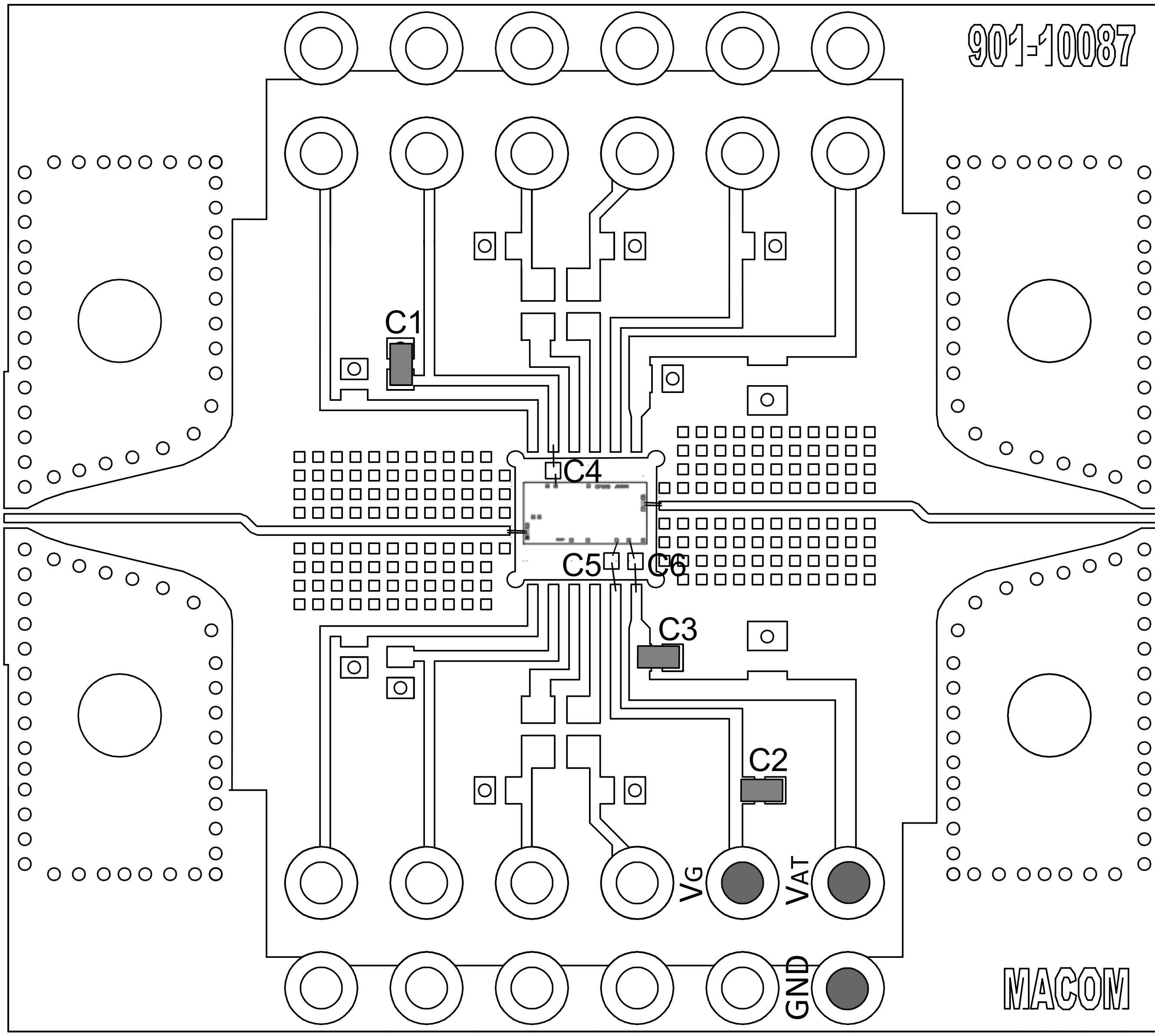
Applications Section: Sample Board Layout



Parts List

Part	Value	Case Style
C1 - C3	0.1 µF	0402
C4 - C6	100 pF	Single Layer

Evaluation PCB Specifications

Top Layer: 1/2 oz Copper Cladding, 0.017 mm thickness *Dielectric Layer:* Rogers RO4350B 0.101 mm thickness *Bottom Layer:* 1/2 oz Copper Cladding, 0.017 mm thickness *Finished overall thickness:* 0.135 mm

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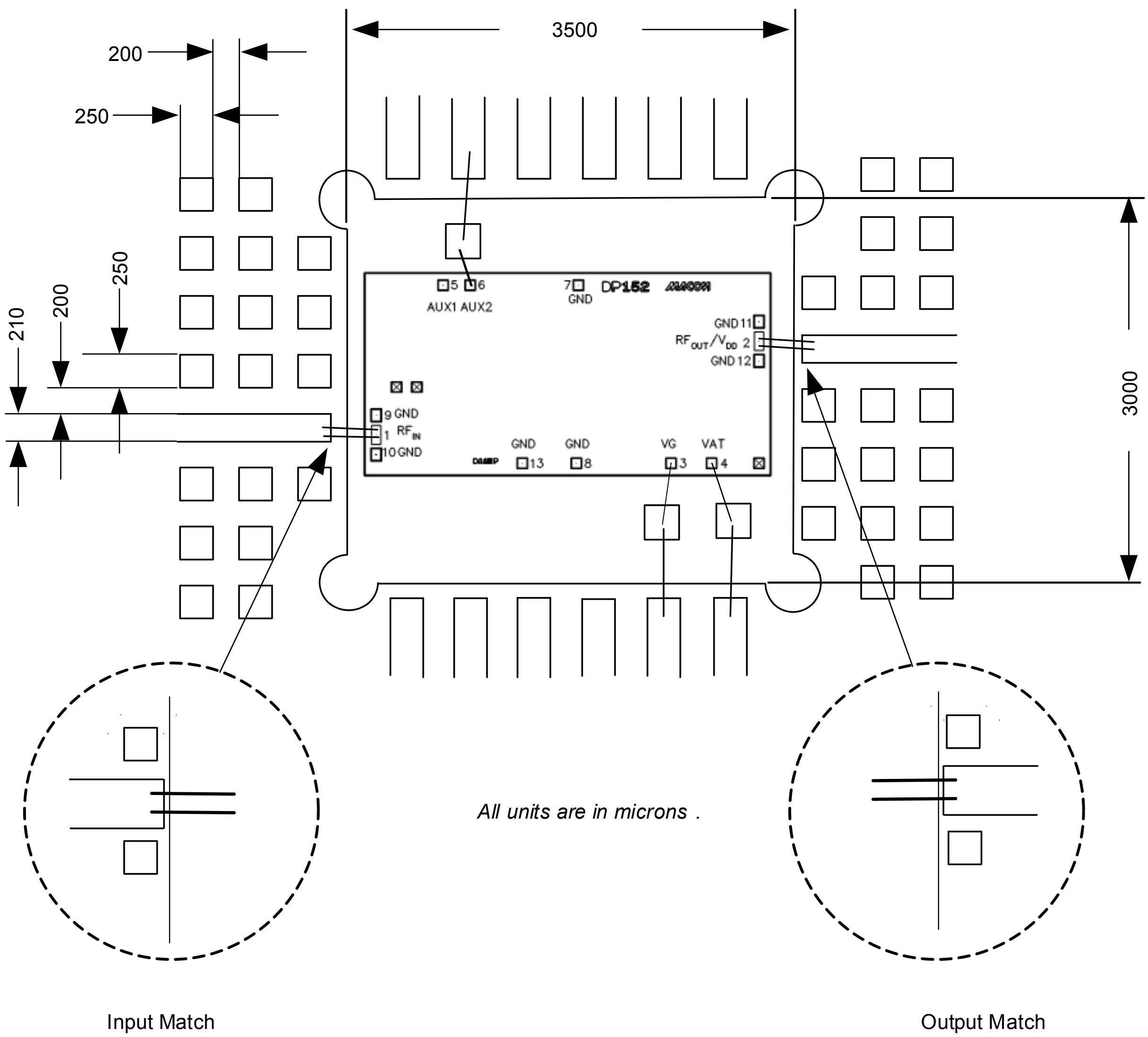
Recommended Bonding Diagram & PCB Layout

RF input and output port matching circuit patterns are designed to compensate for bonding wires. Input and output matching are identical.



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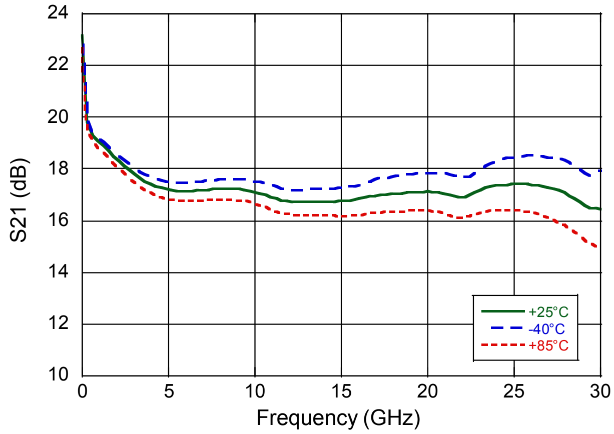
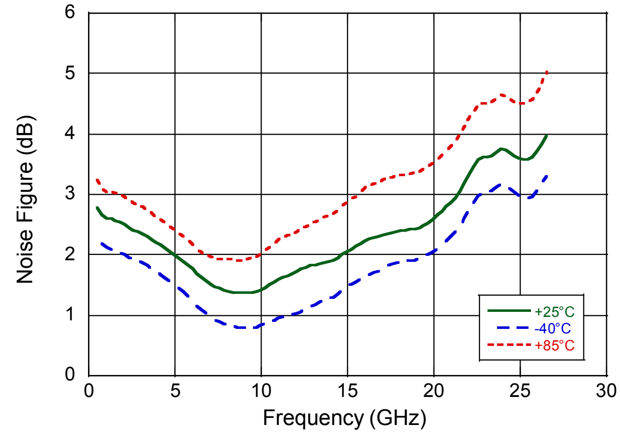
Typical Performance Curves: V_{DD} = 6 V, I_{DSQ} = 75 mA, V_{AT} = 5 V

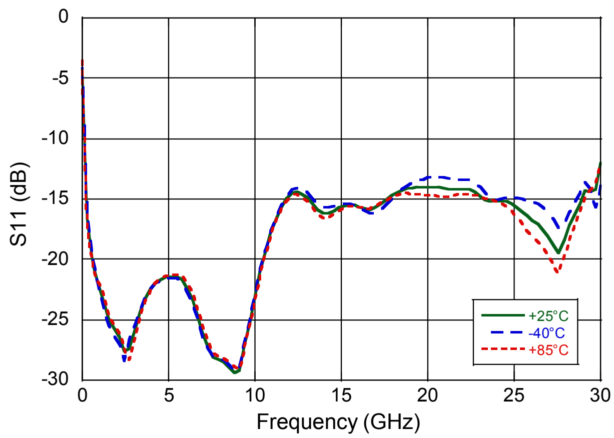
Gain



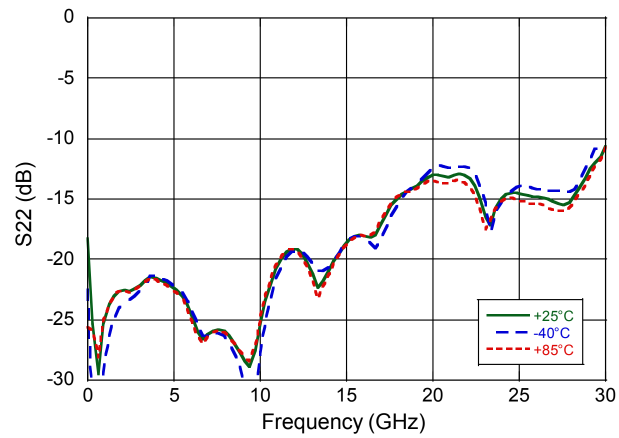
Noise Figure



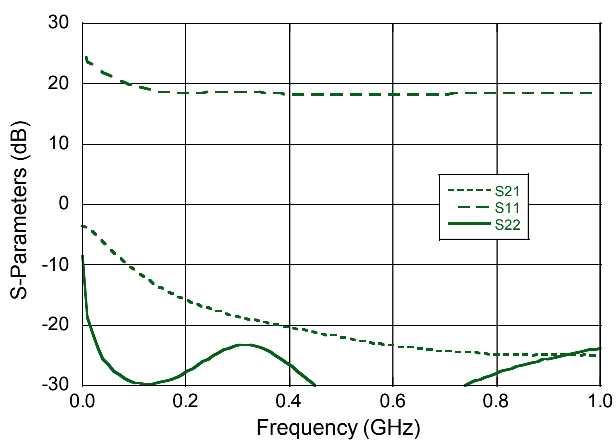
Input Return loss



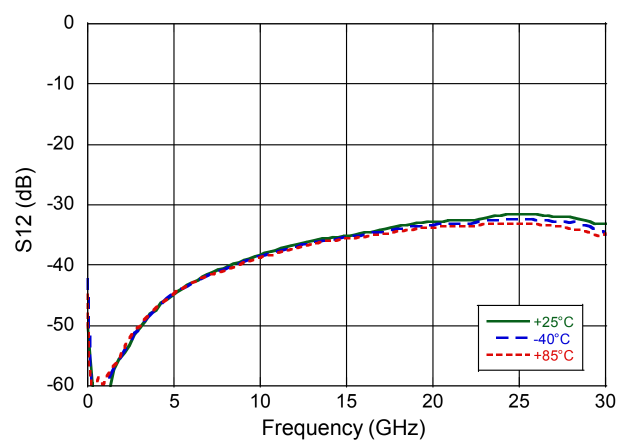
Output Return Loss



Low Frequency S-Parameters



Reverse Isolation



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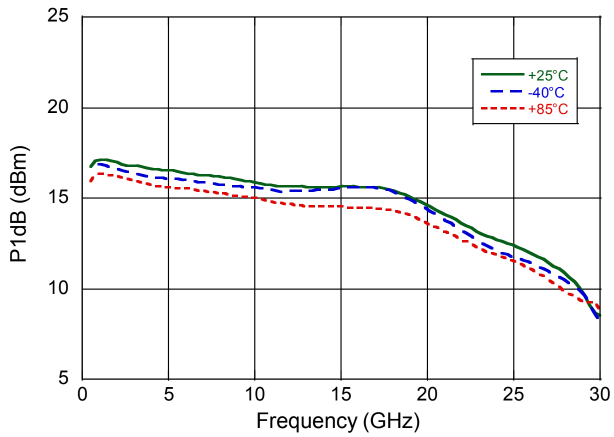
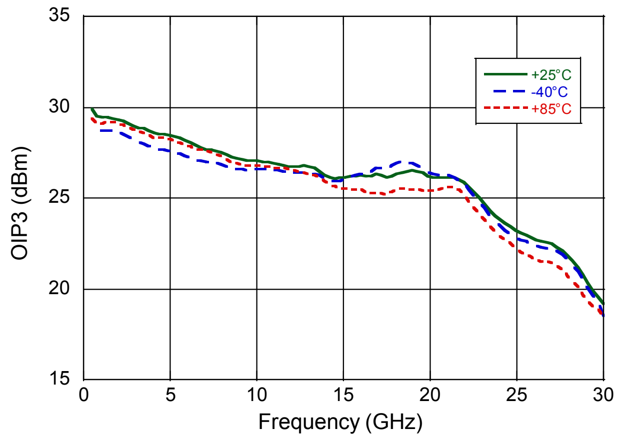
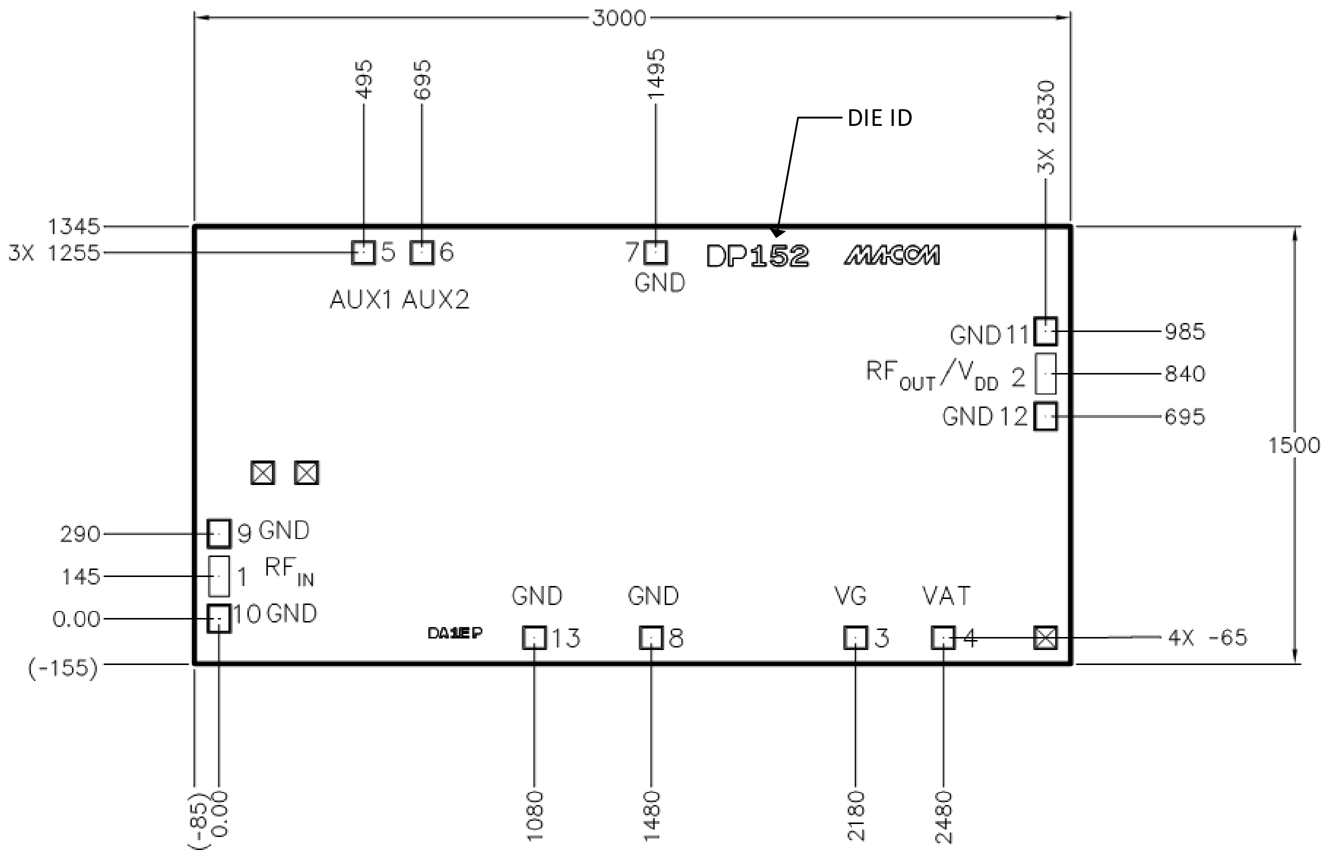
Output P1dB



Output IP3 (10 MHz tone spacing)



MMIC Die Outline



Bond Pad Detail[8,9]

Pin #	Size (x)	Size (y)
1 - 2	70	140
9 -12	70	90
3 - 8, 13	70	70

8. All dimensions shown as microns (µm) with a tolerance of +/-5 µm, unless otherwise noted.
9. Die thickness is 100 µm +/- 10 µm.

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