

MOSFET – Power, Single, N-Channel, TOLL

60 V, 0.9 mΩ, 422 A

NTBLS001N06C

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- Lowers Switching Noise/EMI
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Power Tools, Battery Operated Vacuums
- UAV/Drones, Material Handling
- BMS/Storage, Home Automation

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	60	V
Gate-to-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	$T_C = 25^\circ\text{C}$	I_D	422 A
		$T_C = 25^\circ\text{C}$	P_D	284 W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25^\circ\text{C}$	I_D	51 A
		$T_A = 25^\circ\text{C}$	P_D	4.2 W
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	I_{DM}	900	A
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +175	$^\circ\text{C}$
Source Current (Body Diode)		I_S	236	A
Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 39 \text{ A}$)		E_{AS}	760	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^\circ\text{C}$

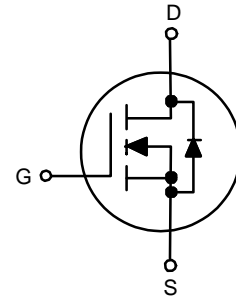
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 2)	$R_{\theta JC}$	0.53	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	36	

1. Surface-mounted on FR4 board using a 1 in² pad size, 2 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

$V_{(BR)DSS}$	$R_{DS(ON) MAX}$	$I_D MAX$
60 V	0.9 mΩ @ 10 V	422 A
	1.4 mΩ @ 6 V	



MO-299A
TOLL
CASE
100CU

ORDERING INFORMATION

Device	Package	Shipping†
NTBLS001N06C	MO-299A (Pb-Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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Table 1. ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 562 \mu\text{A}, \text{ref to } 25^\circ\text{C}$		26		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$	$T_J = 25^\circ\text{C}$		10	μA
			$T_J = 125^\circ\text{C}$		100	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = 20 \text{ V}$			100	nA
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 562 \mu\text{A}$	2.0	2.8	4.0	V
Negative Threshold Temperature Coefficient	$V_{GS(th)}/T_J$	$I_D = 562 \mu\text{A}, \text{ref to } 25^\circ\text{C}$		9.9		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 80 \text{ A}$		0.75	0.9	m Ω
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 6 \text{ V}, I_D = 56 \text{ A}$		1.09	1.4	m Ω
Forward Transconductance	g_{FS}	$V_{DS} = 5 \text{ V}, I_D = 80 \text{ A}$		290		S
Gate-Resistance	R_G	$T_A = 25^\circ\text{C}$		0.6		Ω
CHARGES & CAPACTIANCES						
Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V}, V_{DS} = 30 \text{ V}, f = 10 \text{ kHz}$		11575		pF
Output Capacitance	C_{oss}			5973		pF
Reverse Transfer Capacitance	C_{rss}			76		pF
Total Gate Charge	$Q_{G(tot)}$	$V_{GS} = 10 \text{ V}, V_{DS} = 30 \text{ V}, I_D = 80 \text{ A}$		143		nC
Threshold Gate Charge	$Q_{G(th)}$			31		nC
Gate-to-Source Charge	Q_{gs}			54		nC
Gate-to-Drain Charge	Q_{gd}			13		nC
Total Gate Charge	$Q_{G(tot)}$	$V_{GS} = 6 \text{ V}, V_{DS} = 30 \text{ V}, I_D = 80 \text{ A}$		52		nC
SWITCHING CHARACTERISTICS, $V_{GS} = 10 \text{ V}$ (Note 3)						
Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10 \text{ V}, V_{DS} = 30 \text{ V}, I_D = 80 \text{ A}, R_G = 6 \Omega$		34		ns
Rise Time	t_r			53		ns
Turn-Off Delay Time	$t_{d(off)}$			119		ns
Fall Time	t_f			91		ns
DRAIN-SOURCE DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	$I_S = 80 \text{ A}, V_{GS} = 0 \text{ V}$	$T_J = 25^\circ\text{C}$	0.79	1.2	V
		$I_S = 80 \text{ A}, V_{GS} = 0 \text{ V}$	$T_J = 125^\circ\text{C}$	0.66		V
Reverse Recovery Time	t_{rr}	$V_{GS} = 0 \text{ V}, di_S/dt = 100 \text{ A}/\mu\text{s}, I_S = 56 \text{ A}$		120		ns
Charge Time	t_a			60		ns
Discharge Time	t_b			60		ns
Reverse Recovery Charge	Q_{rr}			322		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures

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TYPICAL CHARACTERISTICS

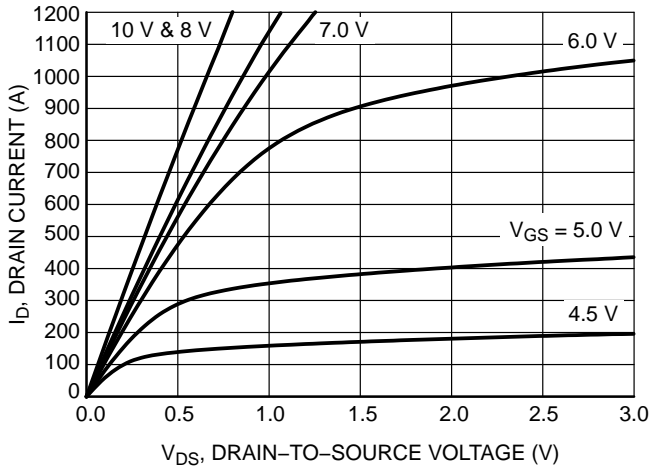


Figure 1. On-Region Characteristics

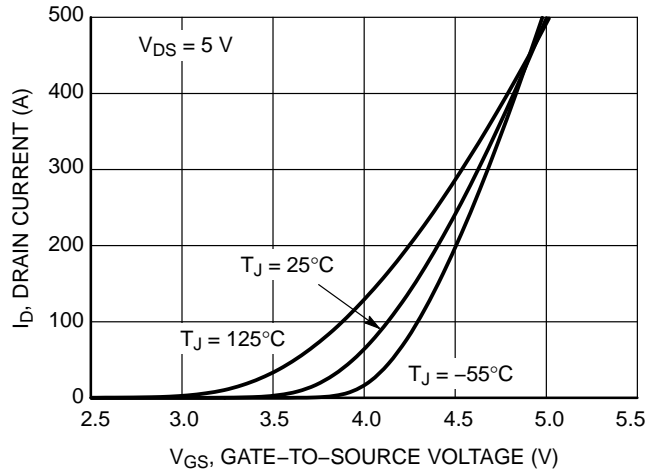


Figure 2. Transfer Characteristics

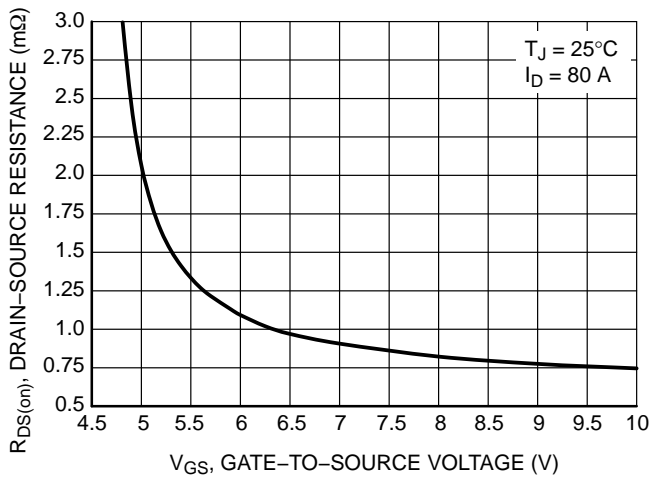


Figure 3. On-Resistance vs. V_{GS}

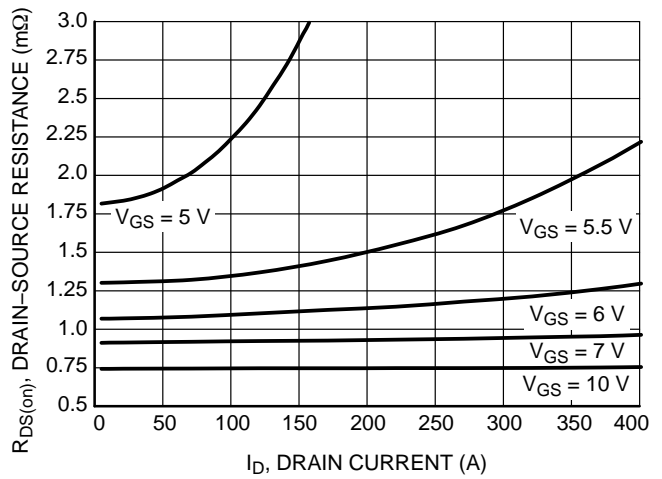


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

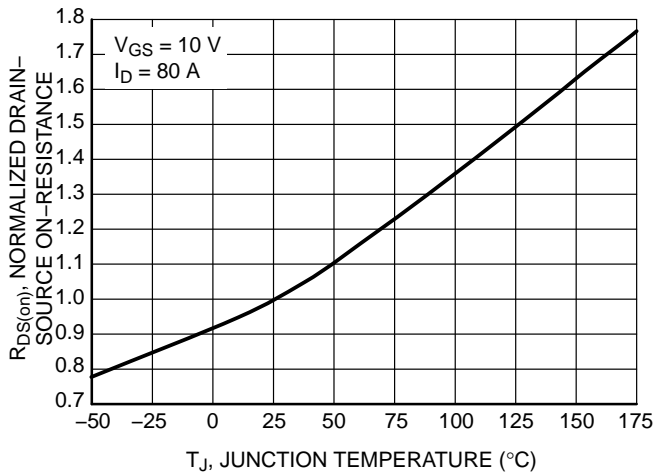


Figure 5. On-Resistance Variation with Temperature

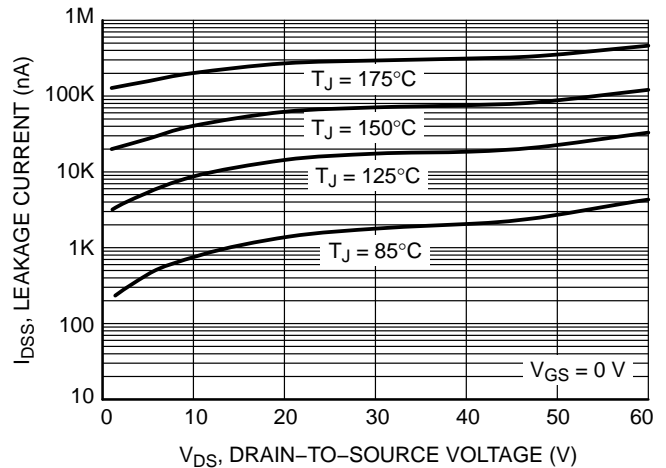


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

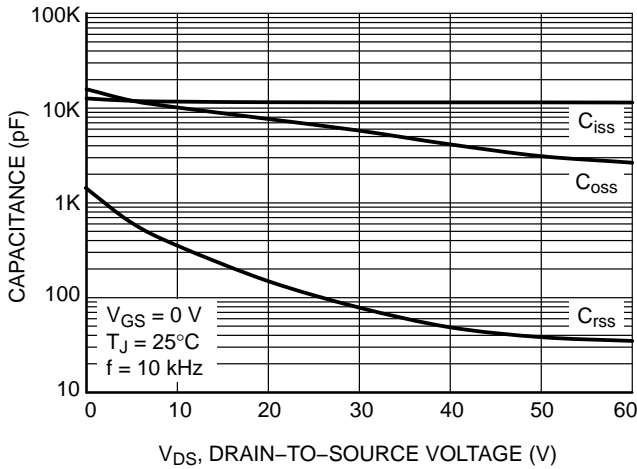


Figure 7. Capacitance Variation

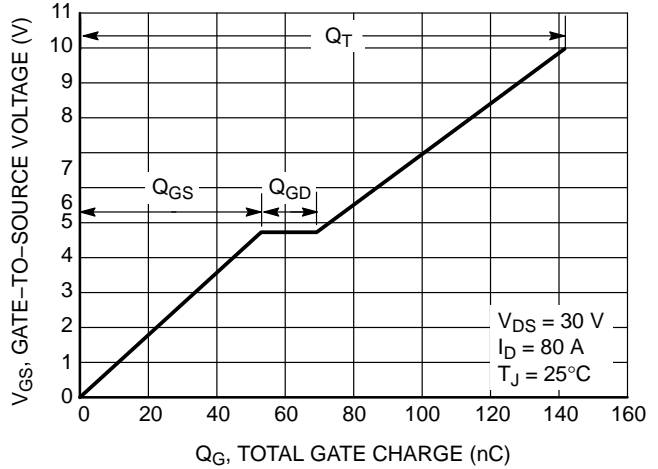


Figure 8. Gate-to-Source Voltage vs. Total Gate Charge

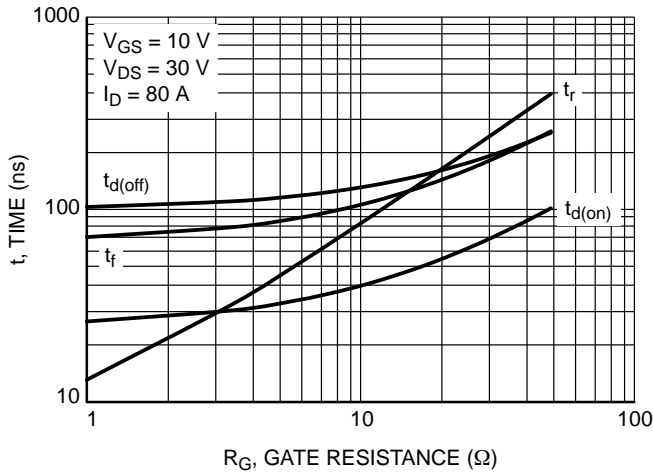


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

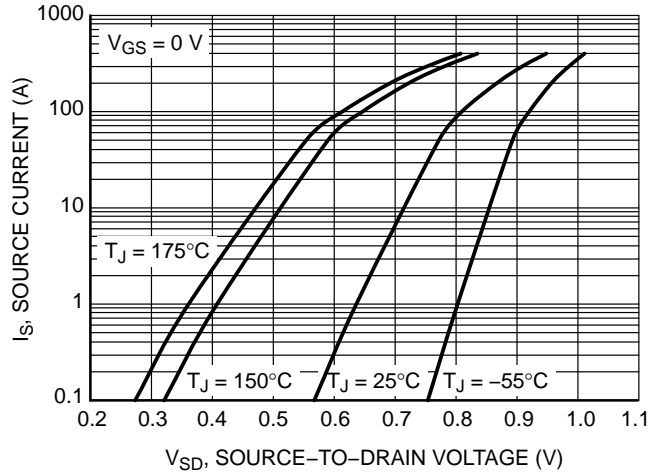


Figure 10. Diode Forward Voltage vs. Current

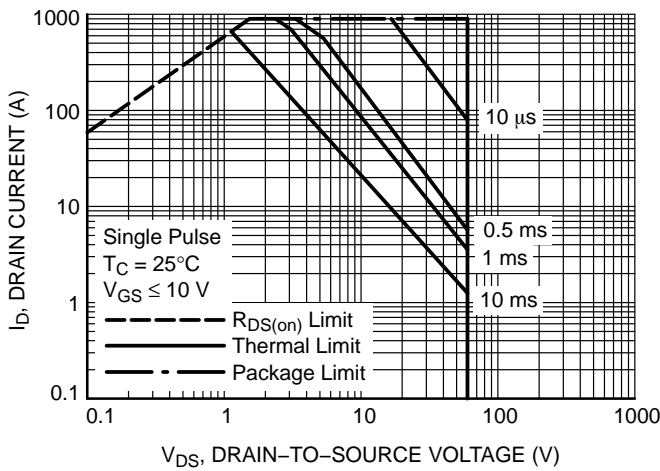


Figure 11. Maximum Rated Forward Biased Safe Operating Area

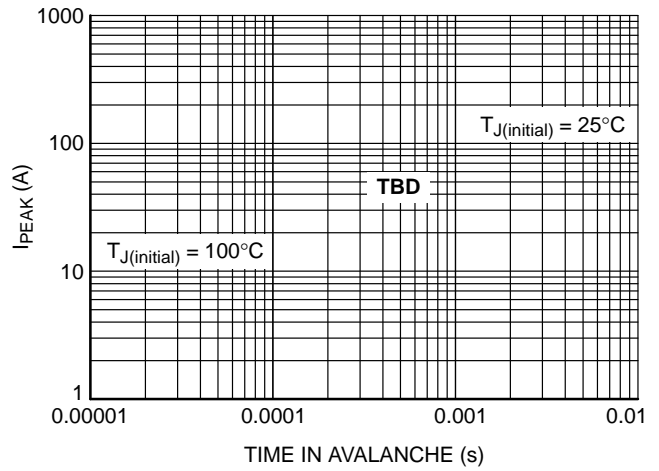


Figure 12. Peak Power

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TYPICAL CHARACTERISTICS

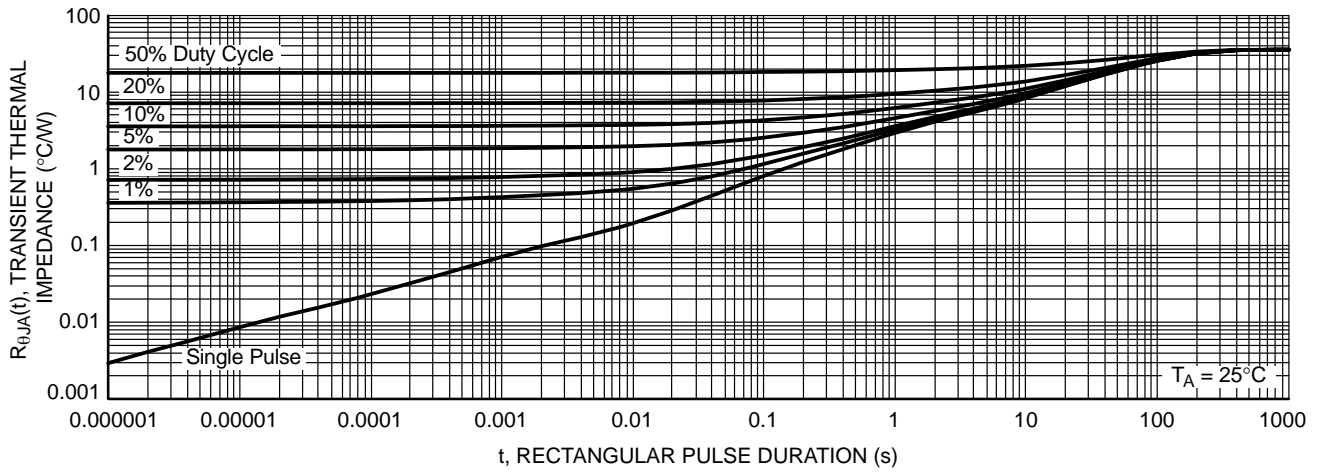


Figure 13. Thermal Response (Junction-to-Ambient)

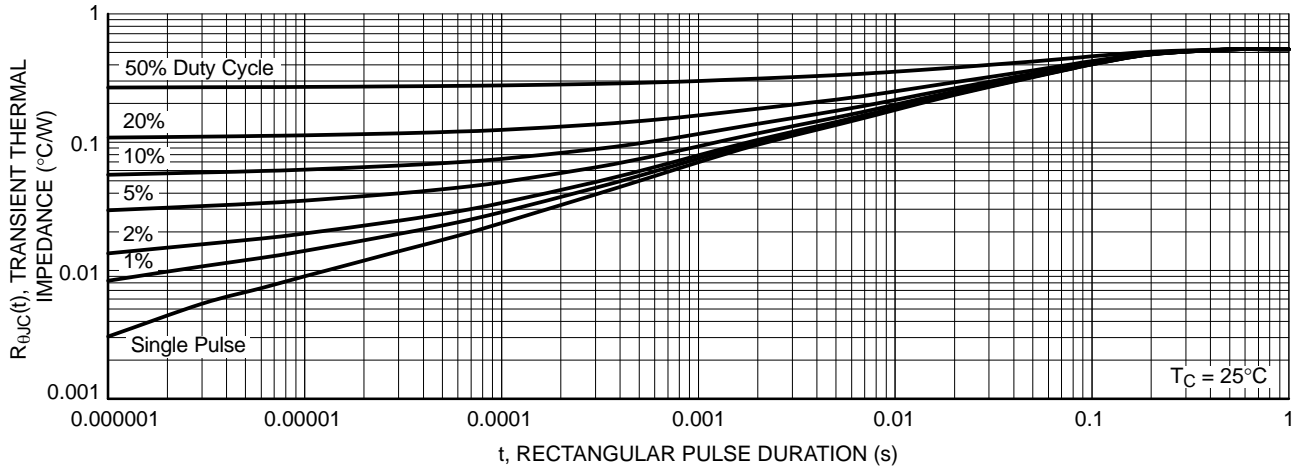
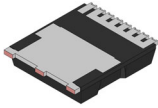
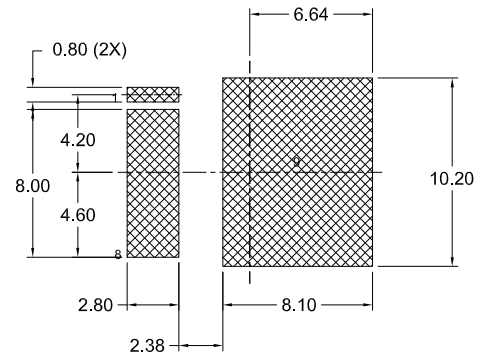
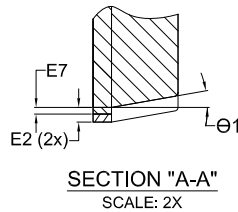
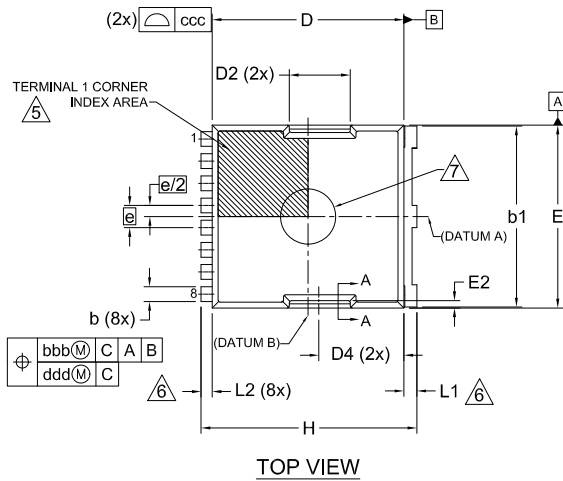


Figure 14. Thermal Response

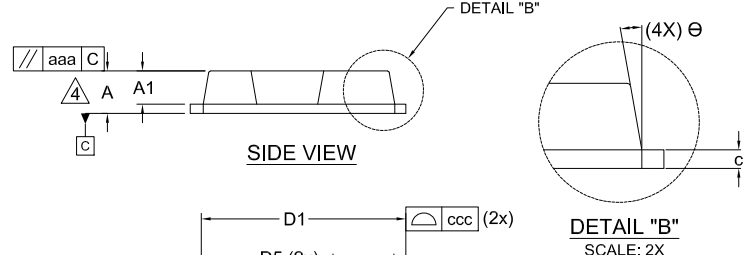


H-PSOF8L 11.68x9.80x2.30, 1.20P
CASE 100CU
ISSUE F

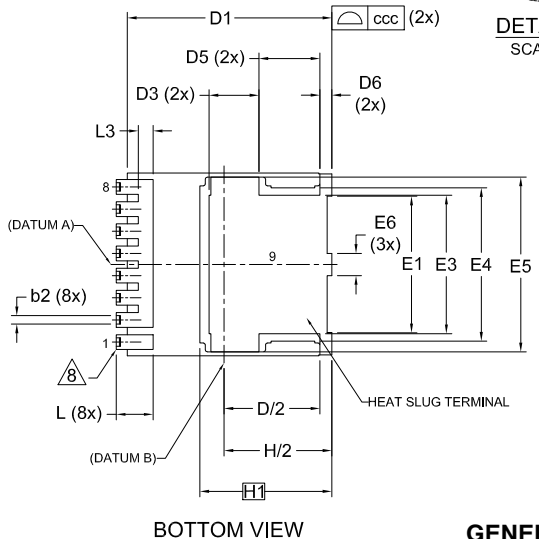
DATE 30 JUL 2024



LAND PATTERN RECOMMENDATION
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.



- NOTES:
1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE B.
 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
 3. "e" REPRESENTS THE TERMINAL PITCH.
 4. THIS DIMENSION INCLUDES ENCAPSULATION THICKNESS "A1", AND PACKAGE BODY THICKNESS, BUT DOES NOT INCLUDE ATTACHED FEATURES, e.g., EXTERNAL OR CHIP CAPACITORS. AN INTEGRAL HEATSLUG IS NOT CONSIDERED AS ATTACHED FEATURE.
 5. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE HATCHED AREA.
 6. DIMENSIONS b1,L1,L2 APPLY TO PLATED TERMINALS.
 7. THE LOCATION AND SIZE OF EJECTOR MARKS ARE OPTIONAL.
 8. THE LOCATION AND NUMBER OF FUSED LEADS ARE OPTIONAL.

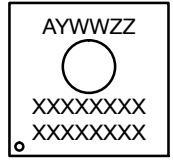


DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.35	0.45	0.55
c	0.40	0.50	0.60
D	10.28	10.38	10.48
D/2	5.09	5.19	5.29
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D3	2.60	2.70	2.80
D4	4.45	4.55	4.65
D5	3.20	3.30	3.40
D6	0.55	0.65	0.75
E	9.80	9.90	10.00
E1	7.30	7.40	7.50
E2	0.30	0.40	0.50
E3	7.40	7.50	7.60
E4	8.20	8.30	8.40

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E5	9.36	9.46	9.56
E6	1.10	1.20	1.30
E7	0.15	0.18	0.21
e	1.20 BSC		
e/2	0.60 BSC		
H	11.58	11.68	11.78
H/2	5.74	5.84	5.94
H1	7.15 BSC		
L	1.90	2.00	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.70	0.80	0.90
θ	10° REF		
θ1	10° REF		
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		

GENERIC MARKING DIAGRAM*

A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code
XXXX = Specific Device Code



*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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