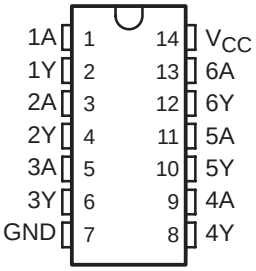
- **Dependable Texas Instruments Quality and Reliability**

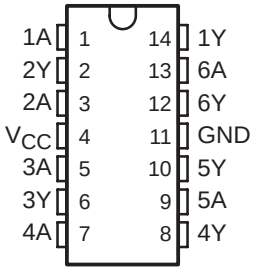
## description/ordering information

These devices contain six independent inverters.

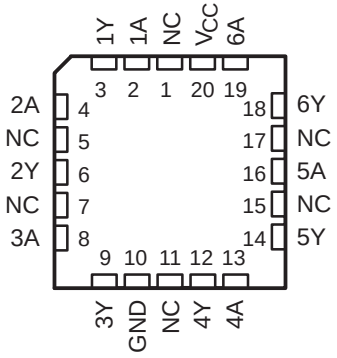
**SN5404 . . . J PACKAGE**
**SN54LS04, SN54S04 . . . J OR W PACKAGE**
**SN7404, SN74S04 . . . D, N, OR NS PACKAGE**
**SN74LS04 . . . D, DB, N, OR NS PACKAGE**
**(TOP VIEW)**




**SN5404 . . . W PACKAGE**
**(TOP VIEW)**




**SN54LS04, SN54S04 . . . FK PACKAGE**
**(TOP VIEW)**




NC − No internal connection

## ORDERING INFORMATION

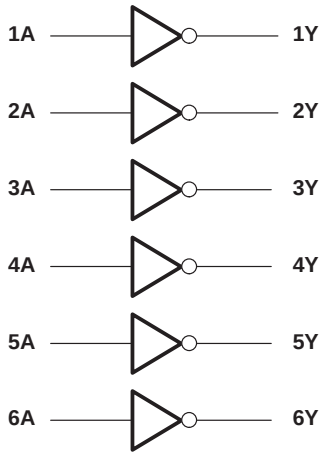
| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| 0°C to 70°C | PDIP − N | Tube | SN7404N | SN7404N |
| | | Tube | SN74LS04N | SN74LS04N |
| | | Tube | SN74S04N | SN74S04N |
| | SOIC − D | Tube | SN7404D | 7404 |
| | | Tape and reel | SN7404DR | |
| | | Tube | SN74LS04D | LS04 |
| | | Tape and reel | SN74LS04DR | |
| | | Tube | SN74S04D | S04 |
| | | Tape and reel | SN74S04DR | |
| | SOP − NS | Tape and reel | SN7404NSR | SN7404 |
| | | Tape and reel | SN74LS04NSR | 74LS04 |
| | | Tape and reel | SN74S04NSR | 74S04 |
| | SSOP − DB | Tape and reel | SN74LS04DBR | LS04 |
| −55°C to 125°C | CDIP − J | Tube | SN5404J | SN5404J |
| | | Tube | SNJ5404J | SNJ5404J |
| | | Tube | SN54LS04J | SN54LS04J |
| | | Tube | SN54S04J | SN54S04J |
| | | Tube | SNJ54LS04J | SNJ54LS04J |
| | | Tube | SNJ54S04J | SNJ54S04J |
| | CFP − W | Tube | SNJ5404W | SNJ5404W |
| | | Tube | SNJ54LS04W | SNJ54LS04W |
| | | Tube | SNJ54S04W | SNJ54S04W |
| | LCCC − FK | Tube | SNJ54LS04FK | SNJ54LS04FK |
| | | Tube | SNJ54S04FK | SNJ54S04FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**FUNCTION TABLE**
**(each inverter)**

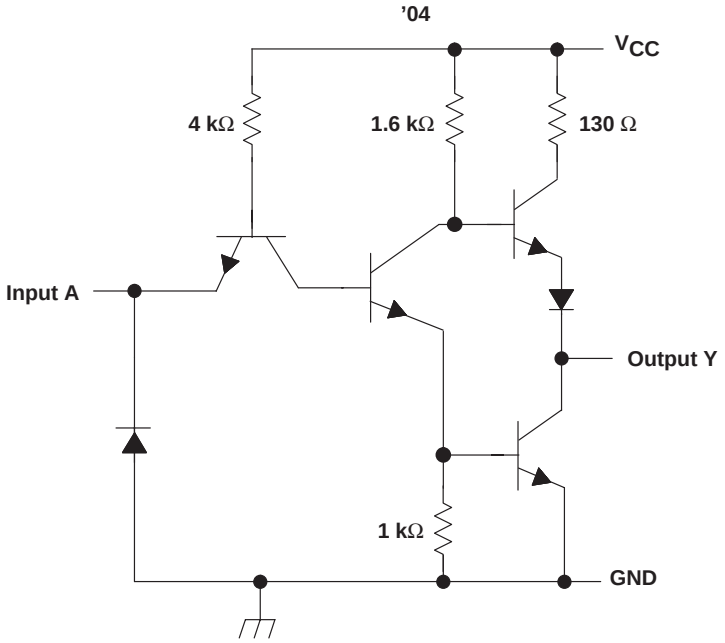
| INPUT A | OUTPUT Y |
|---|---|
| H | L |
| L | H |

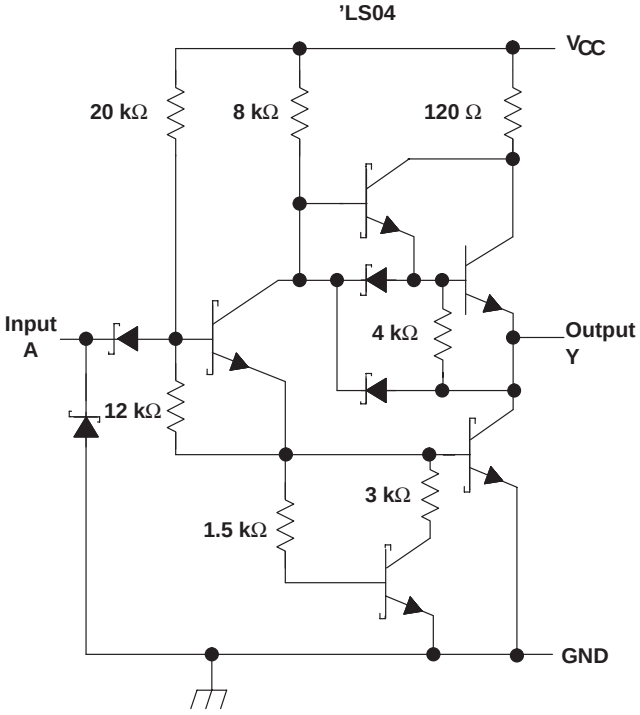
## logic diagram (positive logic)

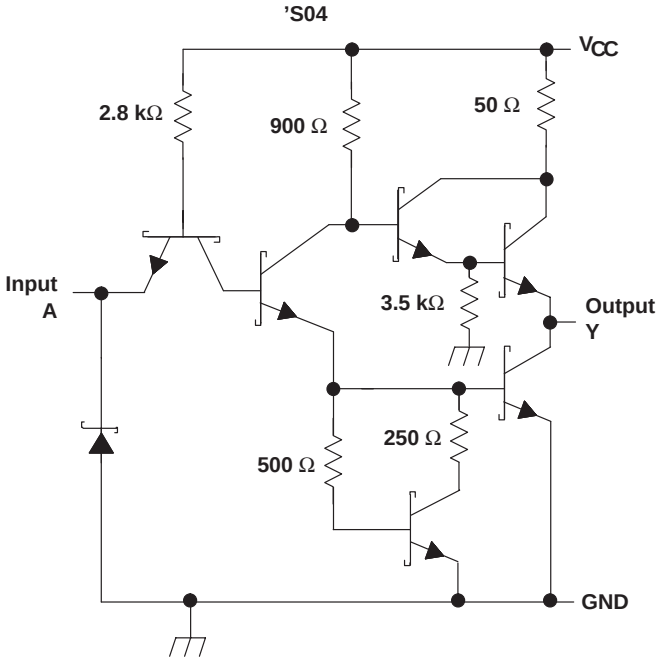



$Y = \overline{A}$

## schematics (each gate)




Resistor values shown are nominal.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage, $V_I$: '04, 'S04 . . . . . 5.5 V
'LS04 . . . . . 7 V
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package . . . . . 86°C/W
DB package . . . . . 96°C/W
N package . . . . . 80°C/W
NS package . . . . . 76°C/W
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 3)

| | | SN5404 | | | SN7404 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | −0.4 | | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | | | 16 | | | 16 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

NOTE 3: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS‡ | | | SN5404 | | | SN7404 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP§ | MAX | MIN | TYP§ | MAX | |
| $V_{IK}$ | $V_{CC}$ = MIN, | $I_I$ = −12 mA | | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | $V_{CC}$ = MIN, | $V_{IL}$ = 0.8 V, | $I_{OH}$ = −0.4 mA | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| $V_{OL}$ | $V_{CC}$ = MIN, | $V_{IH}$ = 2 V, | $I_{OL}$ = 16 mA | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| $I_I$ | $V_{CC}$ = MAX, | $V_I$ = 5.5 V | | | | 1 | | | 1 | mA |
| $I_{IH}$ | $V_{CC}$ = MAX, | $V_I$ = 2.4 V | | | | 40 | | | 40 | µA |
| $I_{IL}$ | $V_{CC}$ = MAX, | $V_I$ = 0.4 V | | | | −1.6 | | | −1.6 | mA |
| $I_{OS}$¶ | $V_{CC}$ = MAX | | | −20 | | −55 | −18 | | −55 | mA |
| $I_{CCH}$ | $V_{CC}$ = MAX, | $V_I$ = 0 V | | | 6 | 12 | | 6 | 12 | mA |
| $I_{CCL}$ | $V_{CC}$ = MAX, | $V_I$ = 4.5 V | | | 18 | 33 | | 18 | 33 | mA |

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
¶ Not more than one output should be shorted at a time.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | SN5404 SN7404 | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | |
| $t_{PLH}$ | A | Y | $R_L$ = 400 Ω, $C_L$ = 15 pF | | 12 | 22 | ns |
| $t_{PHL}$ | | | | | 8 | 15 | |

## recommended operating conditions (see Note 3)

| | | SN54LS04 | | | SN74LS04 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.7 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | −0.4 | | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | | | 4 | | | 8 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

NOTE 3: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS† | | | SN54LS04 | | | SN74LS04 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | $V_{CC}$ = MIN, | $I_I$ = −18 mA | | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | $V_{CC}$ = MIN, | $V_{IL}$ = MAX, | $I_{OH}$ = −0.4 mA | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| $V_{OL}$ | $V_{CC}$ = MIN, | $V_{IH}$ = 2 V | $I_{OL}$ = 4 mA | | 0.25 | 0.4 | | | 0.4 | V |
| | | | $I_{OL}$ = 8 mA | | | | | 0.25 | 0.5 | |
| $I_I$ | $V_{CC}$ = MAX, | $V_I$ = 7 V | | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = MAX, | $V_I$ = 2.7 V | | | | 20 | | | 20 | μA |
| $I_{IL}$ | $V_{CC}$ = MAX, | $V_I$ = 0.4 V | | | | −0.4 | | | −0.4 | mA |
| $I_{OS}$§ | $V_{CC}$ = MAX | | | −20 | | −100 | −20 | | −100 | mA |
| $I_{CCH}$ | $V_{CC}$ = MAX, | $V_I$ = 0 V | | | 1.2 | 2.4 | | 1.2 | 2.4 | mA |
| $I_{CCL}$ | $V_{CC}$ = MAX, | $V_I$ = 4.5 V | | | 3.6 | 6.6 | | 3.6 | 6.6 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | SN54LS04 SN74LS04 | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | |
| $t_{PLH}$ | A | Y | $R_L$ = 2 kΩ, $C_L$ = 15 pF | | 9 | 15 | ns |
| $t_{PHL}$ | | | | | 10 | 15 | |

## recommended operating conditions (see Note 3)

| | | SN54S04 | | | SN74S04 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | −1 | | | −1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 20 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

NOTE 3: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

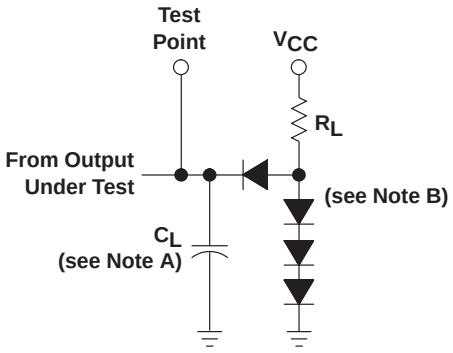
| PARAMETER | TEST CONDITIONS† | | | SN54S04 | | | SN74S04 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | $V_{CC}$ = MIN, | $I_I$ = −18 mA | | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = MIN, | $V_{IL}$ = 0.8 V, | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| $V_{OL}$ | $V_{CC}$ = MIN, | $V_{IH}$ = 2 V, | $I_{OL}$ = 20 mA | | | 0.5 | | | 0.5 | V |
| $I_I$ | $V_{CC}$ = MAX, | $V_I$ = 5.5 V | | | | 1 | | | 1 | mA |
| $I_{IH}$ | $V_{CC}$ = MAX, | $V_I$ = 2.7 V | | | | 50 | | | 50 | µA |
| $I_{IL}$ | $V_{CC}$ = MAX, | $V_I$ = 0.5 V | | | | −2 | | | −2 | mA |
| $I_{OS}$§ | $V_{CC}$ = MAX | | | −40 | | −100 | −40 | | −100 | mA |
| $I_{CCH}$ | $V_{CC}$ = MAX, | $V_I$ = 0 V | | | 15 | 24 | | 15 | 24 | mA |
| $I_{CCL}$ | $V_{CC}$ = MAX, | $V_I$ = 4.5 V | | | 30 | 54 | | 30 | 54 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

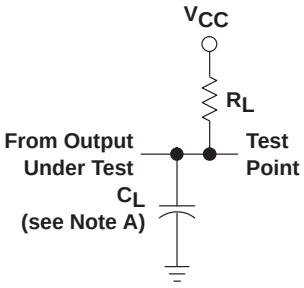
## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | | SN54S04 SN74S04 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | |
| $t_{PLH}$ | A | Y | $R_L$ = 280 Ω, | $C_L$ = 15 pF | | 3 | 4.5 | ns |
| $t_{PHL}$ | | | | | | 3 | 5 | |
| $t_{PLH}$ | A | Y | $R_L$ = 280 Ω, | $C_L$ = 50 pF | | 4.5 | | ns |
| $t_{PHL}$ | | | | | | 5 | | |

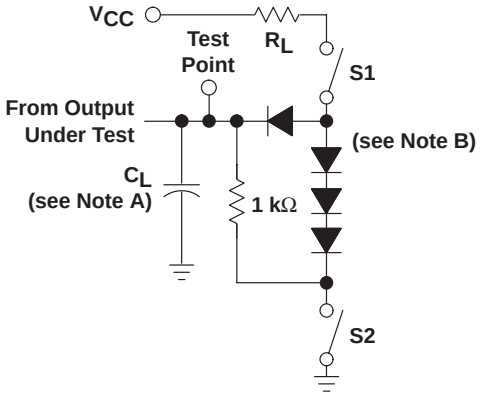
## PARAMETER MEASUREMENT INFORMATION
## SERIES 54/74 AND 54S/74S DEVICES



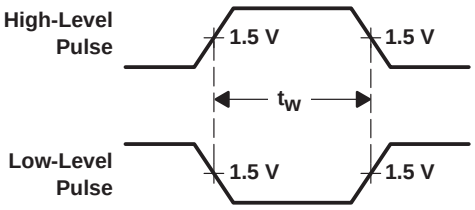

**LOAD CIRCUIT
FOR 2-STATE TOTEM-POLE OUTPUTS**



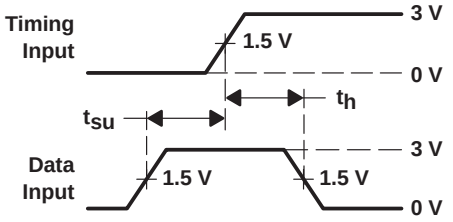

**LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS**



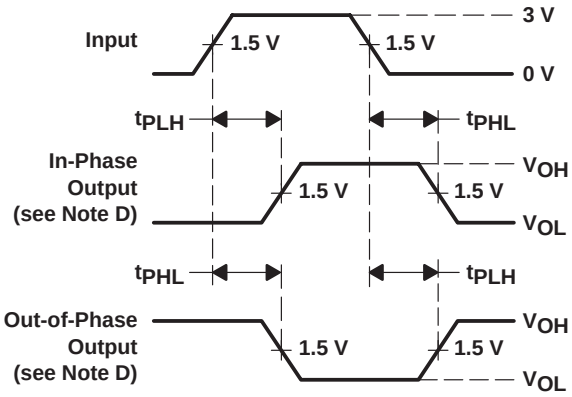

**LOAD CIRCUIT
FOR 3-STATE OUTPUTS**



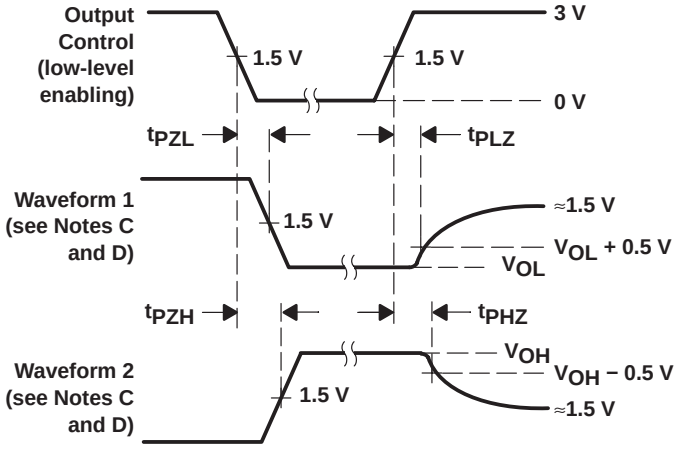

**VOLTAGE WAVEFORMS
PULSE DURATIONS**




**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**




**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**

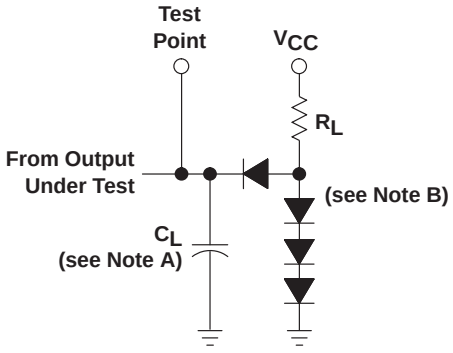



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS**

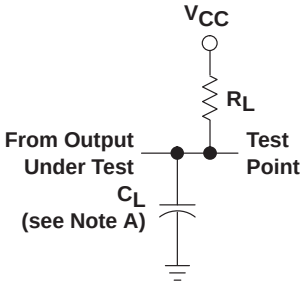
NOTES: A. $C_L$ includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
D. S1 and S2 are closed for $t_{PLH}$, $t_{PHL}$, $t_{PHZ}$, and $t_{PLZ}$; S1 is open and S2 is closed for $t_{PZH}$; S1 is closed and S2 is open for $t_{PZL}$.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\ \Omega$; $t_r$ and $t_f \leq 7$ ns for Series 54/74 devices and $t_r$ and $t_f \leq 2.5$ ns for Series 54S/74S devices.
F. The outputs are measured one at a time, with one input transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

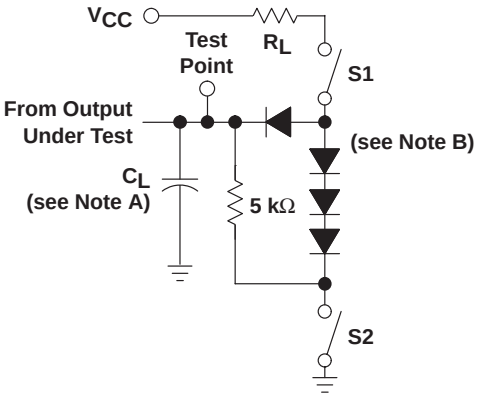
## PARAMETER MEASUREMENT INFORMATION
## SERIES 54LS/74LS DEVICES



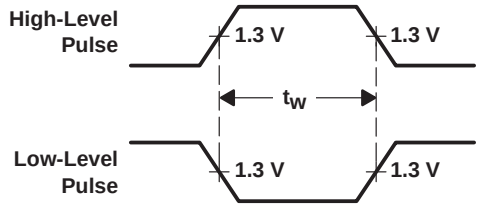

LOAD CIRCUIT
FOR 2-STATE TOTEM-POLE OUTPUTS



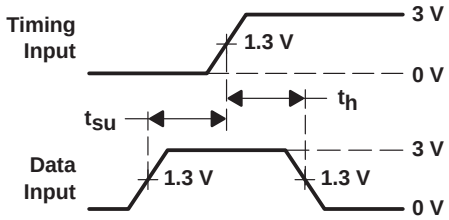

LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



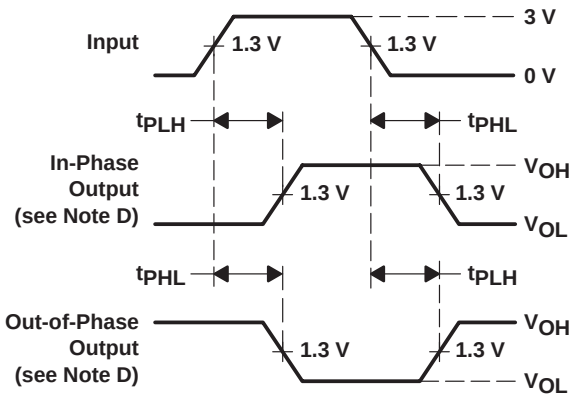

LOAD CIRCUIT
FOR 3-STATE OUTPUTS



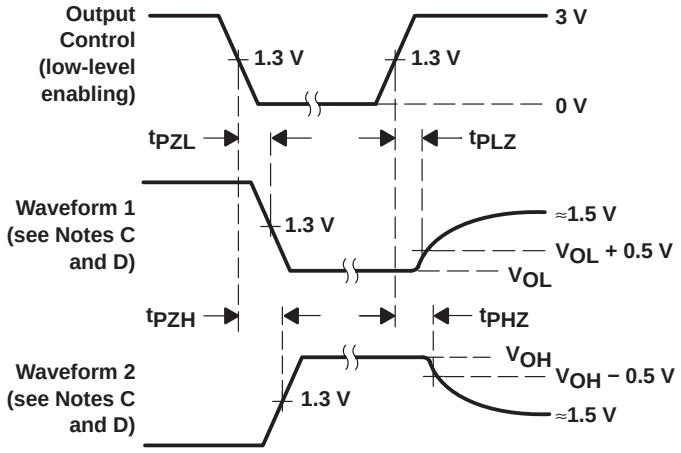

VOLTAGE WAVEFORMS
PULSE DURATIONS




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. $C_L$ includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
D. S1 and S2 are closed for $t_{PLH}$, $t_{PHL}$, $t_{PHZ}$, and $t_{PLZ}$; S1 is open and S2 is closed for $t_{PZH}$; S1 is closed and S2 is open for $t_{PZL}$.
E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\ \Omega$, $t_r \le 1.5$ ns, $t_f \le 2.6$ ns.
G. The outputs are measured one at a time, with one input transition per measurement.

**Figure 2. Load Circuits and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| JM38510/00105BCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 00105BCA | Samples |
| JM38510/00105BDA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 00105BDA | Samples |
| JM38510/07003BCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 07003BCA | Samples |
| JM38510/07003BDA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 07003BDA | Samples |
| JM38510/30003B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/ 30003B2A | Samples |
| JM38510/30003BCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30003BCA | Samples |
| JM38510/30003BDA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30003BDA | Samples |
| JM38510/30003SCA | ACTIVE | CDIP | J | 14 | 25 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30003SCA | Samples |
| JM38510/30003SDA | NRND | CFP | W | 14 | 25 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30003SDA | |
| M38510/00105BCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 00105BCA | Samples |
| M38510/00105BDA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 00105BDA | Samples |
| M38510/07003BCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 07003BCA | Samples |
| M38510/07003BDA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 07003BDA | Samples |
| M38510/30003B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/ 30003B2A | Samples |
| M38510/30003BCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30003BCA | Samples |
| M38510/30003BDA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30003BDA | Samples |
| M38510/30003SCA | ACTIVE | CDIP | J | 14 | 25 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30003SCA | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| M38510/30003SDA | NRND | CFP | W | 14 | 25 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30003SDA | |
| SN5404J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN5404J | Samples |
| SN54LS04J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN54LS04J | Samples |
| SN54S04J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN54S04J | Samples |
| SN7404D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 7404 | Samples |
| SN7404DE4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 7404 | Samples |
| SN7404DG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 7404 | Samples |
| SN7404DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 7404 | Samples |
| SN7404N | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN7404N | Samples |
| SN7404N3 | OBSOLETE | PDIP | N | 14 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN7404NE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN7404N | Samples |
| SN74LS04D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS04 | Samples |
| SN74LS04DBR | ACTIVE | SSOP | DB | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | | LS04 | Samples |
| SN74LS04DG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS04 | Samples |
| SN74LS04DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS04 | Samples |
| SN74LS04DRE4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS04 | Samples |
| SN74LS04DRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS04 | Samples |
| SN74LS04J | OBSOLETE | CDIP | J | 14 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74LS04N | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS04N | Samples |
| SN74LS04N3 | OBSOLETE | PDIP | N | 14 | | TBD | Call TI | Call TI | 0 to 70 | | |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LS04NE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS04N | Samples |
| SN74LS04NSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS04 | Samples |
| SN74LS04NSRG4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS04 | Samples |
| SN74S04D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | S04 | Samples |
| SN74S04DG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | S04 | Samples |
| SN74S04DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | S04 | Samples |
| SN74S04N | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74S04N | Samples |
| SN74S04N3 | OBSOLETE | PDIP | N | 14 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74S04NE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74S04N | Samples |
| SN74S04NSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74S04 | Samples |
| SNJ5404J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ5404J | Samples |
| SNJ5404W | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ5404W | Samples |
| SNJ54LS04FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | SNJ54LS 04FK | Samples |
| SNJ54LS04J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ54LS04J | Samples |
| SNJ54LS04W | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ54LS04W | Samples |
| SNJ54S04FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | SNJ54S 04FK | Samples |
| SNJ54S04J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ54S04J | Samples |
| SNJ54S04W | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ54S04W | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



**OTHER QUALIFIED VERSIONS OF SN5404, SN54LS04, SN54LS04-SP, SN54S04, SN7404, SN74LS04, SN74S04 :**

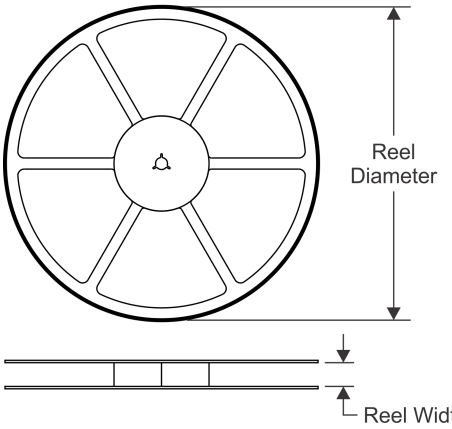
- Catalog: SN7404, SN74LS04, SN54LS04, SN74S04
- Military: SN5404, SN54LS04, SN54S04
- Space: SN54LS04-SP

NOTE: Qualified Version Definitions:

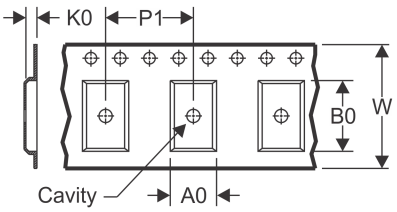
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

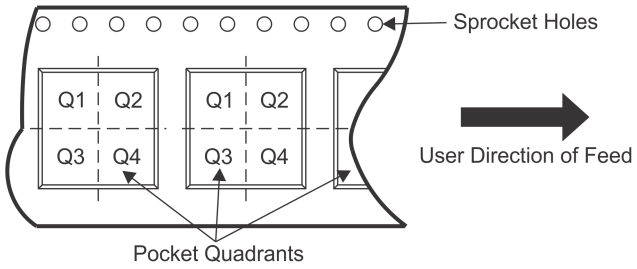



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

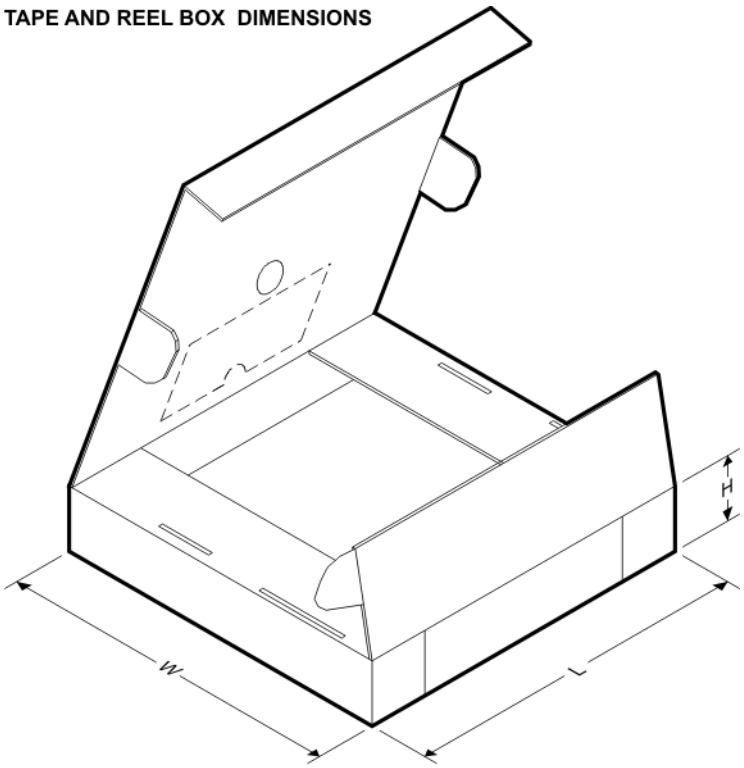
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN7404DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LS04DBR | SSOP | DB | 14 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LS04DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74S04DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74S04NSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



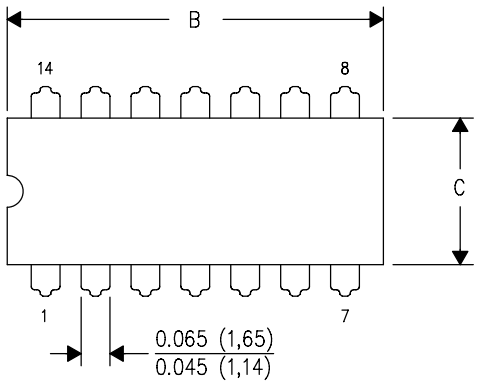

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN7404DR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| SN74LS04DBR | SSOP | DB | 14 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LS04DR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| SN74S04DR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| SN74S04NSR | SO | NS | 14 | 2000 | 367.0 | 367.0 | 38.0 |

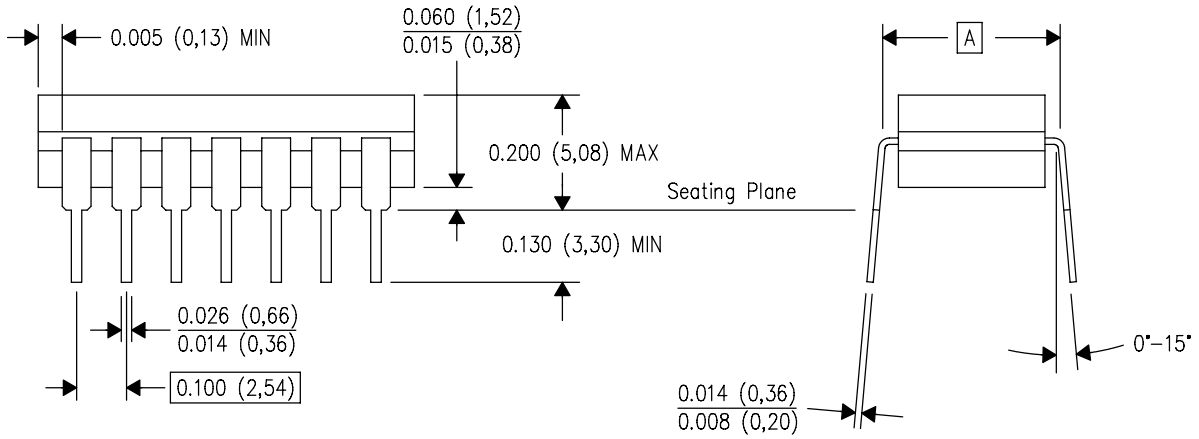
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE



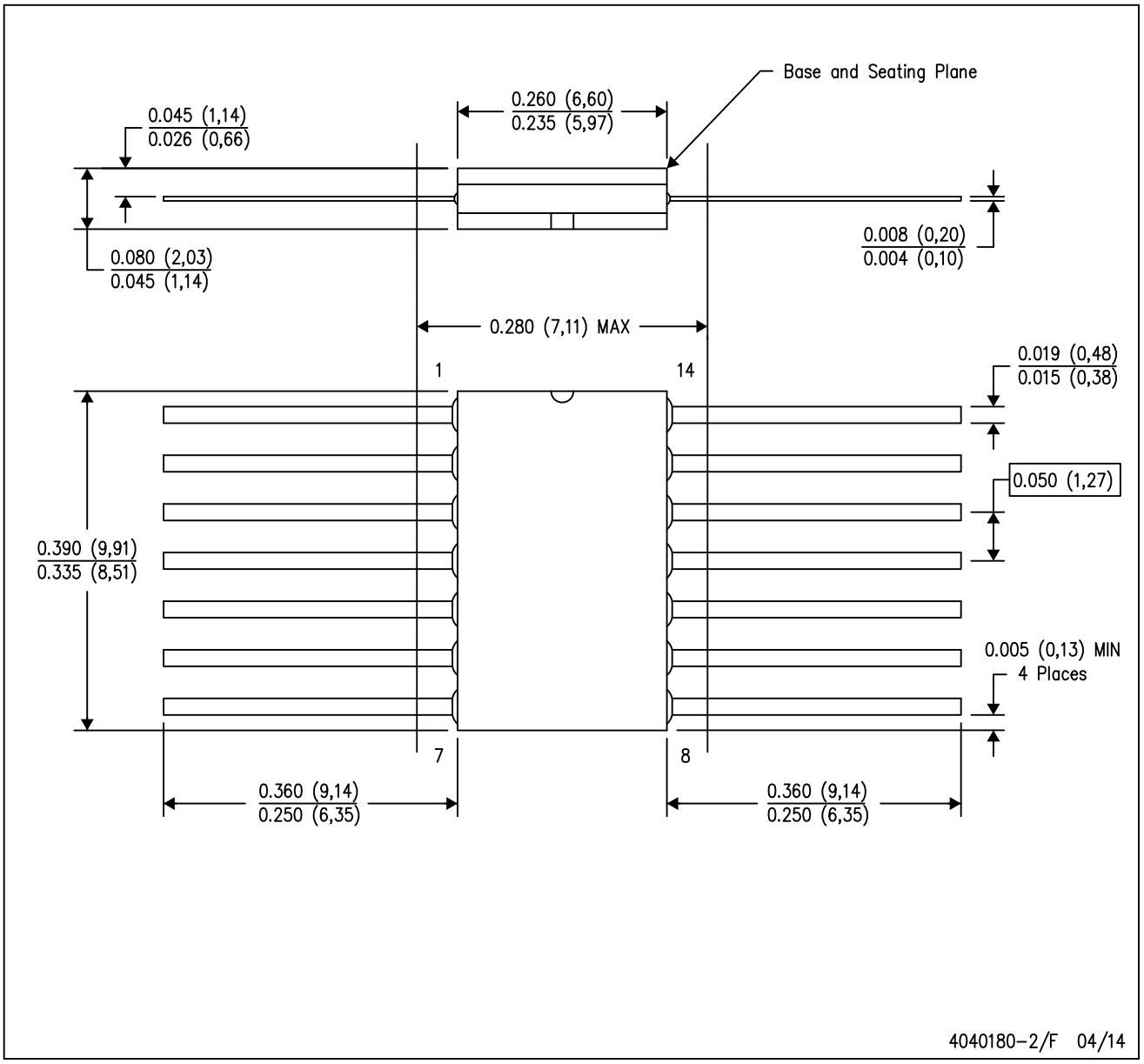

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |




4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

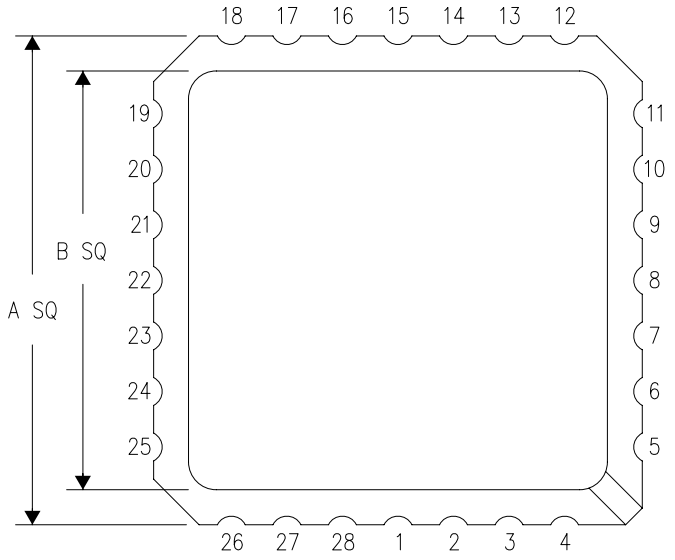
W (R–GDFP–F14) CERAMIC DUAL FLATPACK



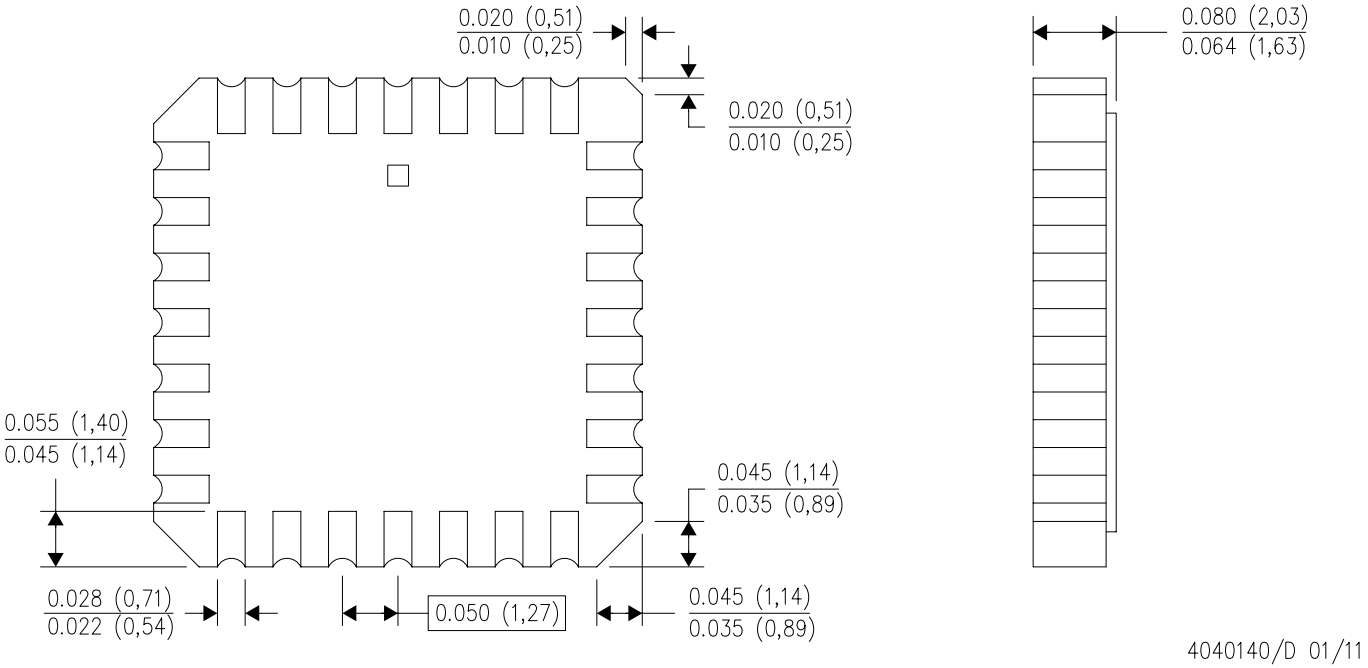

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN




| NO. OF TERMINALS ** | A | | B | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



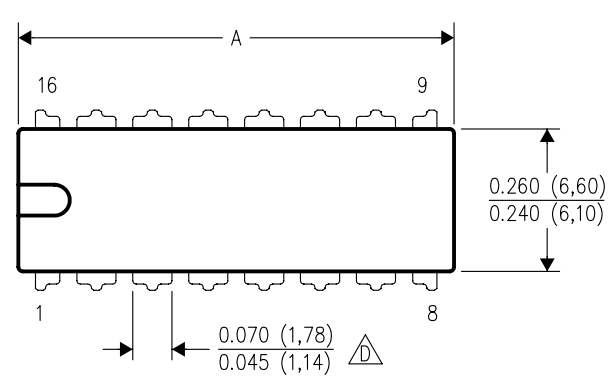

4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

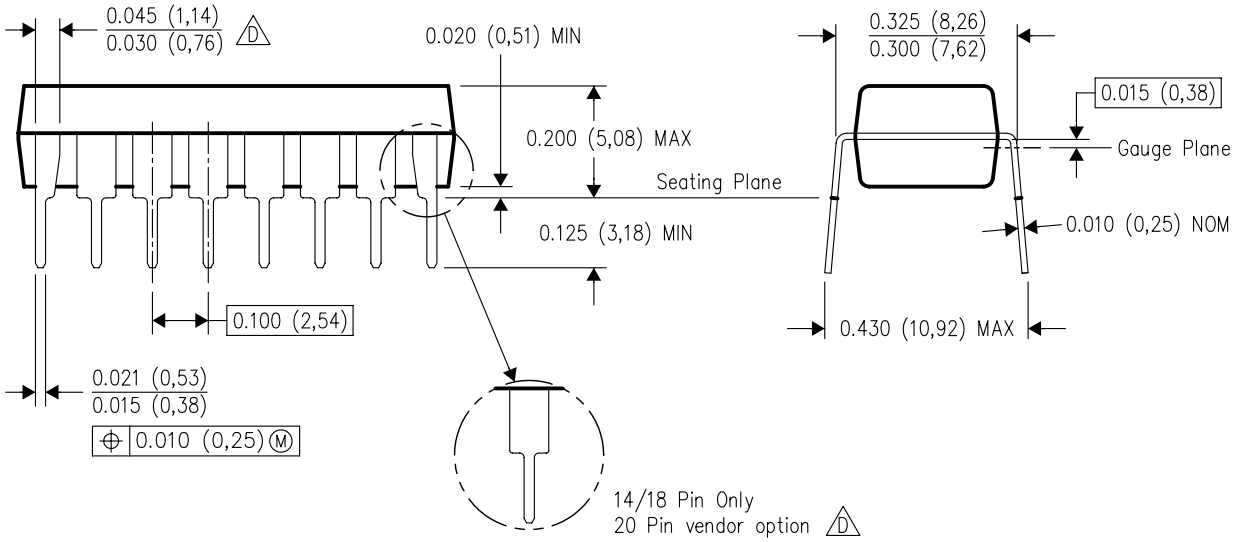
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



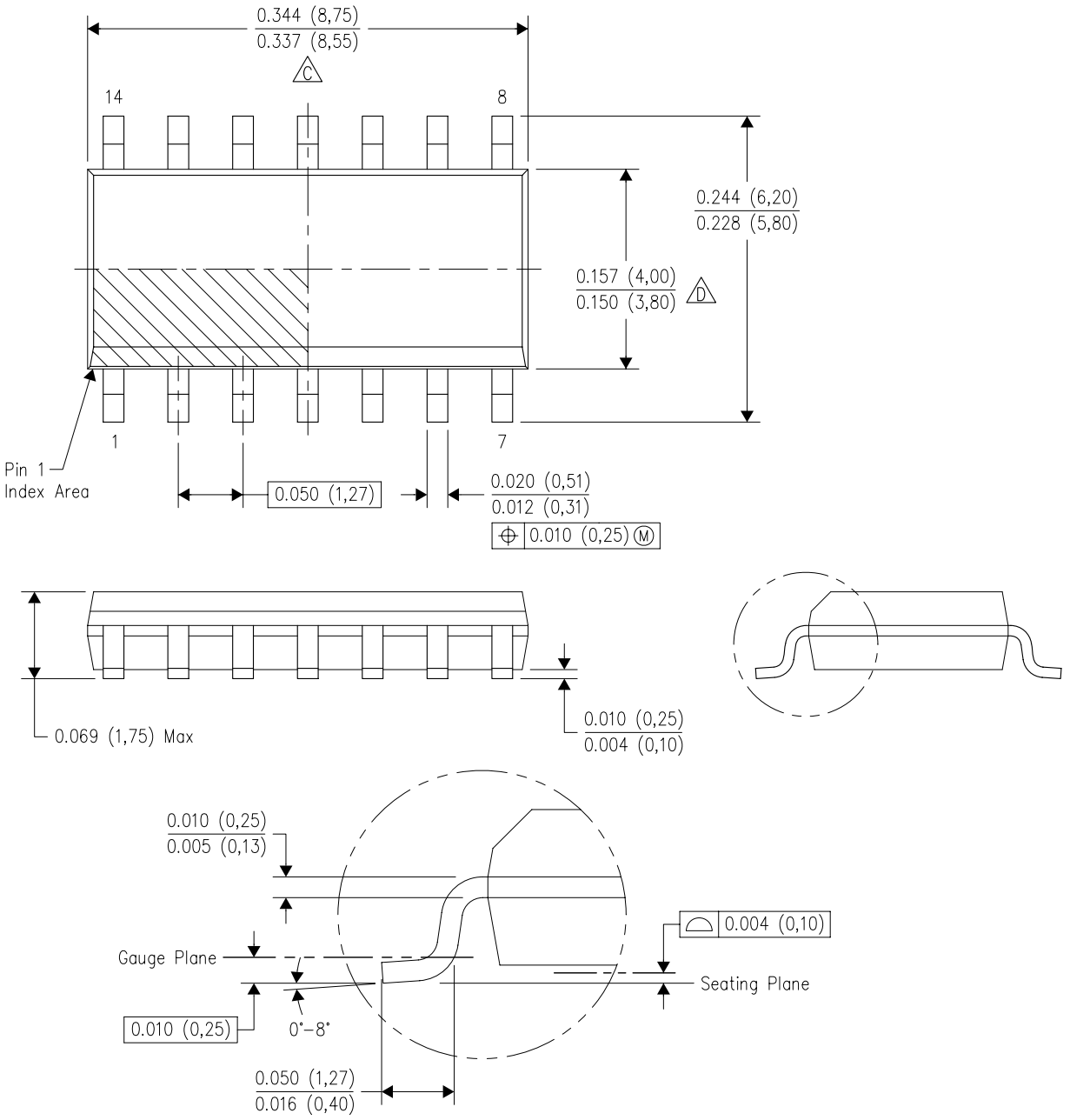

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

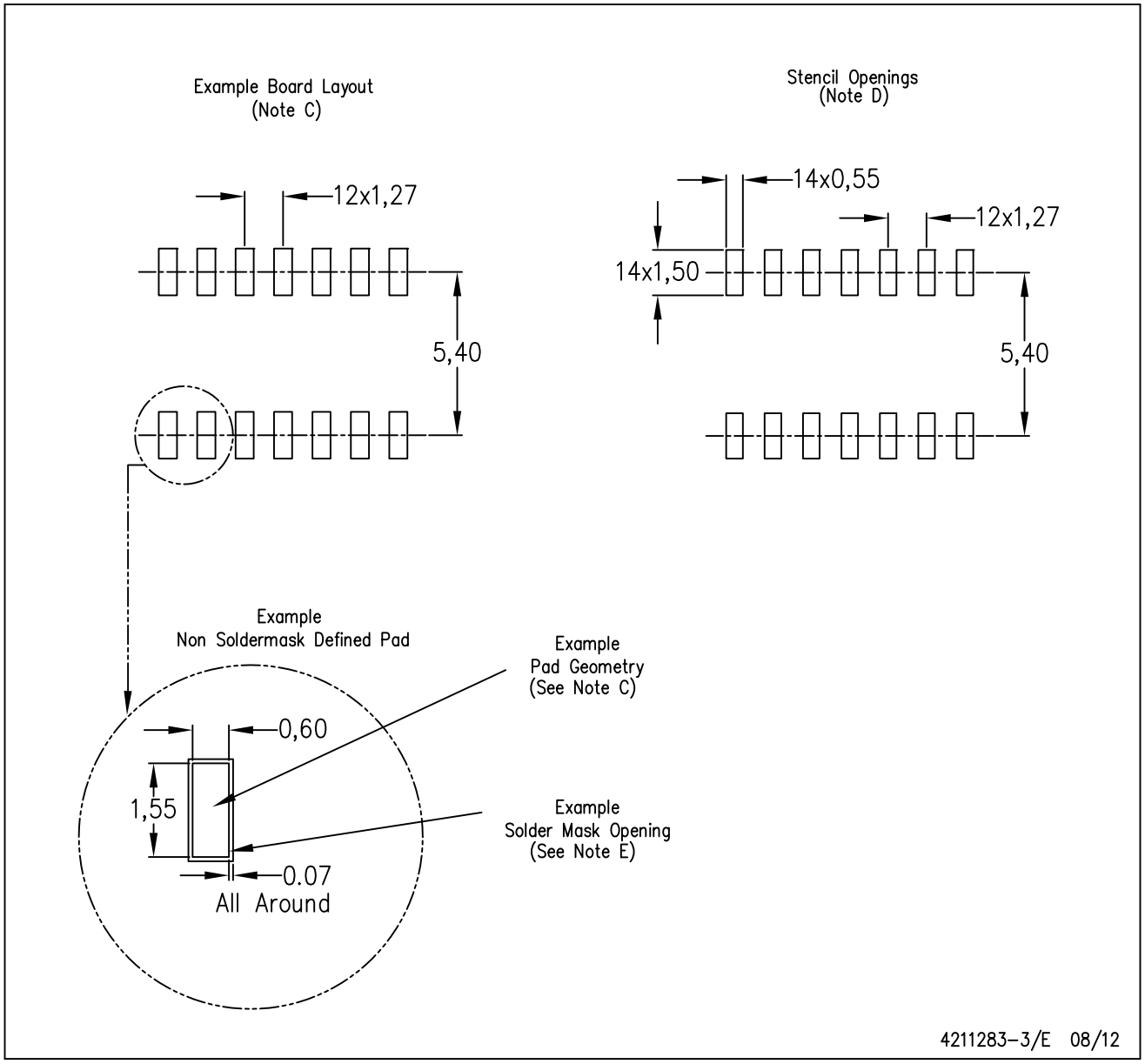
D (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE

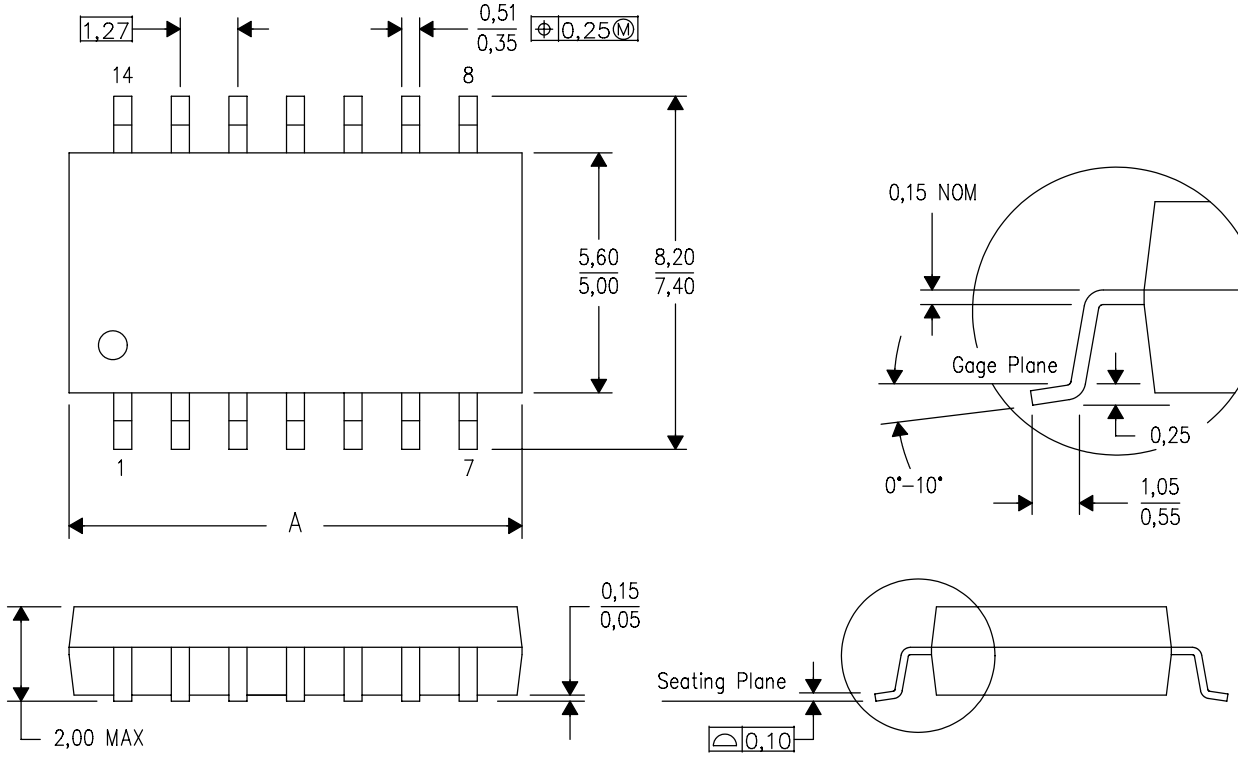



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

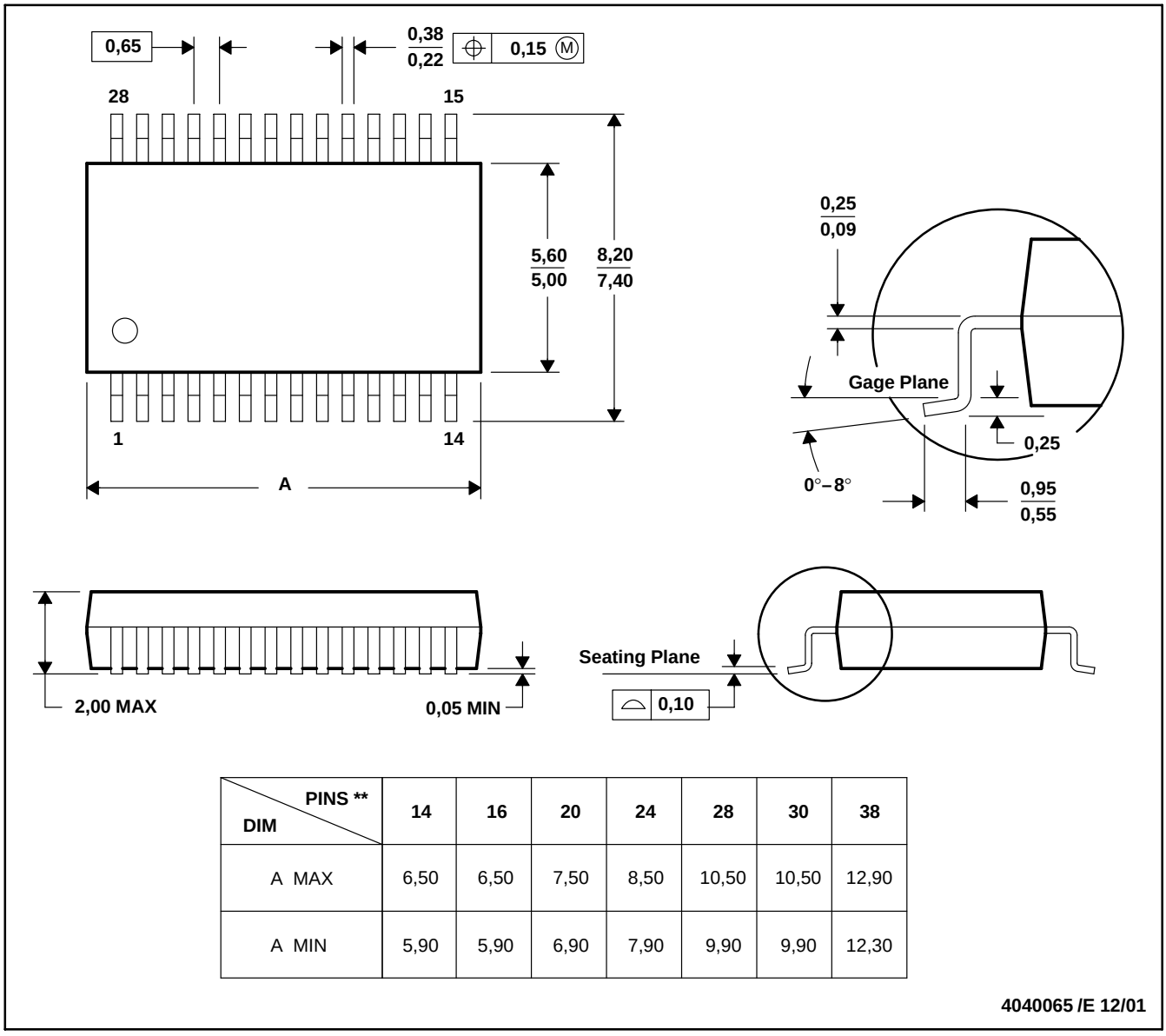
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

**DB (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**28 PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 | 28 | 30 | 38 |
|---|---|---|---|---|---|---|---|
| A MAX | 6,50 | 6,50 | 7,50 | 8,50 | 10,50 | 10,50 | 12,90 |
| A MIN | 5,90 | 5,90 | 6,90 | 7,90 | 9,90 | 9,90 | 12,30 |

**4040065 /E 12/01**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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