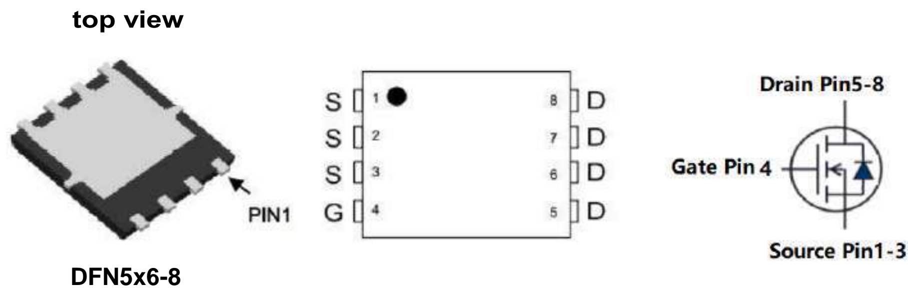
Features

- High ruggedness
- Low Gate Charge (Typ 143nC)
- Improved dv/dt Capability
- 100% Avalanche Tested
- Application:Synchronous Rectification, Li Battery Protect Board, Inverter

Product Summary

V_{DS}	30	V
$R_{DS(on),Typ}$ @ V_{GS}=10 V	1.7	mΩ
I_D	150	A



Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DSS}	Drain to source voltage	30	V
I_D	Continuous drain current (@T_c=25°C)	150*	A
	Continuous drain current (@T_c=100°C)	78*	A
I_{DM}	Drain current pulsed(note 1)	600	A
I_{DSM}	Continuous drain current (@T_a=25°C)	30	A
	Continuous drain current (@T_a=70°C)	24	A
V_{GS}	Gate to source voltage	±20	V
E_{AS}	Single pulsed avalanche energy (note 2)	576	mJ
E_{AR}	Repetitive avalanche energy (note 1)	57	mJ
dv/dt	Peak diode recovery dv/dt (note 3)	5	V/ns
P_D	Total power dissipation (@T_c=25°C)	43	W
	Total power dissipation (@T_a=25°C)	2.6	W
T_{STG}, T_J	Operating junction temperature & storage temperature	-55 ~ + 150	°C

*. Drain current is limited by junction temperature.

Thermal characteristics

Symbol	Parameter	Value	Unit
R_{thjc}	Thermal resistance, Junction to case	1.8	°C/W
R_{thja}	Thermal resistance, Junction to ambient	62	°C/W

Note: R_{thja} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{thjc} is guaranteed by design while R_{thca} is determined by the user's board design.

Electrical characteristic (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Off characteristics						
BV_{DSS}	Drain to source breakdown voltage	V_{GS}=0V, I_D=250uA	30			V
ΔBV_{DSS} / ΔT_J	Breakdown voltage temperature coefficient	I_D=250uA, referenced to 25°C		0.02		V/°C
I_{DSS}	Drain to source leakage current	V_{DS}=30V, V_{GS}=0V			1	uA
		V_{DS}=24V, T_J=125°C			50	uA
I_{GSS}	Gate to source leakage current, forward	V_{GS}=20V, V_{DS}=0V			100	nA
	Gate to source leakage current, reverse	V_{GS}=-20V, V_{DS}=0V			-100	nA
On characteristics						
$V_{GS(TH)}$	Gate threshold voltage	V_{DS}=V_{GS}, I_D=250uA	1.2		2.4	V
$R_{DS(ON)}$	Drain to source on state resistance	V_{GS}=4.5V, I_D=30A,T_J=25°C		3.4	4.5	mΩ
		V_{GS}=10V, I_D=30A,T_J=25°C		1.7	2.5	mΩ
G_{fs}	Forward transconductance	V_{DS}=5V, I_D=30A		73		S
Dynamic characteristics						
C_{iss}	Input capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		6272		pF
C_{oss}	Output capacitance			1022		
C_{rss}	Reverse transfer capacitance			718		
$t_{d(on)}$	Turn on delay time	V_{DS}=15V, I_D=30A, R_G=4.7Ω, V_{GS}=10V (note 4,5)		20		ns
t_r	Rising time			58		
$t_{d(off)}$	Turn off delay time			158		
t_f	Fall time			77		
Q_g	Total gate charge	V_{DS}=24V, V_{GS}=10V, I_D=30A , I_G=5mA (note 4,5)		143		nC
Q_{gs}	Gate-source charge			17		
Q_{gd}	Gate-drain charge			43		
R_g	Gate resistance	V_{DS}=0V, Scan F mode		4.2		Ω

Source to drain diode ratings characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_S	Continuous source current	Integral reverse p-n Junction diode in the MOSFET			150	A
I_{SM}	Pulsed source current				600	A
V_{SD}	Diode forward voltage drop.	I_S=45A, V_{GS}=0V			1.4	V
t_{rr}	Reverse recovery time	I_S=30A, V_{GS}=0V, dI_F/dt=100A/us		26		ns
Q_{rr}	Reverse recovery charge			10		nC

※. Notes

1. Repeatitive rating : pulse width limited by junction temperature.
2. L =0.5mH, I_{AS} =48A, V_{DD}=30V, R_G=25Ω, Starting T_J = 25°C
3. I_{SD} ≤30A, di/dt = 100A/us, V_{DD} ≤ BV_{DSS}, Staring T_J =25°C
4. Pulse Test : Pulse Width ≤ 300us, duty cycle ≤ 2%.
5. Essentially independent of operating temperature.

Fig. 1. On-state characteristics

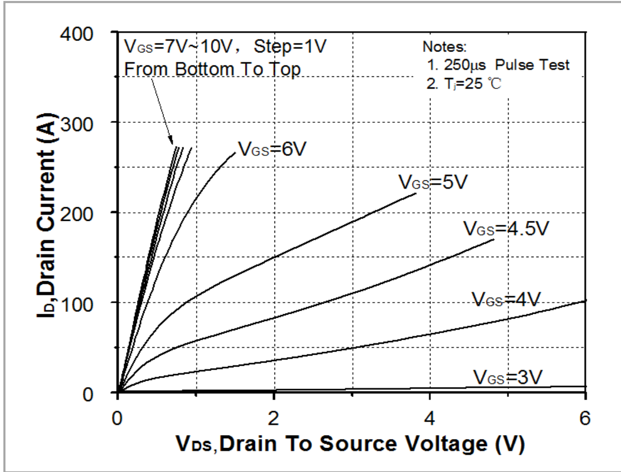


Fig. 2. Transfer Characteristics

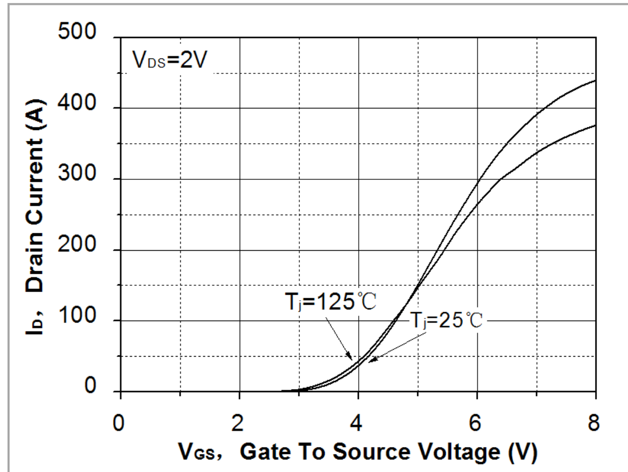


Fig. 3. On-resistance variation vs. drain current and gate voltage

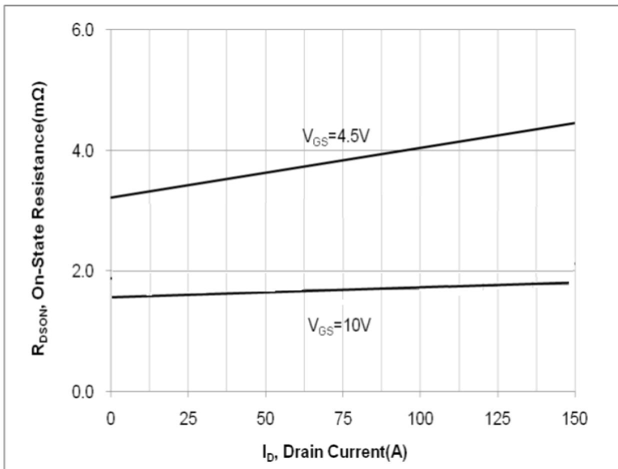


Fig. 4. On-state current vs. diode forward voltage

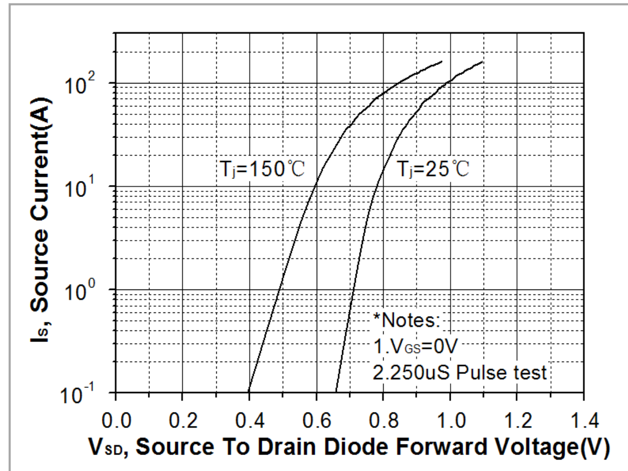


Fig 5. Breakdown voltage variation vs. junction temperature

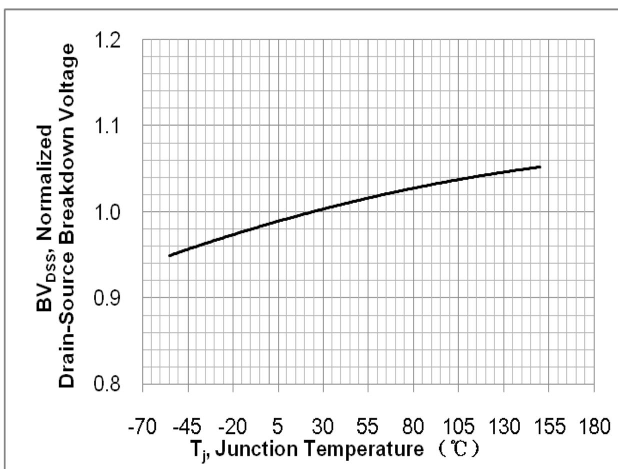


Fig. 6. On-resistance variation vs. junction temperature

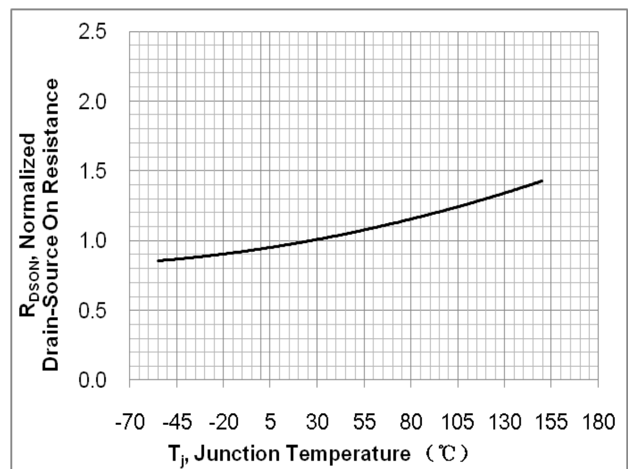


Fig. 7. Gate charge characteristics

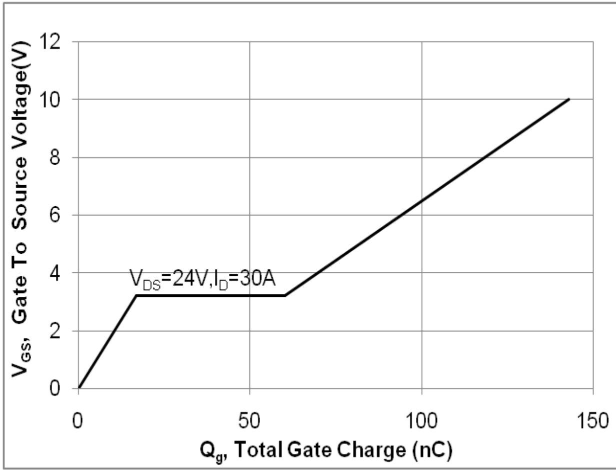


Fig. 8. Capacitance Characteristics

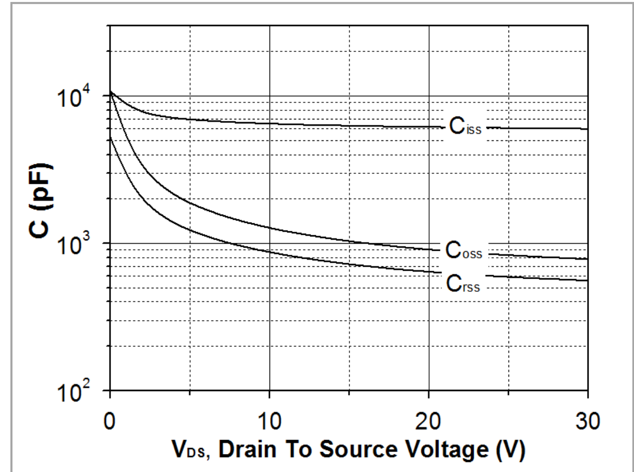


Fig. 9. Maximum safe operating area

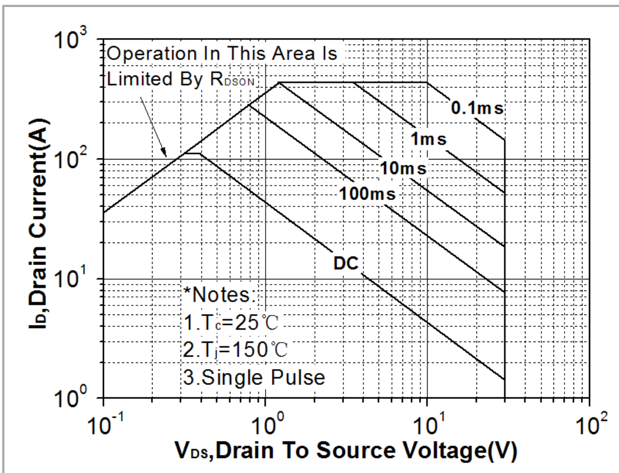


Fig. 10. Maximum drain current vs. case temperature

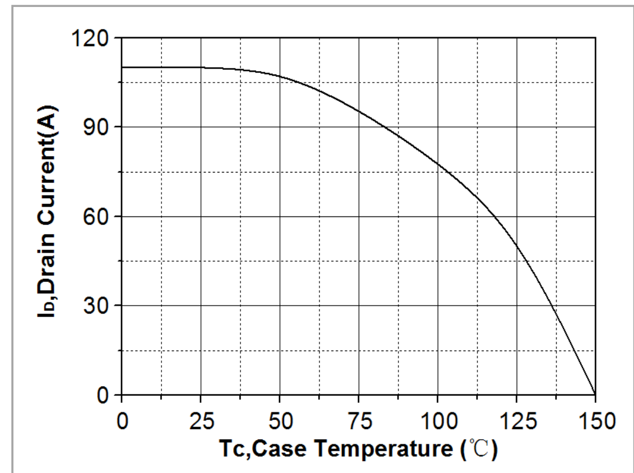


Fig. 11. Transient thermal response curve

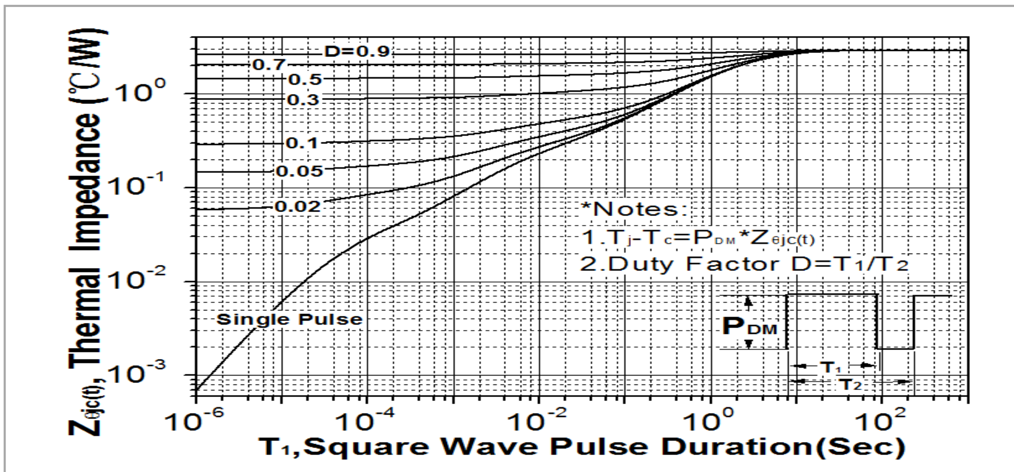


Fig. 12. Gate charge test circuit & waveform

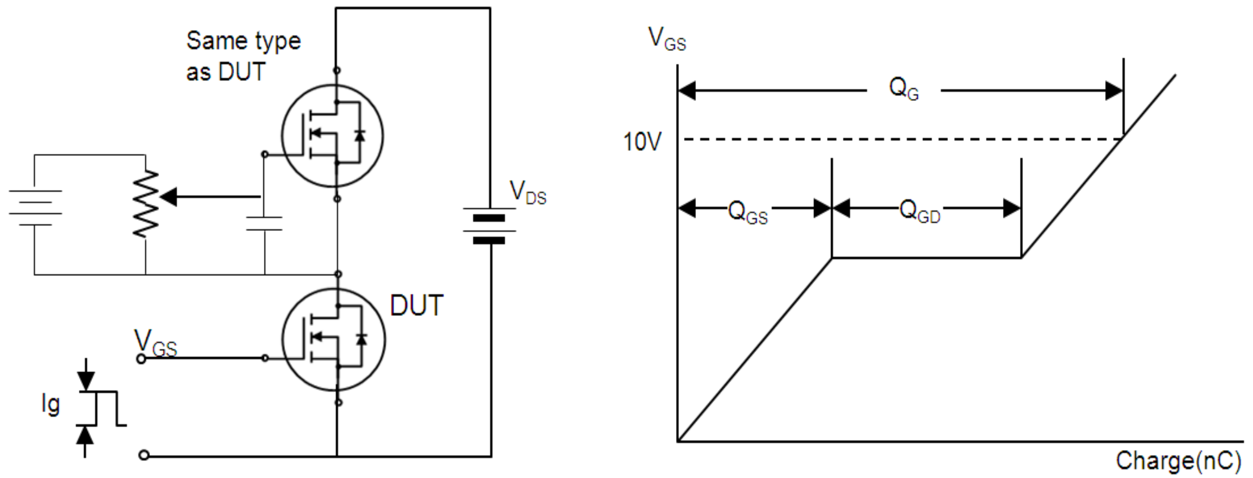


Fig. 13. Switching time test circuit & waveform

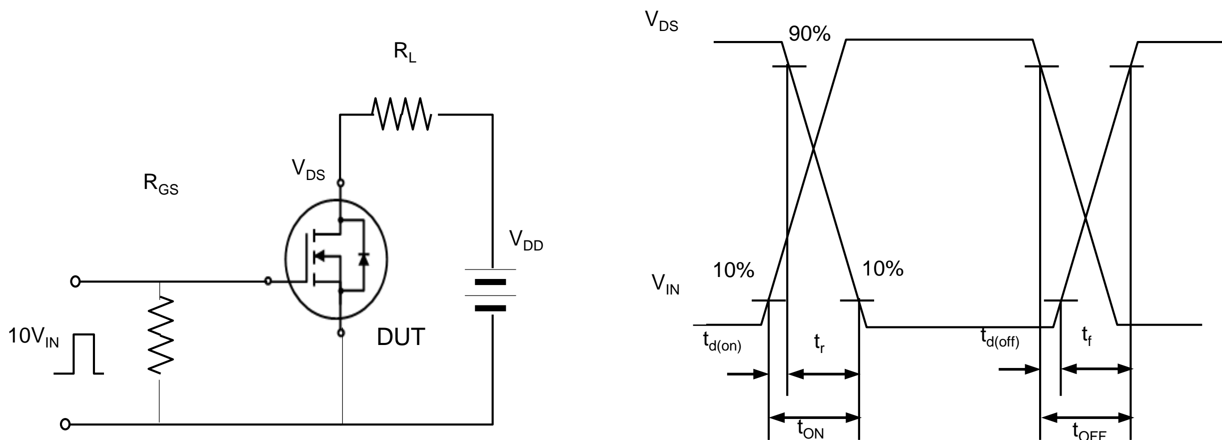


Fig. 14. Unclamped Inductive switching test circuit & waveform

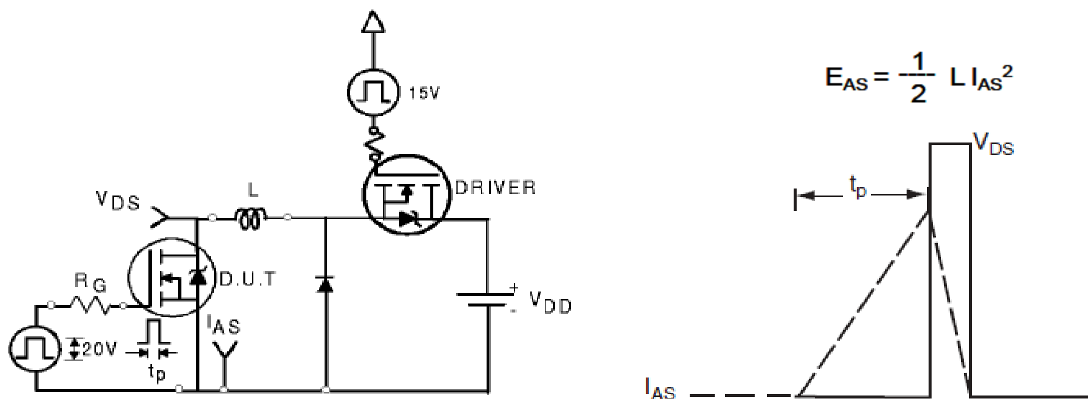
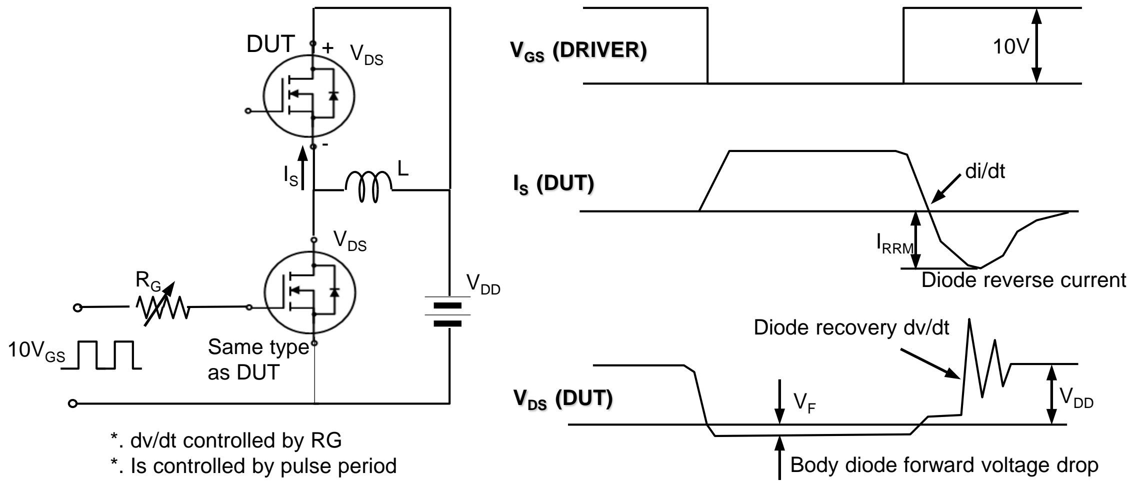
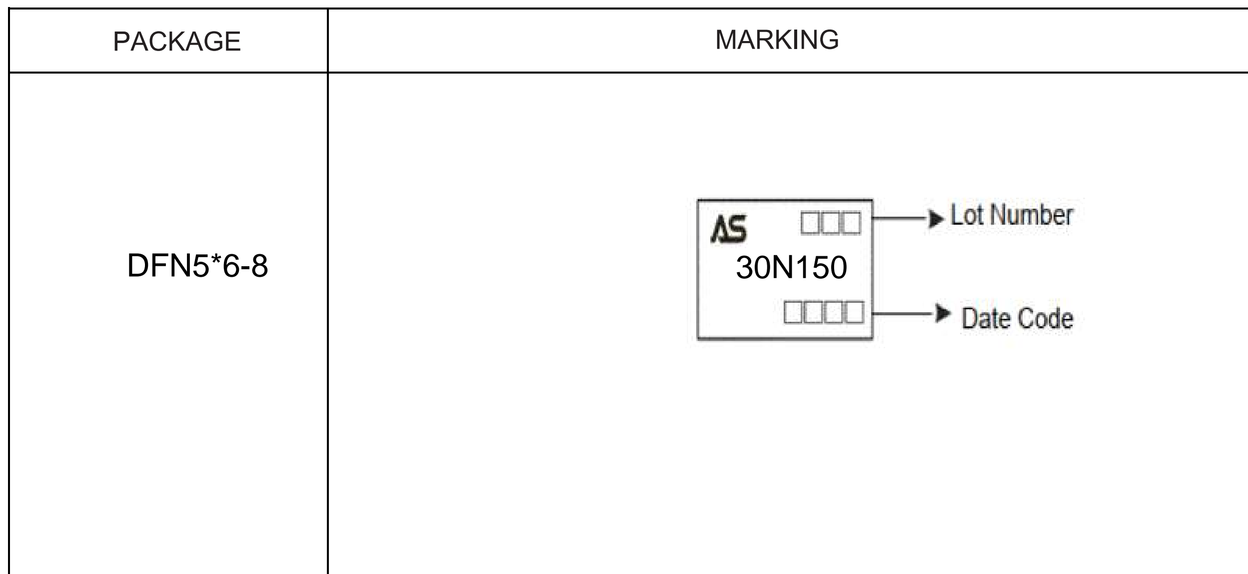


Fig. 15. Peak diode recovery dv/dt test circuit & waveform

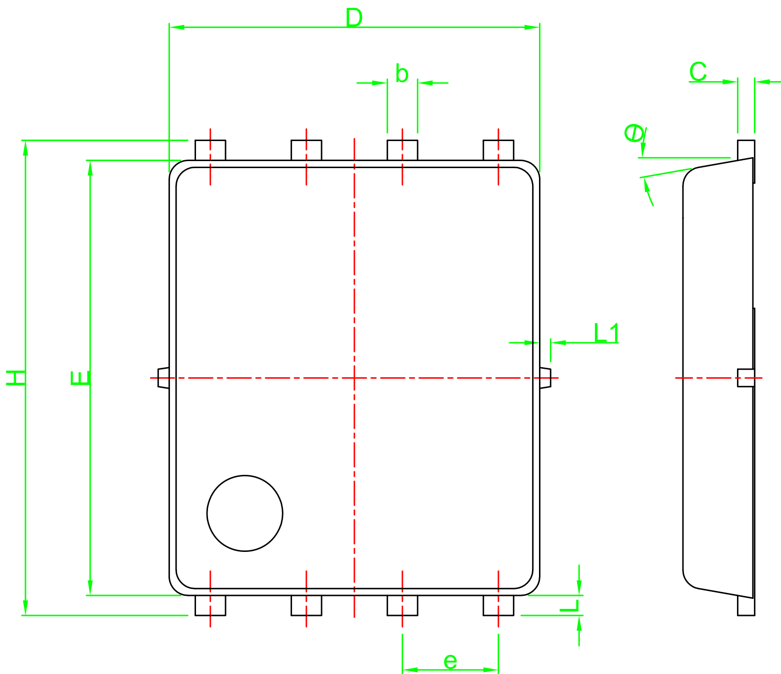


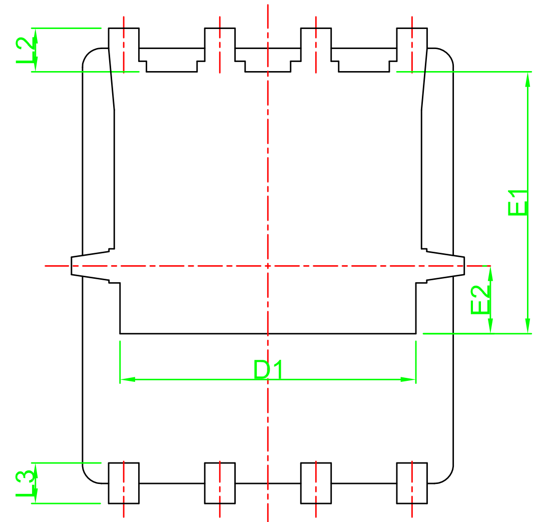
Ordering and Marking Information

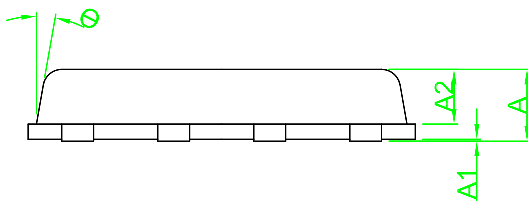
Ordering Device No.	Marking	Package	Packing	Quantity
ASDM30N150Q-R	30N150	DFN5*6-8	Tape&Reel	4000/Reel

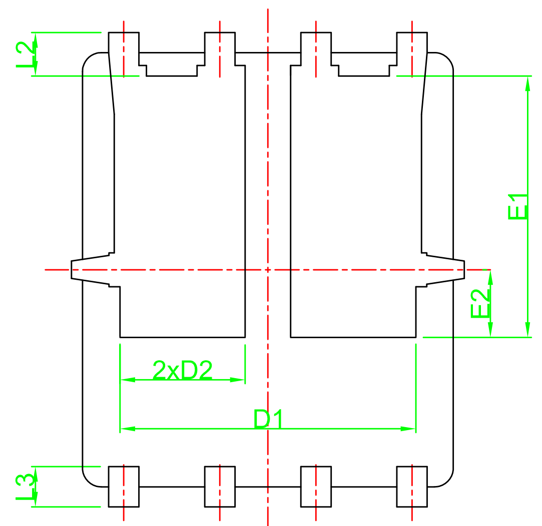


PACKAGE	MARKING
DFN5*6-8	









DFN5*6-8

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	0.85	1.00	0.033	0.039
A1	0.01	0.05	0.000	0.002
A2	0.69	0.75	0.027	0.030
b	0.40	0.45	0.016	0.018
C	0.20	0.30	0.008	0.012
D	4.80	4.95	0.189	0.195
D1	3.91	4.06	0.154	0.160
D2	1.60	1.80	0.063	0.071
e	1.27 TYP		0.05 TYP	
E	5.65	5.80	0.222	0.228
E1	3.46	3.50	0.136	0.138
E2	0.80	0.95	0.031	0.037
L	0.15	0.3	0.006	0.012
L1	0.08	0.15	0.003	0.006
L2	0.58	0.73	0.023	0.029
L3	0.45	0.60	0.018	0.024
H	6.15	6.28	0.242	0.247
Θ	8°	12°	8°	12°

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