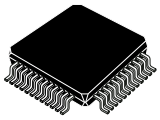
L9679E

Datasheet

Automotive battery cut-off circuit and airbag system expansion IC



TQFP48 exposed pad down (7x7x1 mm)

Product status link
L9679E

Product summary	
Order code	**L9679E**
Package	TQFP48 exp. pad (7x7x1.0 mm)
Packing	Tray
Order code	**L9679ETR**
Package	TQFP48 exp. pad (7x7x1.0 mm)
Packing	Tape and Reel

Features

- AEC-Q100 qualified
- Squib/Pyroswitch deployment drivers
  - 8-channel HSD/LSD
  - 25 V maximum deployment voltage
  - Various deployment profiles
  - Current monitoring Rmeasure, STB, STG and leakage diagnostics
  - High- and low-side driver FET tests
- Four-channel remote sensor interface
  - PSI-5 satellite sensors
  - Configurable asynchronous/synchronous protocols
- Configurable arming input signals
- Temperature sensor
- 32-bit SPI communications
  - 2 SPI buses (1 global, 1 for satellite communication)
  - Parity bit
- Integrated ADC measurements (1 ADC converter)
- Operating temperature: -40 °C to 105 °C
- Package - 48 pins

Applications

- Airbag systems
- Cut-off battery systems
- Pyro Fuse/Pyroswitch management

Description

The L9679E is an extension chip in airbag systems or a pyroswitch manager. This device is family-compatible with the L9679 and L9680 devices. The device includes an octal driver for squib/pyroswitch deployments and a quad channel interface for PSI-5 sensors. Deployment profiles can be set according to user specifications via SPI configuration, as well as the protocol to be used to communicate with the satellite sensors. Independent configurable arming inputs are provided for a programmable mapping of the loops to be deployed.

1 Absolute maximum ratings

This part may be irreparably damaged if taken outside the specified Absolute Maximum Ratings. Operation above the Absolute Maximum Ratings may also cause a decrease in reliability.

The operating junction temperature range is -40 °C to +150 °C. The maximum junction temperature must not be exceeded except when in deployment and within the deploy power stages. Deployment is possible starting with a junction temperature of 150 °C.

Table 1. Absolute maximim ratings

Pin name	Pin function	Min	Max	Unit
SR4	Squib/Pyroswitch 4 low-side pin	-0.3	35	V
SF4	Squib/Pyroswitch 4 high-side pin	-1.0	40	V
SG45	Squib/Pyroswitch 4 & 5 ground pin	-0.3	0.3	V
SS45	Squib/Pyroswitch 4 & 5 deployment supply pin	-0.3	40	V
SF5	Squib/Pyroswitch 5 high-side pin	-1.0	40	V
SR5	Squib/Pyroswitch 5 low-side pin	-0.3	35	V
SR0	Squib/Pyroswitch 0 low-side pin	-0.3	35	V
SF0	Squib/Pyroswitch 0 high-side pin	-1.0	40	V
SG01	Squib/Pyroswitch 0 & 1 ground pin	-0.3	0.3	V
SS01	Squib/Pyroswitch 0 & 1 deployment supply pin	-0.3	40	V
SF1	Squib/Pyroswitch 1 high-side pin	-1.0	40	V
SR1	Squib/Pyroswitch 1 low-side pin	-0.3	35	V
RSU0	PSI-5 ch. 0 remote sensor output	-1	40	V
RSU1	PSI-5 ch. 1 remote sensor output	-1	40	V
VSAT	SAT input voltage	-0.3	40	V
VSYNC	SYNC input voltage	-0.3	40	V
GNDA	Analog ground	-0.3	0.3	V
FEN1	Arming input 1	-0.3	VCC+0.3 ≤ 6.5	V
FEN2	Arming input 2	-0.3	VCC+0.3 ≤ 6.5	V
SATSYNC	Initiate Satellite Sensor Sync Pulse	-0.3	VCC+0.3 ≤ 6.5	V
RESET_N	Reset input	-0.3	VCC+0.3 ≤ 6.5	V
TEST	Test mode input pin	-0.3	20	V
RSU2	PSI-5 ch. 2 remote sensor output	-1	40	V
RSU3	PSI-5 ch. 3 remote sensor output	-1	40	V
SR3	Squib/Pyroswitch 3 low-side pin	-0.3	35	V
SF3	Squib/Pyroswitch 3 high-side pin	-1.0	40	V
SS23	Squib/Pyroswitch 2 & 3 deployment supply pin	-0.3	40	V
SG23	Squib/Pyroswitch 2 & 3 ground pin	-0.3	0.3	V
SF2	Squib/Pyroswitch 2 high-side pin	-1.0	40	V
SR2	Squib/Pyroswitch 2 low-side pin	-0.3	35	V
SR7	Squib/Pyroswitch 7 low-side pin	-0.3	35	V
SF7	Squib/Pyroswitch 7 high-side pin	-1.0	40	V
SS67	Squib/Pyroswitch 6 & 7 deployment supply pin	-0.3	40	V
SG67	Squib/Pyroswitch 6 & 7 ground pin	-0.3	0.3	V
SF6	Squib/Pyroswitch 6 high-side pin	-1.0	40	V
SR6	Squib/Pyroswitch 6 low-side pin	-0.3	35	V
CVDD	Internal 3.3V regulator output	-0.3	4.6	V
GNDD	Digital ground	-0.3	0.3	V
FENL	LS driver FET arming input	-0.3	VCC+0.3 ≤ 6.5	V
SCLK_RS	Remote SPI interface clock	-0.3	VCC+0.3 ≤ 6.5	V

Pin name	Pin function	Min	Max	Unit
CS_RS	Remote SPI interface chip select	-0.3	VCC+0.3 ≤ 6.5	V
MOSI_RS	Remote SPI interface data in	-0.3	VCC+0.3 ≤ 6.5	V
MISO_RS	Remote SPI interface data out	-0.3	VCC+0.3 ≤ 6.5	V
VCC	VCC voltage supply	-0.3	6.5	V
MISO_G	Global SPI interface data out	-0.3	VCC+0.3 ≤ 6.5	V
MOSI_G	Global SPI interface data in	-0.3	VCC+0.3 ≤ 6.5	V
SCLK_G	Global SPI interface clock	-0.3	VCC+0.3 ≤ 6.5	V
CS_G	Global SPI interface chip select	-0.3	VCC+0.3 ≤ 6.5	V
Exposed Pad Down	Substrate ground - Squib/Pyroswitch ground	-0.3	0.3	V

Table 2. ESD robustness

Symbol	Parameter	Test conditions	Min	Unit
HBM	HBM Human Body Model from Q100-002	All pins	±2000	V
HBM	HBM Human Body Model from Q100-002	Only for pins RSUx[x=0...3], SFx[x=0...7], SRx[x=0...7].	±4000	V
CDM	CDM Charged Device Model from Q100-011	All pins	±500	V
CDM	CDM Charged Device Model from Q100-011	Corner pins	±750	V

Table 3. Temperature ranges and thermal resistances

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
T_{amb}	Operating ambient temperature		-40	-	105	°C
T_j	Junction temperature		-40	-	150	°C
$R_{Th\ j\text{-}case}$	Thermal resistance junction-to-case	Bottom cold plate in contact with package bottom case (e-pad side). JESD51 best practice guidelines.	-	2.5	-	°C/W
$R_{Th\ j\text{-}amb}$	Thermal resistance junction-to-ambient	With 2s2p PCB std Jedec. Natural convection. Standard Jedec best JESD51-7	-	30	-	°C/W

2 Operative maximum ratings

Within the operating ratings the part operates as specified and without parameter deviations. Once taken beyond the operative ratings and returned back within, the part will recover with no damage or degradation.

Additional supply voltage and temperature conditions are given separately at the beginning of each specification table.

Table 4. **Operative maximum ratings**

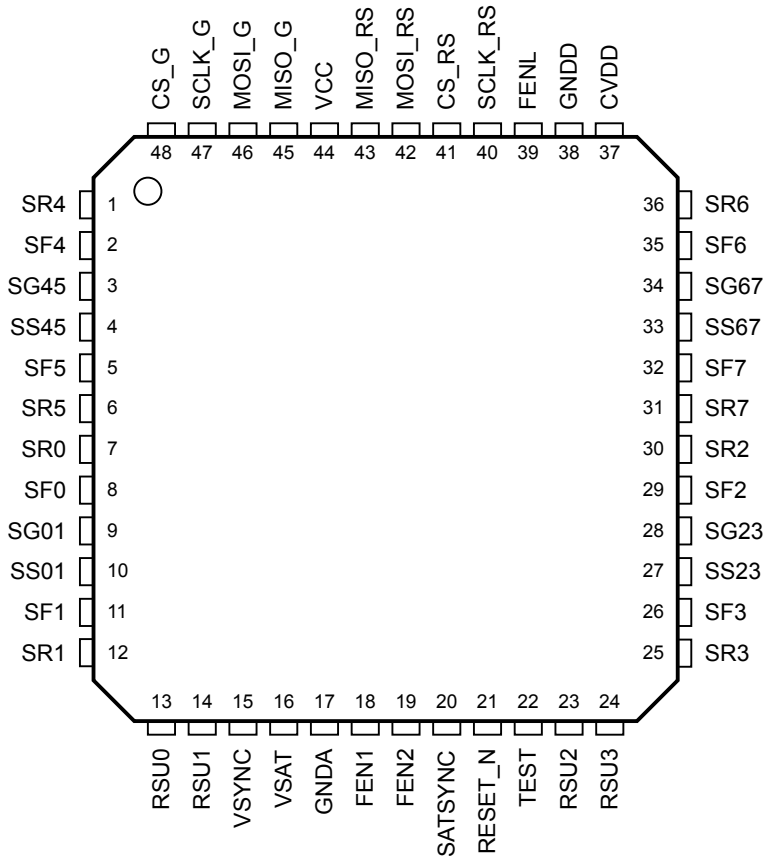
Pin name	Pin function	Min	Max	Unit
SR4	Squib/Pyroswitch 4 low-side pin	-0.1	SS45	V
SF4	Squib/Pyroswitch 4 high-side pin	-1.0	SS45	V
SG45	Squib/Pyroswitch 4 & 5 ground pin	-0.1	0.1	V
SS45	Squib/Pyroswitch 4 & 5 deployment supply pin	-0.1	35	V
SF5	Squib/Pyroswitch 5 high-side pin	-1.0	SS45	V
SR5	Squib/Pyroswitch 5 low-side pin	-0.1	SS45	V
SR0	Squib/Pyroswitch 0 low-side pin	-0.1	SS01	V
SF0	Squib/Pyroswitch 0 high-side pin	-1.0	SS01	V
SG01	Squib/Pyroswitch 0 & 1 ground pin	-0.1	+0.1	V
SS01	Squib/Pyroswitch 0 & 1 deployment supply pin	-0.1	35	V
SF1	Squib/Pyroswitch 1 high-side pin	-1.0	SS01	V
SR1	Squib/Pyroswitch 1 low-side pin	-0.1	SS01	V
RSU0	PSI-5 ch. 0 remote sensor output	-1	VRSU_SYNC_MAX	V
RSU1	PSI-5 ch. 1 remote sensor output	-1	VRSU_SYNC_MAX	V
VSAT	SAT input voltage	-0.1	10	V
VSYNC	SYNC input voltage	-0.1	35	V
GNDA	Analog ground	-0.1	0.1	V
FEN1	Arming input 1	-0.1	VCC+0.1 ≤ 5.5	V
FEN2	Arming input 2	-0.1	VCC+0.1 ≤ 5.5	V
SATSYNC	Initiate Satellite Sensor Sync Pulse	-0.1	VCC+0.1 ≤ 5.5	V
RESET_N	Reset input	-0.1	VCC+0.1 ≤ 5.5	V
TEST	Test mode input pin	-0.1	15	V
RSU2	PSI-5 ch. 2 remote sensor output	-1	VRSU_SYNC_MAX	V
RSU3	PSI-5 ch. 3 remote sensor output	-1	VRSU_SYNC_MAX	V
SR3	Squib/Pyroswitch 3 low-side pin	-0.1	SS23	V
SF3	Squib/Pyroswitch 3 high-side pin	-1.0	SS23	V
SS23	Squib/Pyroswitch 2 & 3 deployment supply pin	-0.1	35	V
SG23	Squib/Pyroswitch 2 & 3 ground pin	-0.1	+0.1	V
SF2	Squib/Pyroswitch 2 high-side pin	-1.0	SS23	V
SR2	Squib/Pyroswitch 2 low-side pin	-0.1	SS23	V
SR7	Squib/Pyroswitch 7 low-side pin	-0.1	SS67	V
SF7	Squib/Pyroswitch 7 high-side pin	-1.0	SS67	V
SS67	Squib/Pyroswitch 6 & 7 deployment supply pin	-0.1	35	V
SG67	Squib/Pyroswitch 6 & 7 ground pin	-0.1	+0.1	V
SF6	Squib/Pyroswitch 6 high-side pin	-1.0	SS67	V
SR6	Squib/Pyroswitch 6 low-side pin	-0.1	SS67	V
CVDD	Internal 3.3V regulator output	-0.1	3.6	V
GNDD	Digital ground	-0.1	0.1	V
FENL	LS driver FET arming input	-0.1	VCC+0.1 ≤ 5.5	V
SCLK_RS	Remote SPI interface clock	-0.1	VCC+0.1 ≤ 5.5	V

Pin name	Pin function	Min	Max	Unit
CS_RS	Remote SPI interface chip select	-0.1	VCC+0.1 ≤ 5.5	V
MOSI_RS	Remote SPI interface data in	-0.1	VCC+0.1 ≤ 5.5	V
MISO_RS	Remote SPI interface data out	-0.1	VCC+0.1 ≤ 5.5	V
VCC	VCC voltage supply	-0.1	5.5	V
MISO_G	Global SPI interface data out	-0.1	VCC+0.1 ≤ 5.5	V
MOSI_G	Global SPI interface data in	-0.1	VCC+0.1 ≤ 5.5	V
SCLK_G	Global SPI interface clock	-0.1	VCC+0.1 ≤ 5.5	V
CS_G	Global SPI interface chip select	-0.1	VCC+0.1 ≤ 5.5	V
Exposed Pad Down	Substrate ground - Squib/Pyroswitch ground	-0.1	0.1	V

3 Pins description

The L9679E pinout is shown below. The IC is housed in a 48-pin package (7 x 7 x 1.0 mm) with 5x5 mm exposed pad down.

Figure 1. Pinout diagram (top view)



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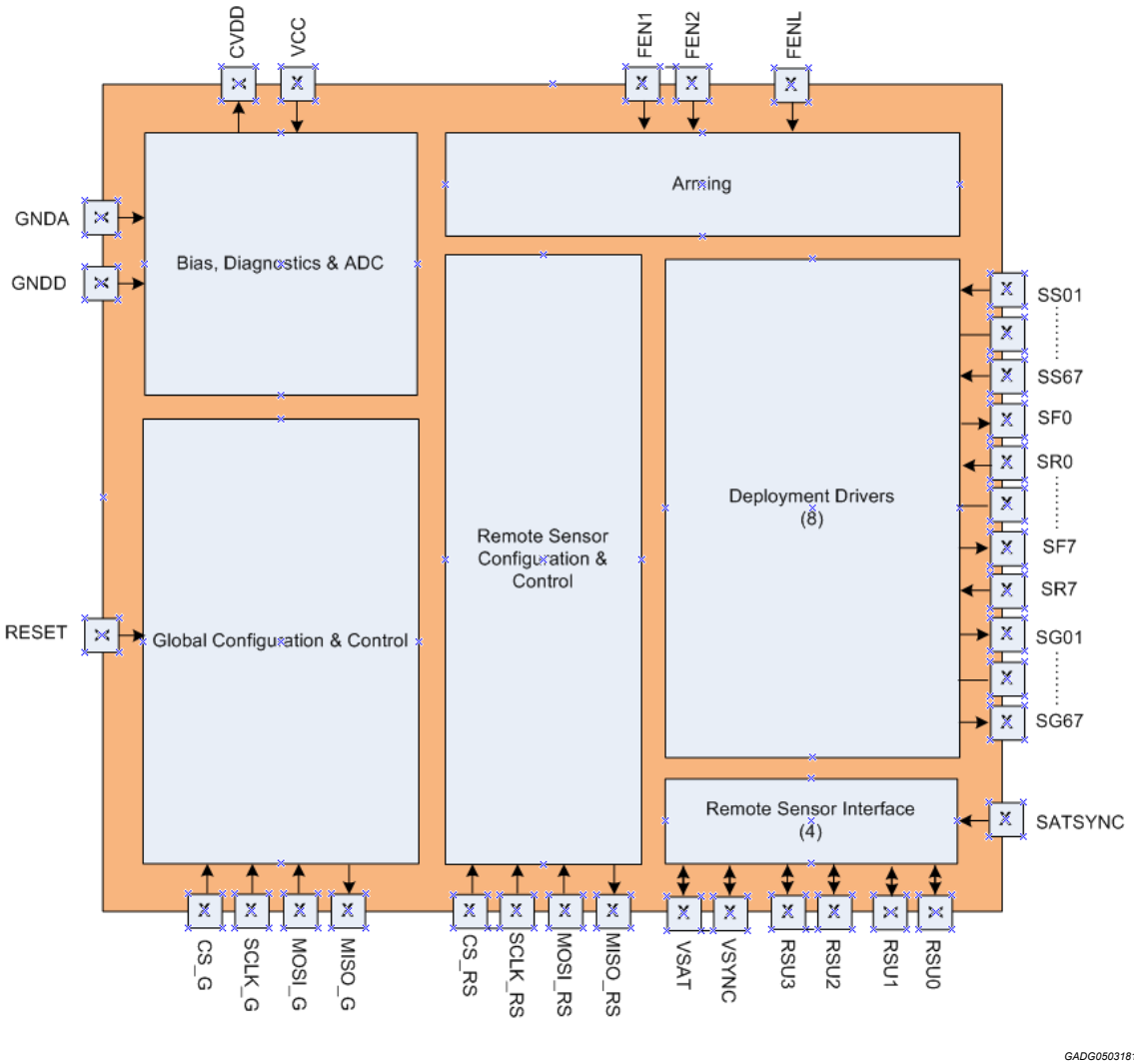
4 Overview and block diagram

The L9679E IC is an application-specific standard component for airbag systems and pyroswitch management. Its main functions include deployment drivers, remote sensor interfaces (PSI-5 satellite sensors) and diagnostics. A block diagram for this IC is shown here in Figure 2. Functional block diagram.

Figure 2. Functional block diagram



4.1 Deployment drivers

- 8 high-side deployment drivers, 8 low-side deployment drivers
- User-programmable deployment options
  - 1.20 A or 1.75 A minimum
  - Programmable time in 64us increments
- Capability to deploy a squib/pyroswitch with a minimum current of 1.2 / 1.75 A and the low-side FET shorted to ground up to 25 V on SSxy
- Independently controlled high-side and low-side FETs
- Squib/Pyroswitch resistance measurement
- Firing current monitor feature
- High- and low-side FET tests
- Open and shorts diagnostics, including between loop drivers
- Independent fire enable logic, SPI and discrete digital input

4.2 Remote sensor interfaces

- Four-channel receiver
  - standard PSI-5 v1.3 compatible with asynchronous and synchronous protocols
- Current limit with shortcircuit protection diagnostics
- PSI-5 satellite sensor mode
  - Auto-adjusting current trip points for each satellite channel
  - Even parity, 8- or 10-bit messages, 125 k or 189 kbps
  - Satellite message error detection

4.3 Arming logic

- Three discrete and independent input arming signals

4.4 Other features

- One dedicated 32-bit SPI bus for global configuration and control
- One dedicated 32-bit SPI bus for remote sensor configuration and control
- Temperature sensor
- Independent thermal shutdown protection on the remote sensor interfaces
- All diagnostics are digital and are available through SPI communications
- Configurable digital I/O pin voltage range, 5 V or 3.3 V

5 Start-up and power control

5.1 Power supply overview

The L9679E IC contains an integrated power management system able to provide all necessary voltages for internal functionality. External supplies are required to operate squib/pyroswitch drivers and RSU interfaces. The power supply block contains the following features:

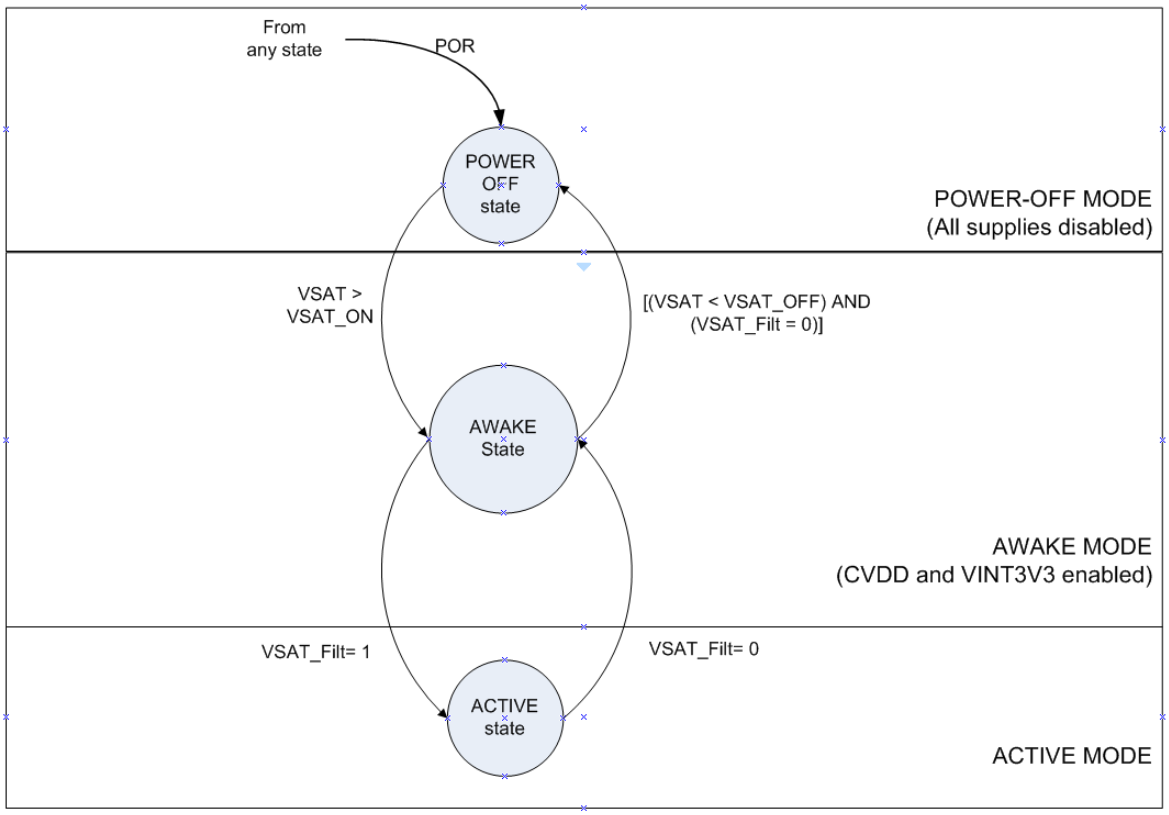
- Two 3.3 V internal regulators for operating internal logic (CVDD) and analog circuits (VINT3V3). An external CVDD pin is used to provide filtering capacitance to digital section supply rail. VSAT is the supply of these two regulators. They are enabled when VSAT voltage goes above VSAT_ON threshold.
- Sync pulse supply (VSYNC) input rail ensures a minimum voltage for operating the satellite sync signal and running part of the squib/pyroswitch diagnostics set. At system level, it can be connected to the SYNCBOOST output rail generated by L9679 or L9680 devices.
- The VSAT input rail ensures the supply to operate the satellite interface. At system level, it can be connected to the SATBUCK output rail generated by L9679 or L9680 devices.
- The VCC input rail ensure the supply to operate the SPI interface, in particular the VCC rail is used only to supply the MISO_G and MISO_RS output digital buffers.

5.2 Power mode control

Start-up and power down of the L9679E are controlled by the VCC pin, VSYNC pin, VSAT pin, RESET_N pin and device status.

There are three main power modes: power-off, awake and active mode. Each power mode is described below and represented in the state flow diagram shown in the following figure.

Figure 3. Power control state flow diagram



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5.2.1 Power-off mode

During the Power-off mode all supplies are disabled keeping the system in a quiescent state with very low current draw from battery. As soon as VSAT>VSAT_ON the IC will move to Awake Mode.

5.2.2 Awake mode

During the Awake mode the VINT3V3 and CVDD internal regulators are turned on and once internal POR is released and RESET_N pin is pulled high, the IC is ready for full activation of all the functionalities.

5.2.3 Active mode

When POR has been released and if VSAT stays above VSAT_ON threshold at least for $T_{VSATFILT}$ the device enters Active mode.

In this state the internal regulators are not immediately switched off in case VSAT goes below VSAT_OFF threshold. It's necessary that VSAT stays below VSAT_OFF for at least $T_{VSATFILT}$ to disable internal regulators.This filter time is present to avoid that glitch on VSAT supply can switch off the device. Anyway it must be considered that, if VSAT goes down and output voltage of internal regulators cannot be sustained, the POR signal will be asserted and the device is immediately switched off.

5.2.4 Power-up and power-down sequences

The typical behaviour of the IC during normal power-up and power-down is shown in Figure 4. Normal power-up sequence and Figure 5. Normal power-down sequence.

It's not required that the following sequence is applied. VSAT is the main supply of the device. VSYNC and VCC supplies can be provided before or after VSAT and are necessary to guarantee the full functionality of the device.

Figure 4. **Normal power-up sequence**

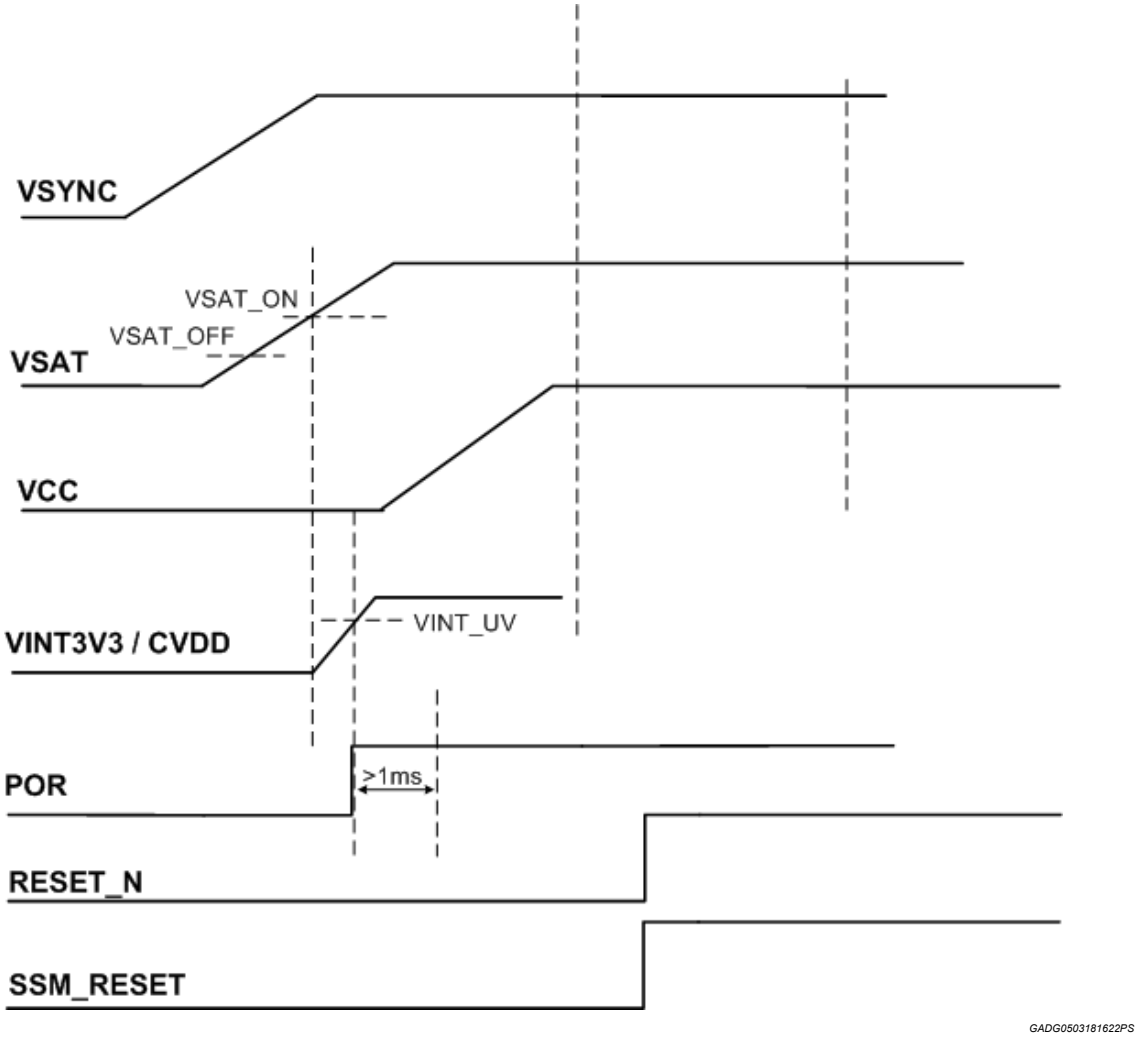
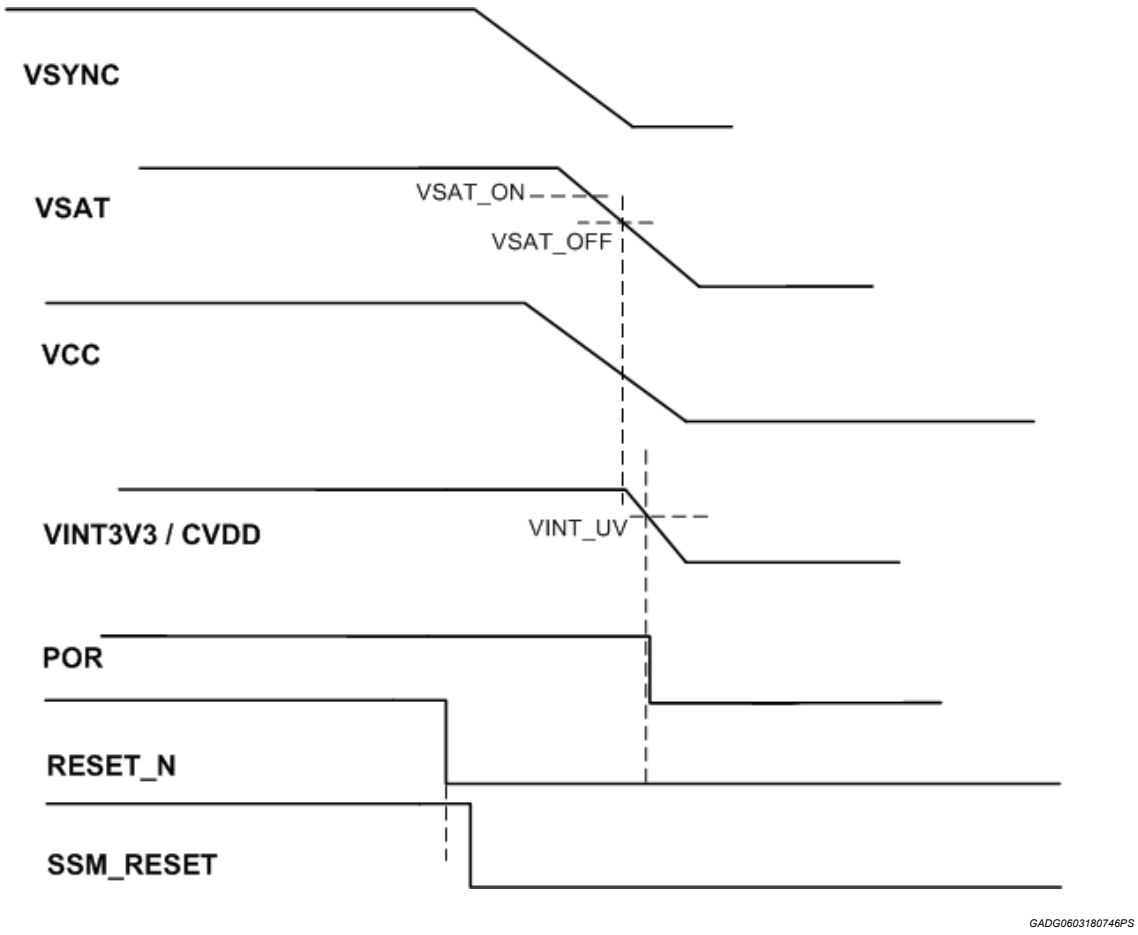


Figure 5. **Normal power-down sequence**



5.2.5 IC operating states

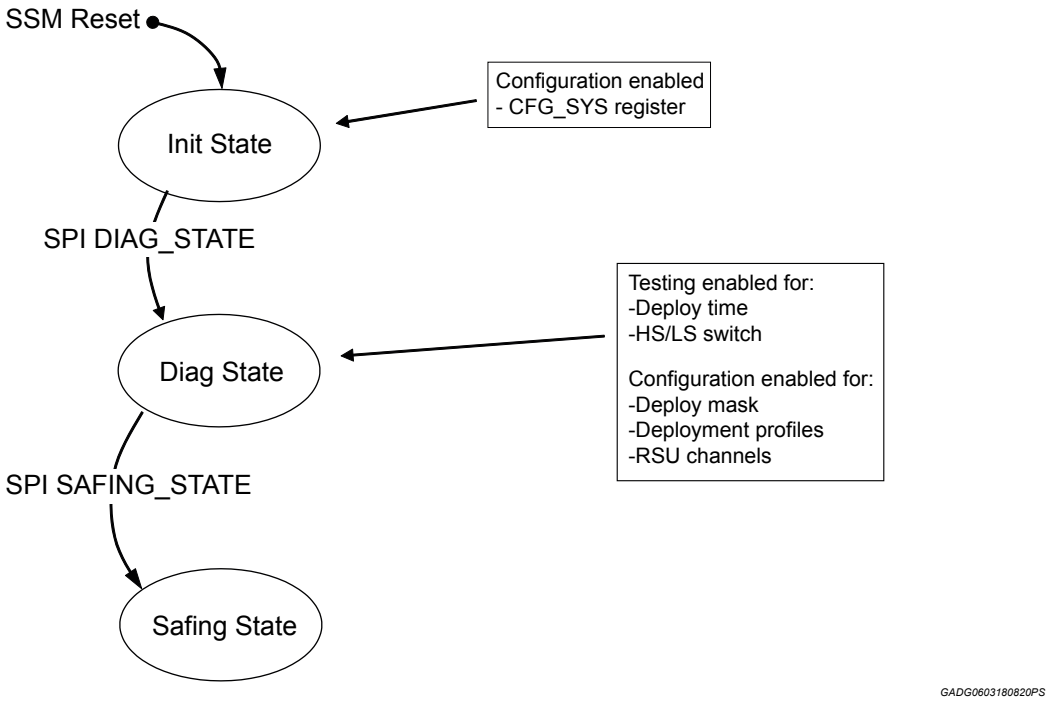
Different states can be identified while operating the device. These states allow safe and predictable initialization, test and operation of the part.

As soon as the RESET signal is de-asserted, L9679E enters the Init state: during this state the device must be initialized by the controller. In particular, the SYS_CFG register can be programmed only during this state.

Upon the DIAG_STATE SPI command, the device switches to Diag state for diagnostics purposes. The remaining configuration of the device is allowed in this state, in particular the RSU channels and deployment profiles. Several tests are also enabled while being in this state and all these tests are mutually exclusive to one another. HS and LS switch tests of the squib/pyroswitch drivers can only be processed during this Diag state. When not in Diag state, any commands for squib/pyroswitch driver switch tests will be ignored. Checks for the configured firing time configuration through the FENL pin are also performed. The SSM remains in this state until commanded to transition into the Safing state via the dedicated SPI commands.

Upon reception of the SAFING_STATE command while in Diag state, the device enters the Safing state. This is the primary run-time state for normal operation, the only state where deployment is permitted. The only means of exiting Safing state is by the assertion of the SSM_Reset signal.The device operating states are shown in Figure 6. IC operating state diagram.

Figure 6. **IC operating state diagram**



5.3 Oscillators

The device integrates two trimmed oscillators, both of them with spread spectrum capability selectable via the CLK_CNF register.

The main oscillator runs at 16 MHz typ and is used to provide clock to the internal synchronous logic.

The auxiliary oscillator runs at 7.5 MHz typ. and is used to monitor the main oscillator. In case the main oscillator frequency is lower than the minimum threshold, this condition is detected by the frequency monitor circuit and latched into the CLKFRERR flag in the FLTSR register. Eventually a POR would be issued. If the clock error is temporary, it is possible to read the fault flag once out of POR.

5.4 Reset control

The device provides an input RESET pin, used to reset the internal logic to safe control system operation in case of internal ECU failures, and a soft reset SPI command.

A low-level signal on this input pin longer than $T_{FLT\_RESET\_N}$ deglitch filter, or the soft reset SPI command reception, will produce the following changes on the IC:

- Clearing of all internal logic registers to the default state
- IC operating state going back to the Init State (see Figure 6. IC operating state diagram)
- Running diagnostics being disabled
- RSU channels being switched off and their data registers being reset to default state
- Running deployments being interrupted.

The RESET pin input circuitry implements a deglitch filter to reject spurious transitions on the signal.

Moreover, the device implements an internal power on reset (POR) producing the same changes at IC level as the RESET pin. This POR is triggered by:

- GDN loss
- BG error
- Internal supply error

The cause of the RESET activation is latched and reported into the fault status register FLTSR and cleared upon SPI reading. During the RESET event the logic is under reset but the FLTSR is not reset. So the fault info will be available as soon as the IC will be out of reset.

Figure 7. **Internal voltage monitors**

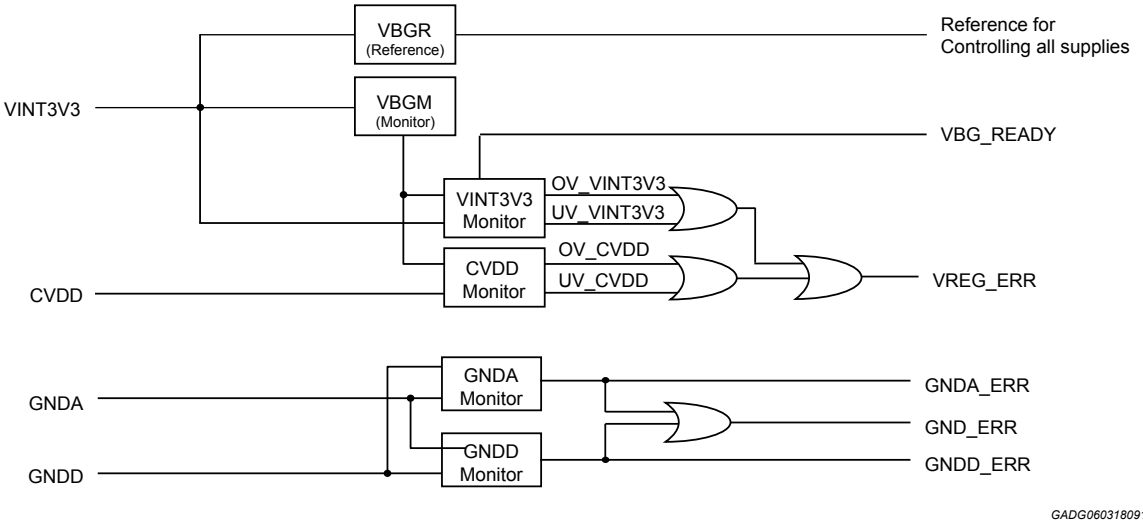
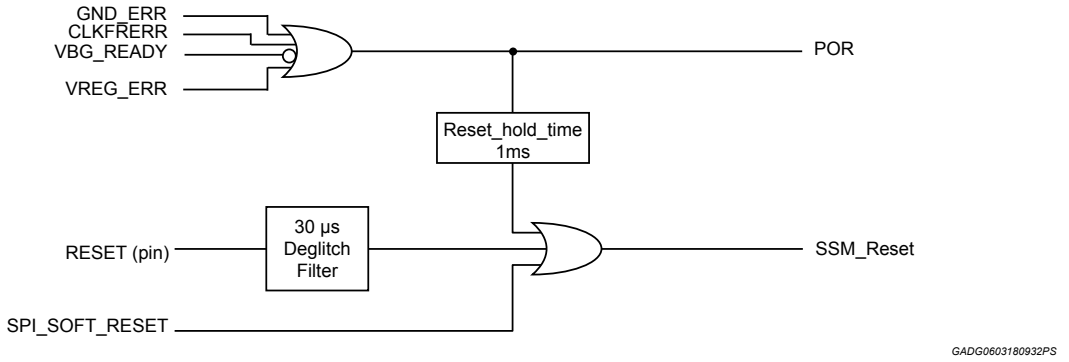


Figure 8. **Reset control logic**



6 SPI interface

The L9679E has many user-selectable features controlled through serial communications by the integrated microcontroller. The device features two SPI interfaces: one global SPI and one remote sensor SPI. The global SPI interface provides general configuration, control and status functions for the device, while the remote sensor SPI provides dedicated communication of the remote sensor data and status registers to the microcontroller.

6.1 SPI protocol

Each SPI interface (global and remote sensor) uses its own dedicated set of 4 I/O pins: CS_G, SCLK_G, MOSI_G and MISO_G for Global SPI; CS_RS, SCLK_RS, MOSI_RS and MISO_RS for remote sensor SPI. Both of the SPI interfaces use the same protocol described here below (the suffix "_X" used in the SPI pin names below is intended to stand for either "_G" or "_RS" depending on the specific SPI interface considered)

The IC SPI interface is composed by an input shift register, an output shift register and four control signals. MOSI_X is the data input to the input shift register. MISO_X is the data output from the output shift register. SCLK_X is the clock input used to shift data into the input shift register or out from the output one while CS_X is the active low chip select input.

All SPI communications are executed in exact 32-bit increments. The general format of the 32-bit transmission for the SPI interface is shown in Table 5. SPI MOSI_X frame layout and Table 6. SPI MISO_X frame layout

The data sent to the IC (i.e. MOSI_X) consists of a target read register ID (RID), a target write register ID (WID), write data parity (WPAR) and 16 bits of data (WRITE). WRITE data is the data to be written to the target write register indicated by WID. Data returned from the IC (i.e. MISO_X) consists of a global status word (GSW), read data parity (RPAR) and 20 bits of data (READ). READ data will be the contents of the target read register as indicated by the RID bits. The parity bits WPAR and RPAR cover all the 32 bits of the MOSI and MISO frames, respectively. Odd parity type is used.

Table 5. SPI MOSI_X frame layout

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GID	RID[6:0]							WID[6:0]							WPAR	WRITE[15:0]																

Table 6. SPI MISO_X frame layout

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GSW[10:0]											RPAR	READ[19:0]																			

Communications are controlled through CS_X, enabling and disabling communication. When CS_X is at high logic, all SPI communication I/O is tri-stated and no data is accepted. When CS_X is low, data is latched on the rising edge of SCLK_X and data is shifted on the falling edge. The MOSI_X pin receives serial data from the master with MSB first. Likewise for MISO_X, data is read MSB first, LSB last.

The L9679E features a data validation method through the SCLK_X input to keep transmissions with not exactly 32 bits from being written to the device. The SCLK_X input counts the number of received clocks and should the clock counter exceed or count fewer than 32 clocks, the received message is discarded and a SPI_FLT bit is flagged in the Global Status Word (GSW). The SPI_FLT bit is also set in case of parity error detected on the MOSI_X frame. Any attempt to access a register with forbidden access mode (read or write) does not lead to changes to the internal registers, but the SPI_FLT bit is not set in this case.

6.2 Global SPI register map

The Global SPI interface consists of several 32-bit registers which allow the configuration, control and status of the IC as well as special manufacturing test modes. The register definition is defined by the read register ID (RID) and the write register ID (WID) as shown in Table 7. Global SPI register map. The Global ID bit (GID) is used to extend the available register addresses, but it is shared between RID and WID; only RID and WID with the same GID value can be addressed within the same SPI word. The operating states here below show in which states the SPI command is processed.

The L9679E checks the validity of the received WID and RID fields in the MOSI_G frame. Should an SPI write command with WID matching a writeable register be received in an illegal operating state, the command will be discarded and the ERR_WID bit will be flagged in the next Global Status Word GSW. The ERR_WID flag is not set in case WID addresses a read/only register. Should a SPI read command be received containing an unused RID address, the command will be discarded and the ERR_RID bit will be flagged in the current GSW.

Table 7. Global SPI register map

GID	RID / WID								Hex	R/W	Name	Description	Operating state(1)		
													Init	Diag	Safing
0	0	0	0	0	0	0	0	0	0x00	R	FLTSR	Global fault status register			
0	0	0	0	0	0	0	1	0	0x01	R/W	SYS_CFG	General system initialization	√		
0	0	0	0	0	0	1	0	0	0x02	R/W	SYS_CTL	General system configuration	√	√	√
0	0	0	0	0	0	1	1	0	0x03	W	SPI_SOFT_RESET	Command to trigger internal SSM reset	√	√	√
0	0	0	0	0	1	0	0	0	0x04	R	SYS_STATE	Read register to report in which operating state the device is			
0	0	0	0	0	1	0	1	0	0x05	R	POWER_STATE	Power state register (feedback on voltage thresholds)			
0	0	0	0	0	1	1	0	0	0x06	R/W	DCR_0	Deployment configuration register		√	√
0	0	0	0	0	1	1	1	0	0x07	R/W	DCR_1			√	√
0	0	0	0	1	0	0	0	0	0x08	R/W	DCR_2			√	√
0	0	0	0	1	0	0	1	0	0x09	R/W	DCR_3			√	√
0	0	0	0	1	0	1	0	0	0x0A	R/W	DCR_4			√	√
0	0	0	0	1	0	1	1	0	0x0B	R/W	DCR_5			√	√
0	0	0	0	1	1	0	0	0	0x0C	R/W	DCR_6			√	√
0	0	0	0	1	1	0	1	0	0x0D	R/W	DCR_7			√	√
0	0	0	0	1	1	1	0	0	0x0E						
0	0	0	0	1	1	1	1	0	0x0F						
0	0	0	1	0	0	0	0	0	0x10						
0	0	0	1	0	0	0	1	0	0x11						
0	0	0	1	0	0	1	0	0	0x12	R/W	DEPCOM	Deployment command register			√
0	0	0	1	0	0	1	1	0	0x13	R	DSR_0	Deployment status register			
0	0	0	1	0	1	0	0	0	0x14	R	DSR_1				
0	0	0	1	0	1	0	1	0	0x15	R	DSR_2				
0	0	0	1	0	1	1	0	0	0x16	R	DSR_3				
0	0	0	1	0	1	1	1	0	0x17	R	DSR_4				
0	0	0	1	1	0	0	0	0	0x18	R	DSR_5				
0	0	0	1	1	0	0	1	0	0x19	R	DSR_6				
0	0	0	1	1	0	1	0	0	0x1A	R	DSR_7				

GID	RID / WID								Hex	R/W	Name	Description	Operating state[1]		
													Init	Diag	Safing
0	0	0	1	1	0	1	1		0x1B						
0	0	0	1	1	1	0	0		0x1C						
0	0	0	1	1	1	0	1		0x1D						
0	0	0	1	1	1	1	0		0x1E						
0	0	0	1	1	1	1	1		0x1F	R	DCMTS01	Deployment current monitor register			
0	0	1	0	0	0	0	0		0x20	R	DCMTS23				
0	0	1	0	0	0	0	1		0x21	R	DCMTS45				
0	0	1	0	0	0	1	0		0x22	R	DCMTS67				
0	0	1	0	0	0	1	1		0x23						
0	0	1	0	0	1	0	0		0x24						
0	0	1	0	0	1	0	1		0x25	R/W	SPIDEPEN	Lock/Unlock command			√
0	0	1	0	0	1	1	0		0x26	R	LP_GNDLOSS	Loss of ground fault for squib/pyroswitch loops			
0	0	1	0	0	1	1	1		0x27	R	VERSION_ID	Device version			
0	0	1	0	1	0	0	0		0x28						
0	0	1	0	1	0	0	1		0x29						
0	0	1	0	1	0	1	0		0x2A						
0	0	1	0	1	0	1	1		0x2B						
0	0	1	0	1	1	0	0		0x2C						
0	0	1	0	1	1	0	1		0x2D	R/W	CLK_CONF	Clock configuration	√	√	√
0	0	1	0	1	1	1	0		0x2E						
0	0	1	0	1	1	1	1		0x2F						
0	0	1	1	0	0	0	0		0x30						
0	0	1	1	0	0	0	1		0x31	W	SAFING_STATE	Safing State command		√	√
0	0	1	1	0	0	1	0		0x32						
0	0	1	1	0	0	1	1		0x33						
0	0	1	1	0	1	0	0		0x34						
0	0	1	1	0	1	0	1		0x35		DIAG_STATE	Diag State command	√	√	√
0	0	1	1	0	1	1	0		0x36	R/W	SYSDIAGREQ	Diagnostic command for system safing		√	
0	0	1	1	0	1	1	1		0x37	R	LPDIAGSTAT	Diagnostic result register for deployment loops			
0	0	1	1	1	0	0	0		0x38	R/W	LPDIAGREQ	Diagnostic configuration command for deployment loops		√	√
0	0	1	1	1	0	0	1		0x39						

GID	RID / WID							Hex	R/W	Name	Description	Operating state(1)		
												Init	Diag	Safing
0	0	1	1	1	0	1	0	0x3A	R/W	DIAGCTRL_A	In WID is A to D converter control register A. In RID is A to D result A request.		√	√
0	0	1	1	1	0	1	1	0x3B	R/W	DIAGCTRL_B	In WID is A to D converter control register B. In RID is A to D result B request.		√	√
0	0	1	1	1	1	0	0	0x3C	R/W	DIAGCTRL_C	In WID is A to D converter control register C. In RID is A to D result C request.		√	√
0	0	1	1	1	1	0	1	0x3D	R/W	DIAGCTRL_D	In WID is A to D converter control register D. In RID is A to D result D request.		√	√
0	0	1	1	1	1	1	0	0x3E						
0	0	1	1	1	1	1	1	0x3F						
0	1	0	0	0	0	0	0	0x40						
0	1	0	0	0	0	0	1	0x41						
0	1	0	0	0	0	1	0	0x42						
0	1	0	0	0	0	1	1	0x43						
0	1	0	0	0	1	0	0	0x44						
0	1	0	0	0	1	0	1	0x45						
0	1	0	0	0	1	1	0	0x46						
0	1	0	0	0	1	1	1	0x47						
0	1	0	0	1	0	0	0	0x48						
0	1	0	0	1	0	0	1	0x49						
0	1	0	0	1	0	1	0	0x4A	R/W	RSCR0	PSI-5 configuration register		√	
0	1	0	0	1	0	1	1	0x4B	R/W	RSCR1			√	
0	1	0	0	1	1	0	0	0x4C	R/W	RSCR2			√	
0	1	0	0	1	1	0	1	0x4D	R/W	RSCR3			√	
0	1	0	0	1	1	1	0	0x4E	R/W	RSCTRL	Remote sensor control register		√	√
0	1	0	0	1	1	1	1	0x4F						
0	1	0	1	0	0	0	0	0x50						
0	1	0	1	0	0	0	1	0x51						
0	1	0	1	0	0	1	0	0x52						
0	1	0	1	0	0	1	1	0x53						
0	1	0	1	0	1	0	0	0x54						

GID	RID / WID							Hex	R/W	Name	Description	Operating state(1)		
												Init	Diag	Safing
0	1	0	1	0	1	0	1	0x55						
0	1	0	1	0	1	1	0	0x56						
0	1	0	1	0	1	1	1	0x57						
0	1	0	1	1	0	0	0	0x58						
0	1	0	1	1	0	0	1	0x59						
0	1	0	1	1	0	1	0	0x5A						
0	1	0	1	1	0	1	1	0x5B						
0	1	0	1	1	1	0	0	0x5C						
0	1	0	1	1	1	0	1	0x5D						
0	1	0	1	1	1	1	0	0x5E						
0	1	0	1	1	1	1	1	0x5F						
0	1	1	0	0	0	0	0	0x60						
0	1	1	0	0	0	0	1	0x61						
0	1	1	0	0	0	1	0	0x62						
0	1	1	0	0	0	1	1	0x63						
0	1	1	0	0	1	0	0	0x64						
0	1	1	0	0	1	0	1	0x65						
0	1	1	0	0	1	1	0	0x66						
0	1	1	0	0	1	1	1	0x67						
0	1	1	0	1	0	0	0	0x68						
0	1	1	0	1	0	0	1	0x69						
0	1	1	0	1	0	1	0	0x6A	R	ARM_STATE	Status of arming signals			
0	1	1	0	1	0	1	1	0x6B						
0	1	1	0	1	1	0	0	0x6C						
0	1	1	0	1	1	0	1	0x6D						
0	1	1	0	1	1	1	0	0x6E	R/W	LOOP_MATRIX_ ARM1	Assignment of FEN1 pin to which LOOPS		√	
0	1	1	0	1	1	1	1	0x6F	R/W	LOOP_MATRIX_ ARM2	Assignment of FEN2 pin to which LOOPS		√	
0	1	1	1	0	0	0	0	0x70						
0	1	1	1	0	0	0	1	0x71						
0	1	1	1	0	0	1	0	0x72						
0	1	1	1	0	0	1	1	0x73						
0	1	1	1	0	1	0	0	0x74						
0	1	1	1	0	1	0	1	0x75						
0	1	1	1	0	1	1	0	0x76						
0	1	1	1	0	1	1	1	0x77						
0	1	1	1	1	0	0	0	0x78						
0	1	1	1	1	0	0	1	0x79						

GID	RID / WID							Hex	R/W	Name	Description	Operating state(1)		
												Init	Diag	Safing
0	1	1	1	1	0	1	0	0x7A						
0	1	1	1	1	0	1	1	0x7B						
0	1	1	1	1	1	0	0	0x7C						
0	1	1	1	1	1	0	1	0x7D						
0	1	1	1	1	1	1	0	0x7E						
0	1	1	1	1	1	1	1	0x7F						
1	0	0	0	0	0	0	0	0x80						
1	0	0	0	0	0	0	1	0x81						
1	0	0	0	0	0	1	0	0x82						
1	0	0	0	0	0	1	1	0x83						
1	0	0	0	0	1	0	0	0x84						
1	0	0	0	0	1	0	1	0x85						
1	0	0	0	0	1	1	0	0x86						
1	0	0	0	0	1	1	1	0x87						
1	0	0	0	1	0	0	0	0x88						
1	0	0	0	1	0	0	1	0x89						
1	0	0	0	1	0	1	0	0x8A						
1	0	0	0	1	0	1	1	0x8B						
1	0	0	0	1	1	0	0	0x8C						
1	0	0	0	1	1	0	1	0x8D						
1	0	0	0	1	1	1	0	0x8E						
1	0	0	0	1	1	1	1	0x8F						
1	0	0	1	0	0	0	0	0x90						
1	0	0	1	0	0	0	1	0x91						
1	0	0	1	0	0	1	0	0x92						
1	0	0	1	0	0	1	1	0x93						
1	0	0	1	0	1	0	0	0x94						
1	0	0	1	0	1	0	1	0x95						
1	0	0	1	0	1	1	0	0x96						
1	0	0	1	0	1	1	1	0x97						
1	0	0	1	1	0	0	0	0x98						
1	0	0	1	1	0	0	1	0x99						
1	0	0	1	1	0	1	0	0x9A						
1	0	0	1	1	0	1	1	0x9B						
1	0	0	1	1	1	0	0	0x9C						
1	0	0	1	1	1	0	1	0x9D						
1	0	0	1	1	1	1	0	0x9E						
1	0	0	1	1	1	1	1	0x9F						

GID	RID / WID							Hex	R/W	Name	Description	Operating state(1)		
												Init	Diag	Safing
1	0	1	0	0	0	0	0	0xA0						
1	0	1	0	0	0	0	1	0xA1						
1	0	1	0	0	0	1	0	0xA2						
1	0	1	0	0	0	1	1	0xA3						
1	0	1	0	0	1	0	0	0xA4						
1	0	1	0	0	1	0	1	0xA5						
1	0	1	0	0	1	1	0	0xA6						
1	0	1	0	0	1	1	1	0xA7						
1	0	1	0	1	0	0	0	0xA8						
1	0	1	0	1	0	0	1	0xA9						
1	0	1	0	1	0	1	0	0xAA						
1	0	1	0	1	0	1	1	0xAB						
1	0	1	0	1	1	0	0	0xAC						
1	0	1	0	1	1	0	1	0xAD						
1	0	1	0	1	1	1	0	0xAE						
1	0	1	0	1	1	1	1	0xAF						
1	0	1	1	0	0	0	0	0xB0						
1	0	1	1	0	0	0	1	0xB1						
1	0	1	1	0	0	1	0	0xB2						
1	0	1	1	0	0	1	1	0xB3						
1	0	1	1	0	1	0	0	0xB4						
1	0	1	1	0	1	0	1	0xB5						
1	0	1	1	0	1	1	0	0xB6						
1	0	1	1	0	1	1	1	0xB7						
1	0	1	1	1	0	0	0	0xB8						
1	0	1	1	1	0	0	1	0xB9						
1	0	1	1	1	0	1	0	0xBA						
1	0	1	1	1	0	1	1	0xBB						
1	0	1	1	1	1	0	0	0xBC						
1	0	1	1	1	1	0	1	0xBD						
1	0	1	1	1	1	1	0	0xBE						
1	0	1	1	1	1	1	1	0xBF						
1	1	0	0	0	0	0	0	0xC0						
1	1	0	0	0	0	0	1	0xC1						
1	1	0	0	0	0	1	0	0xC2						
1	1	0	0	0	0	1	1	0xC3						
1	1	0	0	0	1	0	0	0xC4						
1	1	0	0	0	1	0	1	0xC5						

GID	RID / WID							Hex	R/W	Name	Description	Operating state(1)		
												Init	Diag	Safing
1	1	0	0	0	1	1	0	0xC6						
1	1	0	0	0	1	1	1	0xC7						
1	1	0	0	1	0	0	0	0xC8						
1	1	0	0	1	0	0	1	0xC9						
1	1	0	0	1	0	1	0	0xCA						
1	1	0	0	1	0	1	1	0xCB						
1	1	0	0	1	1	0	0	0xCC						
1	1	0	0	1	1	0	1	0xCD						
1	1	0	0	1	1	1	0	0xCE						
1	1	0	0	1	1	1	1	0xCF						
1	1	0	1	0	0	0	0	0xD0						
1	1	0	1	0	0	0	1	0xD1						
1	1	0	1	0	0	1	0	0xD2						
1	1	0	1	0	0	1	1	0xD3						
1	1	0	1	0	1	0	0	0xD4						
1	1	0	1	0	1	0	1	0xD5						
1	1	0	1	0	1	1	0	0xD6						
1	1	0	1	0	1	1	1	0xD7						
1	1	0	1	1	0	0	0	0xD8						
1	1	0	1	1	0	0	1	0xD9						
1	1	0	1	1	0	1	0	0xDA						
1	1	0	1	1	0	1	1	0xDB						
1	1	0	1	1	1	0	0	0xDC						
1	1	0	1	1	1	0	1	0xDD						
1	1	0	1	1	1	1	0	0xDE						
1	1	0	1	1	1	1	1	0xDF						
1	1	1	0	0	0	0	0	0xE0						
1	1	1	0	0	0	0	1	0xE1						
1	1	1	0	0	0	1	0	0xE2						
1	1	1	0	0	0	1	1	0xE3						
1	1	1	0	0	1	0	0	0xE4						
1	1	1	0	0	1	0	1	0xE5						
1	1	1	0	0	1	1	0	0xE6						
1	1	1	0	0	1	1	1	0xE7						
1	1	1	0	1	0	0	0	0xE8						
1	1	1	0	1	0	0	1	0xE9						
1	1	1	0	1	0	1	0	0xEA						
1	1	1	0	1	0	1	1	0xEB						

GID	RID / WID								Hex	R/W	Name	Description	Operating state[1]		
													Init	Diag	Safing
1	1	1	0	1	1	0	0		0xEC						
1	1	1	0	1	1	0	1		0xED						
1	1	1	0	1	1	1	0		0xEE						
1	1	1	0	1	1	1	1		0xEF						
1	1	1	1	0	0	0	0		0xF0						
1	1	1	1	0	0	0	1		0xF1						
1	1	1	1	0	0	1	0		0xF2						
1	1	1	1	0	0	1	1		0xF3						
1	1	1	1	0	1	0	0		0xF4						
1	1	1	1	0	1	0	1		0xF5						
1	1	1	1	0	1	1	0		0xF6						
1	1	1	1	0	1	1	1		0xF7						
1	1	1	1	1	0	0	0		0xF8						
1	1	1	1	1	0	0	1		0xF9						
1	1	1	1	1	0	1	0		0xFA						
1	1	1	1	1	0	1	1		0xFB						
1	1	1	1	1	1	0	0		0xFC						
1	1	1	1	1	1	0	1		0xFD						
1	1	1	1	1	1	1	0		0xFE						
1	1	1	1	1	1	1	1		0xFF						

1. A checkmark indicates in which operating state a WRITE-command is valid

6.3 Global SPI tables

A summary of all the registers contained within the global SPI map is shown below and is referenced throughout the specification as they apply. The SPI register tables also specify the effect of the internal reset signals assertion on each bit field.

Note: The symbol '-' is used to indicate that the register is not affected by the relevant reset signal.

6.3.1 Global SPI global status word

The Global SPI frame contains an 11-bit word that returns global status information. The Global Status Word (GSW) of the Global SPI is the most significant 11 bits of MISO_G data.

Table 8. Global SPI global status Word

MISO_G	GSW	Name	POR	WSM	SSM	Description
31	10	SPIFLT	0	0	0	SPI Fault, set if previous SPI frame had wrong parity check or wrong number of bits, cleared upon read 0: No fault 1: Fault
30	9	DEPOK	0	0	0	General Deployment Successful Flag, logical OR of the corresponding CHxDS bits (bit 15) in DSRx Registers 0: All the DSRx-CHDS bits are 0 1: At least one of the DSRx-CHDS bits is 1
29	8		0	0	0	Unused
28	7		0	0	0	Unused
27	6		0	0	0	Unused
26	5	POWERFLT	0	0	0	Fault present in Power State Register, logical OR between bits from 15 to 14 of POWER_STATE Register 0: All the bits from 15 to 14 in the POWER_STATE Registers are 0s 1: At least one of the bits from 15 to 14 in the POWER_STATE Registers is 1
25	4	FLT	1	1	1	Fault present in Fault Status Register (FLTSR), logical OR between all bits of FLTSR 0: All the bits in the Fault Status Register (FLTSR) are 0s 1: At least one of the bits in the Fault Status Register (FLTSR) is 1
24	3	CONVRDY2	0	0	0	ADC Conversion of request C or D has been completed so new results are available 0: No new data available 1: New data available
23	2	CONVRDY1	0	0	0	ADC Conversion of request A or B has been completed so new results are available 0: No new data available 1: New data available
22	1	ERR_WID	0	0	0	Write address of previous SPI frame is not permitted in current operating phase 0: No Error 1: Error
21	0	ERR_RID	0	0	0	Read address received in the actual SPI frame is unused so data in the response is don't care 0: No Error 1: Error

6.4 Global SPI read/write registers

FLTSR

Fault status register

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	0	0	0	CLKFRERR	0	0	0	0	OTPCRC_ERR	0	0	0	0	0	0	0	0	SSMRST	0	POR

ID: 00
Type: R
Read: 0000
Write: -

	POR	WSM	SSM	
[16]	-	-	-	CLKFRERR: Internal oscillator cross-check error bit. Set when osc. error detected, cleared on SPI read or SUPPLY_POR=1 0: No Fault 1: Fault
[11]	0	-	-	OTPCRC_ERR: OTP CRC error bit Set when OTP error detected (tested at release of POR), cleared by POR=1 0: No Fault 1: Fault
[2]	1	1	1	SSMRST: Safing state machine reset Set when SSM reset goes to '1', cleared upon SPI read 0: SSM reset has not occurred 1: SSM Reset has occurred
[0]	1	-	-	POR: Power on Reset Set when POR goes to '1', cleared upon SPI read 0: POR reset has not occurred 1: POR Reset has occurred

SYS_CFG

System configuration register

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				EN_AUTO_SWITCH_OFF	X	X	X	X	HI_LEV_DIAG_TIME	RSU_SYNCPULSE_SHIFT_CONF	SQMEAS		VMEAS		X	FENL_ACT	X	X	X
MISO	0	0	0	0	EN_AUTO_SWITCH_OFF	0	0	0	0	HI_LEV_DIAG_TIME	RSU_SYNCPULSE_SHIFT_CONF	SQMEAS		VMEAS		0	FENL_ACT	0	0	0

ID: 01
Type: R/W
Read: 0100
Write: 0002

	POR	WSM	SSM	
[15]	0	0	0	EN_AUTO_SWITCH_OFF: Enable auto switch off ISRC current source and DCS regulator after measurement completion 0: Auto switch off disabled 1: Auto switch off enabled
[10]	0	0	0	HI_LEV_DIAG_TIME: Selection of duration of high level squib/pyroswitch diagnostics 0: Short time (see high level diag diagram) 1: Long time (see high level diag diagram)
[9]	0	0	0	RSU_SYNCPULSE_SHIFT_CONF: Selection of sync pulses shift duration 0 Long time 1 Short time
[8:7]	00	00	00	SQMEAS: Sample number in squib/pyroswitch measurement and temperature conversions: Updated by SSM_RESET or SPI write 00: 8 samples

				01: 16 samples 10: 4 samples 11: 2 sample
[6:5]	00	00	00	VMEAS: Sample number in any other voltage measurement conversions Updated by SSM_RESET or SPI write 00: 4 samples 01: 16 samples 10: 8 samples 11: 1 sample
[3]	0	0	0	FENL_ACT: FENL enable low sides Updated by SSM_RESET or SPI write 0: FENL is not used (specific low sides enable when related high sides is enabled) 1: FENL enables (when high) all low sides

SYS_CTL

System control register

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	PD&VRCM_SEL	X	VSAT_TH_SEL	X	X	X	X	X	X	X	X	X	X	X	X
MISO	0	0	0	0	0	PD&VRCM_SEL	0	VSAT_TH_SEL	0	0	0	0	0	0	0	0	0	0	0	0

ID: 02

Type: R/W

Read: 0200

Write: 0004

	POR	WSM	SSM	
[14]	0	0	0	PD&VRCM_SEL: Squib/Pyroswitch pull down current level and VRCM leakage to GND threshold selection 0: 1 mA pull down current and 450 µA VRCM leakage to GND threshold 1: 5 mA pull down current and 2 mA VRCM leakage to GND threshold
[12]	0	0	0	VSAT_TH_SEL: VSAT comparators threshold selector 0: VSAT_OK= VSAT_OK_TH0 1: VSAT_OK= VSAT_OK_TH1

SPI_Soft_Reset

SPI soft reset command

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI			'									0x3C95								
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ID: 03

Type: W

Read: -

Write: 006

	POR	WSM	SSM	
[15:0]	N/A	N/A	N/A	SPI_Soft_Reset: Non-latched command that allows assertion of SSM_Reset that means initialization of registers to default value and stat machine to idle state.

SYS_STATE

System state register

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	0	0	0	0	0	0	0	0	0	OPER_CTL_STATE			0	0	0	0	0	0	0	0

ID: 04

Type: R

Read: 0400

Write: -

	POR	WSM	SSM	
[10:8]	000	000	000	OPER_CTL_STATE[2:0]: Reports operating control state Updated per power up phases diagram 000: INIT 001: DIAG 010: SAFING 011: unused 100: unused 101: unused 110: unused 111: unused

POWER_STATE

Power state register

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI					X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO					VSAT_NOK	VSINK_NOK	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ID: 05

Type: R

Read: 0500

Write: -

	POR	WSM	SSM	
[15]	-	-	-	VSAT_NOK: VSAT bad pin status Set base on voltage, cleared on SPI read 0: VSAT > VSAT_OK 1: VSAT < VSAT_OK
[14]	-	-	-	VSINK_NOK: VSYNC bad pin status Set based on voltage, cleared on SPI read. At power-up (when VSAT goes up), this bit is not masked so will be set to 1 if VSYNC supply goes up later than VSAT. 1: VSYNC < VSYNC_OK 0: VSYNC > VSYNC_OK

DCR_x(x=0, 2, 4, 6)

Deployment configuration channel 0, 2, 4, 6 (DCR_x)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	Deploy_Time						Dep_Current		Dep_expire_time		X	PD_CURR_CSR
MISO	0	0	0	0	0	0	0	0	Deploy_Time						Dep_Current		Dep_expire_time		0	PD_CURR_CSR

ID: 06 (DCR_0), 08 (DCR_2), 0A (DCR_4), 0C (DCR_6)

Type: RW

Read: 0600 (DCR_0), 0800 (DCR_2), 0A00 (DCR_4), 0C00 (DCR_6)

Write: 000C (DCR_0), 0010 (DCR_2), 0014 (DCR_4), 0018 (DCR_6)

	POR	WSM	SSM	
[11:6]	000000	000000	000000	Deploy_Time[5:0]: Default deployment time = 0 µs (no deployment, 8 µs pulse output on ARM1 pin during PULSE TEST) Deployment time: actual deployment time (ms) = Deploy_Time*0.064 ms (0.064 ms/count up to 4.032 ms max)
[5:4]	00	00	00	Dep_Current[1:0]: Deployment Current limit select Updated by SSM_RESET or SPI write while in DIAG state 00: Unused (no deploy) 01: 1.75 A min 10: 1.2 A min 11: Unused (no deploy)
[3:2]	00	00	00	Dep_expire_time[1:0]: Deploy command expiration timer select Updated by SSM_RESET or SPI write while in DIAG state 00: 500 ms 01: 250 ms 10: 125 ms 11: 0 ms
[0]	0	0	0	PD_CURR_CSR: Pull down current control for Common SR connection Updated by SSM_RESET or SPI write 0: PD Current OFF only for channel selected for diagnostic measurement, ON for all other channel 1: PD Current OFF for both channels of the channel pair selected for diagnostic measurement, ON for all other channel

DCR_x(x=1, 3, 5, 7)

Deployment configuration channel 1, 3, 5, 7 (DCR_x)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	Deploy_Time						Dep_Current		Dep_expire_time		X	X
MISO	0	0	0	0	0	0	0	0	Deploy_Time						Dep_Current		Dep_expire_time		0	0

ID: 07 (DCR_1), 09 (DCR_3), 0B (DCR_5), 0D (DCR_7)

Type: R/W

Read: 0700 (DCR_1), 0900 (DCR_3), 0B00 (DCR_5), 0D00 (DCR_7)

Write: 000E (DCR_1), 0012 (DCR_3), 0016 (DCR_5), 001A (DCR_7)

	POR	WSM	SSM	
[11:6]	000000	000000	000000	Deploy_Time[5:0]: Default deployment time = 0 µs (no deployment, 8 µs pulse output on ARM1 pin during PULSE TEST) Deployment time: actual deployment time (ms) = Deploy_Time*0.064 ms (0.064 ms/count up to 4.032 ms max)
[5:4]	00	00	00	Dep_Current[1:0]: Deployment Current limit selectUpdated by SSM_RESET or SPI write while in DIAG state 00: Unused (no deploy) 01: 1.75 A min 10: 1.2 A min 11: Unused (no deploy)
[3:2]	00	00	00	Dep_expire_time[1:0]: Deploy command expiration timer select Updated by SSM_RESET or SPI write while in DIAG state 00: 500 ms 01: 250 ms 10: 125 ms 11: 0 ms

DEPCOM

Deployment command

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	CH7DEPREQ	CH6DEPREQ	CH5DEPREQ	CH4DEPREQ	CH3DEPREQ	CH2DEPREQ	CH1DEPREQ	CH0DEPREQ
MISO	0	0	0	0	0	0	0	0	0	0	0	0	CH7DEP	CH6DEP	CH5DEP	CH4DEP	CH3DEP	CH2DEP	CH1DEP	CH0DEP

ID: 12

Type: R/W

Read: 1200

Write: 0024

	POR	WSM	SSM	
[7:0]	N/A	N/A	N/A	CHxDEPREQ: Channel x Deploy Request - non-latched channel-specific deploy request 0: No change to deployment control for channel x 1: Clear and start Expiration timer if in ARMING or SAFING state and in DEPLOY_ENABLED state
[7:0]	0	0	0	CHxDEP: Channel x deployment expiration timer enable Set when SPI_DEPCOM(CHxDEPREQ=1) AND in ARMING or SAFING state AND in DEP_ENABLED state Cleared on SSM_RESET OR when in DEP_DISABLED state OR when Deploy Expiration Timer x reaches timeout threshold 1: Expiration timer enabled - Deploy command still valid 0: Expiration Timer disabled - Deploy command no more valid

DSR_x (x=0 to 7)

Deployment status channel x

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	0	0	0	0	CHxDS	CHxSTAT	0	DCRxERR							DEP_CHx_ExpTimer					

ID: 13 (DSR_0), 14 (DSR_1), 15 (DSR_2), 16 (DSR_3), 17 (DSR_4), 18 (DSR_5), 19 (DSR_6), 1A (DSR_7)

Type: R

Read: 1300 (DSR_0), 1400 (DSR_1), 1500 (DSR_2), 1600 (DSR_3), 1700 (DSR_4), 1800 (DSR_5), 1900 (DSR_6), 1A00 (DSR_7)

Write: -

	POR	WSM	SSM	
[15]	0	0	0	CHxDS: Channel x deployment successful Updated according to Deployment Driver Control Logic (set when deployment terminates on ch x due to deploy timer timeout, cleared on SSM_RESET OR when deployment starts on ch x) 0: Deployment not successful 1: Deployment successful
[14]	0	0	0	CHxSTAT: Channel x deployment status Updated according to Deployment Driver Control Logic (set when deployment starts on ch x, cleared on SSM_RESET OR when deployment terminates due to deploy timer timeout, LS Over current OR GND Loss) 0 Deployment not in progress 1 Deployment in progress
[12]	0	0	0	DCRxERR: Deployment configuration register error 0 Deploy configuration change accepted and stored in memory 1 Deploy configuration change rejected because deploy is in progress (or DEP_EXPIRE_TIME changed when in DEP_ENABLED state)
[5:0]	000000	000000	000000	DEP_CHx_ExpTimer[5:0]: Channel x Deployment Expiration Timer value 8 ms/count Updated according to Deployment Driver Control Logic (Cleared on SSM_RESET OR when Exp Timer times out OR when SPI_DEPREQx is received while in DEP_ENABLED state AND in ARMING or SAFING states)

DCMTSxy (xy=01,23,45,67)

Deployment current monitor registers

channel 0,1 (DDCMTS01), channel 2,3 (DDCMTS23), channel 4,5 (DDCMTS45), channel 6,7 (DDCMTS67)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	'				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	0	0	0	0	Current_Mon_Timer_y[7:0]								Current_Mon_Timer_x[7:0]							

ID: 1F (DDCMTS01), 20 (DDCMTS23), 21 (DDCMTS45), 22 (DDCMTS67)

Type: R

Read: 1F00 (DDCMTS01), 2000 (DDCMTS23), 2100 (DDCMTS45), 2202 (DDCMTS67)

Write: -

	POR	WSM	SSM	
[15:8]	0x00	0x00	0x00	Current_Mon_Timer_y[7:0]: Channel y current monitor timer value corresponding to SPI command DCMTSxy. Set to default (cleared) on SSM_RESET or when a new deployment starts on channel y. Increments each 16 µs while deployment current exceeds monitor threshold on channel y
[7:0]	0x00	0x00	0x00	Current_Mon_Timer_x[7:0]:Channel x current monitor timer value corresponding to SPI command DCMTSxy. Set to default (cleared) on SSM_RESET or when a new deployment starts on channel x. Increments each 16 µs while deployment current exceeds monitor threshold on channel y

SPIDEPEN

Deploy enable register

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				DEPEN_WR[15:0]															
MISO	0	0	0	0	DEPEN_STATE[15:0]															

ID: 25

Type: R/W

Read: 2500

Write: 004A

	POR	WSM	SSM	
[15:0]	N/A	N/A	N/A	DEPEN_WR[15:0]: Non-latched encoded value for LOCK / UNLOCK command 0x0FF0 LOCK - enter DEP_DISABLED state 0xF00F UNLOCK - enter DEP_ENABLED state.
[15:0]	0x0FF0	0x0FF0	0x0FF0	DEPEN_STATE[15:0]: Deploy Enabled State Updated according to Global SPI Deployment Enable State Diagram 0x0FF0 In DEP_DISABLED state 0xF00F In DEP_ENABLED state

LP_GNDLOSS

Deployment ground loss register

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	'				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	0	0	0	0	0	0	0	0	0	0	0	0	GNDLOSS7	GNDLOSS6	GNDLOSS5	GNDLOSS4	GNDLOSS3	GNDLOSS2	GNDLOSS1	GNDLOSS0

ID: 26

Type: R

Read: 2600

Write: -

	POR	WSM	SSM	
[7]	0	0	0	GNDLOSSx: Loop x Squib/Pyroswitch Ground loss Cleared upon SSM_RESET or SPI read. Set when GND loss is detected during deployment or loop diag's (HS sw test, LS sw test, squib/pyroswitch resistance) 0: Loss of ground not detected 1: Loss of ground detected

VERSION_ID

Device version register

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	'				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	0	0	0	0	0	0	0	0	0	DEVICE ID			0	0	VERSN					

ID: 27

Type: R

Read: 2700

Write: -

	POR	WSM	SSM	
[10:8]	-	-	-	DEVICE ID: Identification of the device Static value - never updated 001: Low end 010: Medium end 011: High end 100: Extension
[5:0	-	-	-	VERSN: Identification of the silicon version Static value - never updated 000000: AA version 000001: AB version 001000: BA version 001001: BB version 010000: CA version 010001: CB version 010010: CC version

CLK_CONF

Clock configuration register

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	AUX_SS_DIS	MAIN_SS_DIS	X	X
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	AUX_SS_DIS	MAIN_SS_DIS	0	0

ID: 2D

Type: R/W

Read: 2D00

Write: 005A

	POR	WSM	SSM	
[3]	1	-	-	AUX_SS_DIS: Auxiliary oscillator Spread Spectrum disable Updated by POR or SPI write 0: Spread Spectrum enabled 1: Spread Spectrum disabled
[2]	0	-	-	MAIN_SS_DIS: Main oscillator Spread Spectrum disable Updated by POR or SPI write 0: Spread Spectrum enabled 1: Spread Spectrum disabled

SAFING_STATE

Safing state entry command

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	'				0xACAC															
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ID: 31

Type: W

Read: -

Write: 0062

POR	WSM	SSM	
N/A	N/A	N/A	Non-latched Safing State entry command Enter safing state from DIAG state and clear arming pulse stretch counter (if received in DIAG or SAFING state)

DIAG_STATE

Diag state entry command

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	'				0x3C								0xC3							
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ID: 35

Type: W

Read: -

Write: 006A

POR	WSM	SSM	
N/A	N/A	N/A	Non-latched Diag State entry command Enter DIAG state from INIT state

SYSDIAGREQ

System diagnostic register

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	DSTEST[3:0]			
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DSTEST[3:0]			

ID: 36

Type: R/W

Read: 3600

Write: 006C

	POR	WSM	SSM	
[3:0]	0000	0000	0000	DSTEST[3:0]: Diagnostic State Test selection Updated by SSM_RESET or SPI write while in DIAG state 0000: all outputs inactive 0001: FENL pin active 0010: all outputs inactive 0011: all outputs inactive 0100: all outputs inactive 0101: all outputs inactive 0110: all outputs inactive 0111: HS squib/pyroswitch driver FET active 1000: LS squib/pyroswitch driver FET active 1001: Output deployment timing pulses on FENL (separated by 8 ms) 1010: all outputs inactive 1011 - 1111: all outputs inactive

LPDIAGSTAT

Diagnostic result register for deployment loops

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	DIAG_LEVEL	TIP	0	FP	FETON	HS_DRV_OK	HSR_HI	HSR_LO	RES_MEAS_CHSEL/HIGH_LEV_DIAG_SELECTED				SBL	STG	STB	SQP	LEAK_CHSEL			

ID: 37
Type: R
Read: 3700
Write: -

	POR	WSM	SSM	
[19]	0	0	0	DIAG_LEVEL: Diagnostic mode selector (Not present for low level diagnostic) 0: low level mode 1: high level mode
[18]	0	0	0	TIP: High level diagnostic test is running Updated by SSM_RESET or Loops diagnostic state machine 0: High level diagnostic test is not running 1: High level diagnostic test is running
[16]	0	0	0	FP: Fault present before requested diagnostic Updated by SSM_RESET or Loops diagnostic state machine 0: Fault not present before requested diagnostic 1: Fault present before requested diagnostic
[15]	0	0	0	FETON:FET activation during diagnostic Updated by SSM_RESET or Loops diagnostic state machine or when HS or LS FET is activated during DIAG state 0: FET is off during diagnostic 1: FET is on during diagnostic

[14]	0	0	0	HS_DRV_OK: FET Test Status Updated by SSM_RESET or Loops diagnostic state machine or when driver full path test is run test is run 0: HS squib/pyroswitch driver full path test did not complete successfully 1: HS squib/pyroswitch driver full path test complete successfully
[13]	0	0	0	HSR_HI: HSR Diagnostic - HIGH Range Updated by SSM_RESET or Loops diagnostic state machine or when squib/pyroswitch resistance test is run 0: HSR measurement < HSR HIGH value 1: HSR measurement > HSR HIGH value
[12]	0	0	0	HSR_LO: HSR Diagnostic - Low Range Updated by SSM_RESET or Loops diagnostic state machine or when squib/pyroswitch resistance test is run 1: HSR measurement< HSR LOW value 0: HSR measurement > HSR LOW value
[11:8]	0000	0000	0000	RES_MEAS_CHSEL/HIGH_LEV_DIAG_SELECTED: Channel selected for resistance measurement Updated by SSM_RESET or Loops diagnostic state machine or as determined by squib/ pyroswitch resistance channel selected RES_MEAS_CHSEL[3:0] 0000: Ch 0 0001: Ch 1 0010: Ch 2 0011: Ch 3 0100: Ch 4 0101: Ch 5 0110: Ch 6 0111: Ch 7 0100 - 1111: None Selected HIGH_LEV_DIAG_SELECTED[3:0] 0000: No diagnostic selected 0001: VRCM CHECK 0010: Leakage CHECK 0011: Short Between Loops CHECK 0100: Unused 0101: Squib/Pyroswitch resistance range CHECK 0110: Squib/Pyroswitch resistance measurement 0111: FET test 0100 - 1111: Unused
[7]	0	0	0	SBL: Short between loop state Updated by SSM_RESET or Loops diagnostic state machine 0: Short between squib/pyroswitch loops is not present 1: Short between squib/pyroswitch loops is present
[6]	0	0	0	STG: Short to Ground Test Status Updated by SSM_RESET or Loops diagnostic state machine or as determined by squib/ pyroswitch leakage diagnostic 0: STG not detected 1: STG detected

[5]	0	0	0	STB: Short to Battery Test Status Updated by SSM_RESET or Loops diagnostic state machine or as determined by squib/ pyroswitch leakage diagnostic 0: STB not detected 1: STB detected
[4]	0	0	0	SQP: Squib/Pyroswitch PIN where leakage test has been performed Updated by SSM_RESET or Loops diagnostic state machine or as determined by squib/ pyroswitch leakage diagnostic 0: SRx 1: SFx
[3:0]	0000	0000	0000	LEAK_CHSEL[3:0]: Channel selected for leakage measurement Updated by SSM_RESET or Loops diagnostic state machine or as determined by squib/pyroswitch leakage diagnostic 0000: Ch 0 0001: Ch 1 0010: Ch 2 0011: Ch 3 0100: Ch 4 0101: Ch 5 0110: Ch 6 0111: Ch 7 1100 - 1111 None Selected

LPDIAGREQL

Loops diagnostic configuration command register for low level diagnostic

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				DIAG_LEVEL	ISRC_CURR_SEL	PD_CURR	ISRC [1:0]		ISINK	VRCM[1:0]		RES_MEAS_CHSEL[3:0]				LEAK_CHSEL[3:0]			
MISO	0	0	0	0	DIAG_LEVEL	ISRC_CURR_SEL	PD_CURR	ISRC [1:0]		ISINK	VRCM[1:0]		RES_MEAS_CHSEL[3:0]				LEAK_CHSEL[3:0]			

ID: 38

Type: R/W

Read: 3800

Write: 0070

	POR	WSM	SSM	
[15]	0	0	0	DIAG_LEVEL: Diagnostic mode selector Updated by SSM_RESET or SPI write 0: low level mode 1: N/A - see description below
[14]	0	0	0	ISRC_CURR_SEL: Selection of ISRC current value 0: 40 mA 1: 8 mA
[13]	0	0	0	PD_CURR: Pull down current control Updated by SSM_RESET or SPI write 0: Request OFF only for channels connected to VRCM or ISINK or ISRC, ON for all other channels 1: Request OFF for all channels
[12:11]	00	00	00	ISRC [1:0]: High side current source for channel selected in RES_MEAS_CHSEL[3:0] Updated by SSM_RESET or SPI write 00: OFF 01: ON 40 mA/ 8 mA current for channel selected in RES_MEAS_CHSEL, OFF on all other channels 10: ON bypass current for channel selected in RES_MEAS_CHSEL, OFF ON all other channels 11: ON ISRC 40mA or 8mA current for channel selected in RES_MEAS_CHSEL and connect the SRM Differential Amplifier to the other squib/pyroswitch channel of the selected channel pair
[10]	0	0	0	ISINK: Low side current sink control (max 50 mA) Updated by SSM_RESET or SPI write 0: All channels OFF 1: ON for channel selected by RES_MEAS_CHSEL[3:0], OFF on all other channels

[9:8]	00	00	00	VRCM[1:0]: Voltage regulator current monitor control Updated by SSM_RESET or SPI write 00: VRCM not connected 01: VRCM connected to SFx of channel selected by LEAK_CHSEL[3:0] 10: VRCM connected to SRx of channel selected by LEAK_CHSEL[3:0] and pull down current of the same channel disabled 11: VRCM connected to SRx of channel selected by LEAK_CHSEL[3:0] and pull down current of the same channel enabled (ISINK and ISRC must be switched off)
[7:4]	0000	0000	0000	RES_MEAS_CHSEL[3:0]: Squib/Pyroswitch resistance measurement channel select - selects the channel and muxes for the resistance test, and the channel for HS driver test (full path fet test) activation Updated by SSM_RESET or SPI write 0000: Channel 0 0001: Channel 1 0010: Channel 2 0011: Channel 3 0100: Channel 4 0101: Channel 5 0110: Channel 6 0111: Channel 7 0100 - 1111 None Selected
[3:0]	0000	0000	0000	LEAK_CHSEL[3:0]: Squib/Pyroswitch Leakage Measurement Channel select - selects the channel and muxes for the leakage test, and the channel for HS/LS FET test activation. Updated by SSM_RESET or SPI write 0000: Channel 0 0001: Channel 1 0010: Channel 2 0011: Channel 3 0100 : Channel 4 0101: Channel 5 0110: Channel 6 0111: Channel 7 0100 - 1111: None Selected

LPDIAGREQH

Loops diagnostic configuration command register for high level diagnostic

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				DIAG_LEVEL	X	X	X	X	X	X	X	HIGH_LEVEL_DIAG_SEL			SQP	LOOP_DIAG_CHSEL[3:0]			
MISO	0	0	0	0	DIAG_LEVEL	0	0	0	0	0	0	0	HIGH_LEVEL_DIAG_SEL			SQP	LOOP_DIAG_CHSEL[3:0]			

ID: 38

Type: RW

Read: 3800

Write: 0070

	POR	WSM	SSM	
[15]	0	0	0	DIAG_LEVEL: Diagnostic mode selector0: N/A - see description above 1: high level mode
[7:5]	000	000	000	HIGH_LEVEL_DIAG_SEL: Selection of high level squib/pyroswitch diagnostic Updated by SSM_RESET or SPI write 000: No diagnostic selected 001: VRCM CHECK 010: Leakage CHECK 011: Short Between Loops CHECK 100: not used 101: Squib/Pyroswitch resistance range CHECK 110: Squib/Pyroswitch resistance measurement 111: FET test
[4]	0	0	0	SQP: Squib/Pyroswitch pin select for all leakage diagnostic Updated by SSM_RESET or SPI write 0: SRx 1: SFx

[3:0]	0000	0000	0000	LOOP_DIAG_CHSEL[3:0]: Channel select - selects the channel and muxes for all squib/ pyroswitch diagnostic. Updated by SSM_RESET or SPI write 0000: Channel 0 0001: Channel 1 0010: Channel 2 0011: Channel 3 0100: Channel 4 0101: Channel 5 0110: Channel 6 0111; Channel 7 1100 - 1111: None Selected

DIAGCTRL_x (x=A, B, C, D)

ADC x control command registers

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	ADCREQ_X[6:0]						
MISO	NEWDATA_X	0	0	ADCREQ_X[6:0]							ADCRES_X[9:0]									

ID: 3A (DIAGCTRL_A), 3B (DIAGCTRL_B), 3C (DIAGCTRL_C), 3D (DIAGCTRL_D)

Type: RW

Read: 3A00 (DIAGCTRL_A), 3B00 (DIAGCTRL_B), 3C00 (DIAGCTRL_C), 3D00 (DIAGCTRL_D)

Write: 0074 (DIAGCTRL_A), 0076 (DIAGCTRL_B), 0078 (DIAGCTRL_C), 007A (DIAGCTRL_D)

	POR	WSM	SSM	
[19]	0	0	0	NEWDATA_X: New data available from convertion Updated by SSM_RESET or ADC state machine 0: cleared on read 1: convertion finished

[16:10]	0x00	0x00	0x00	ADCREQ_X[6:0]: ADC Request select command Updated by SSM_RESET or SPI write to DIAGCTRL_x measurement 0x00: Unused 0x01: ADC ground reference 0x02: ADC full scale reference 0x06: Squib/Pyroswitch x resistance 0x07: Internal BG reference voltage (BGR) 0x08: Internal BG monitor voltage (BGM) 0x09: Vcore 0x0A: Temperature 0x22: Internal analog supply voltage (VINT) 0x23: Internal digital supply voltage (VDD) 0x25: VSYNC pin voltage 0x27: VSAT voltage 0x28; VCC voltage 0x2B: TEST pin voltage 0x32: RSU0 pin Voltage 0x33; RSU1 pin Voltage 0x34; RSU2 pin Voltage 0x35: RSU3 pin Voltage 0x36: SS0 pin voltage 0x37: SS1 pin voltage 0x38: SS2 pin voltage 0x39: SS3 pin voltage 0x3A: SS4 pin voltage 0x3B; SS5 pin voltage 0x3C: SS6 pin voltage 0x3D: SS7 pin voltage 0x46: SF0 0x47: SF1 0x48: SF2 0x49: SF3 0x4A: SF4 0x4B: SF5 0x4C: SF6 0x4D: SF7
[9:0]	0x000	0x000	0x000	ADCRES_X[9:0]: 10-bit ADC result value corresponding to ADCREQ_x request Updated by SSM_RESET or ADC state machine

RSCRx (x=0, 1, 2, 3)

PSI5 configuration register for channel x

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	BLOCK_CURR_IN_MSG	PERIOD_MEAS_DISABLE	X	TSxDIS	BLKTxSEL	PSI5FILT[3:0]				X	X	STS[3:0]			
MISO	0	0	0	0	X	BLOCK_CURR_IN_MSG	PERIOD_MEAS_DISABLE	X	TSxDIS	BLKTxSEL	PSI5FILT[3:0]				X	X	STS[3:0]			

ID: 4A (RSCR0), 4B (RSCR1), 4C (RSCR2), 4D (RSCR3)

Type: RW

Read: 4A00 (RSCR0), 4B00 (RSCR1), 0098 (RSCR2), 009A (RSCR3)

Write: 0094 (RSCR0), 0096 (RSCR1), 0098 (RSCR2), 009A (RSCR3)

	POR	WSM	SSM	
[14]	1	0	1	BLOCK_CURR_IN_MSG: Tracking enable of base and delta current during message transmission 0: Ibase tracking is enabled during blanking and after start bits recognition. Idelta tracking is disabled during blanking and enabled after start bits recognition. 1: Ibase tracking is enabled during blanking and disabled after start bits recognition. Idelta tracking is disabled during blanking and enabled after start bits recognition
[13]	0	0	0	PERIOD_MEAS_DISABLE: Disabling of start bits period measure to decode following bits 0: Period is measured 1: Period is not measured (default is used)
[11]	0	0	0	TSxDIS: Time slot control disable 0: Slot control enabled 1: Slot control disabled
[10]	0	0	0	BLKTxSEL: Blanking time selection 0: Blanking time = 5 ms 1: Blanking time = 10 ms
[9:6]	0010	0010	0010	PSI5FILT[3:0]:PSI5 filter time selection 189k: (16 + x) * T_{osc} 125k: (24 + x) * T_{osc} T_{osc} = 1/16 MHz

[3:0]	0000	0000	0000	STS[3:0]: Sensor Type Selection 0000: Synchronous PSI5, parity, 8-bit, 125k (P8P-500/3L) 0001: Synchronous PSI5, parity, 8-bit, 189k (P8P-500/3H) 0010: Synchronous PSI5, parity, 10-bit, 125k (P10P-500/3L) 0011: Synchronous PSI5, parity, 10-bit, 189k (P10P-500/3H) 0100: Synchronous PSI5, parity, 8-bit, 125k (P8P-500/3L) 0101: Synchronous PSI5, parity, 8-bit, 189k (P8P-500/4H) 0110: Synchronous PSI5, parity, 10-bit, 125k (P10P-500/3L) 0111: Synchronous PSI5, parity, 10-bit, 189k (P10P-500/4H) 1000: Do not use 1001: Do not use 1010: Do not use 1011: Do not use 1100: Asynchronous PSI5, parity, 8-bit, 125k (A8P-228/1L) 1101: Asynchronous PSI5, parity, 8-bit, 189k (A8P-228/1H) 1110: Asynchronous PSI5, parity, 10-bit, 125k (A10P-228/1L) 1111: Asynchronous PSI5, parity, 10-bit, 189k (A10P-228/1H)

RSCTRL

Remote sensor control register

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	CH3EN	SYNC3EN	CH2EN	SYNC2EN	CH1EN	SYNC1EN	CH0EN	SYNC0EN
MISO	0	0	0	0	0	0	0	0	0	0	0	0	CH3EN	SYNC3EN	CH2EN	SYNC2EN	CH1EN	SYNC1EN	CH0EN	SYNC0EN

ID: 4E

Type: R/W

Read: 4E00

Write: 009C

	POR	WSM	SSM	
[7, 5, 3, 1]	0	0	0	CHxEN: Channel x output enable Updated by SSM_RESET or SPI write 0: Off 1: On
[6, 4, 2, 0]	0	0	0	SYNCxEN: Channel x sync pulse enable 0: Off 1: On

ARM_STATE

Arming signals register

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI					X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FEN2	FEN1	FENL	0

ID: 6A

Type: R

Read: 6A00

Write: -

	POR	WSM	SSM	
[3,2]	-	-	-	FENx: State of arming signals Updated per Safing Engine output logic diagram in case of internal safing engine otherwise is the echo of ARMx pins
[1]	-	-	-	FENL: State of external arming control signal (used to arm low side of deployment loops only in case of external arming) Updated based on pin state

LOOP_MATRIX_ARMx (x=1, 2)

Assignment of ARMx to specific loops

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	FENx_L7	FENx_L6	FENx_L5	FENx_L4	FENx_L3	FENx_L2	FENx_L1	FENx_L0
MISO	0	0	0	0	0	0	0	0	0	0	0	0	FENx_L7	FENx_L6	FENx_L5	FENx_L4	FENx_L3	FENx_L2	FENx_L1	FENx_L0

ID: 6E (LOOP_MATRIX_FEN1), 6F (LOOP_MATRIX_FEN2)

Type: RW

Read: 6E00 (LOOP_MATRIX_FEN1), 6F00 (LOOP_MATRIX_FEN2)

Write: 00DC (LOOP_MATRIX_FEN1), 00DE (LOOP_MATRIX_FEN2)

	POR	WSM	SSM	
[7:0]	0	0	0	FENx_Ly: Configures FENx for Loop_y Updated by SSM_RESET or SPI write while in DIAG state 0: FENx signal is not associated with Loop_y 1: FENx signal is associated with Loop_y

6.5 Remote sensor SPI register map

The Remote sensor SPI interface consists of twelve 32-bit read registers (one for each logical channel) to allow access to decoded sensor data and fault registers. The registers are addressed by the read register ID and the global ID bit.

The L9679E checks the validity of the received RID field in the MOSI_RS frame. Should an SPI read command be received containing an unused RID address, the command will be discarded and the ERR_RID bit will be flagged in the current GSW.

Table 9. Remote sensor SPI register map

GID	RID / WID							Hex	R/W	Name	Description	Operating State		
												Init	Diag	Safing
0	1	0	1	0	0	0	0	0x50	R	RSDR0				
0	1	0	1	0	0	0	1	0x51	R	RSDR1				
0	1	0	1	0	0	1	0	0x52	R	RSDR2				
0	1	0	1	0	0	1	1	0x53	R	RSDR3				
0	1	0	1	0	1	0	0	0x54	R	RSDR4				
0	1	0	1	0	1	0	1	0x55	R	RSDR5	Remote sensor data/status registers			
0	1	0	1	0	1	1	0	0x56	R	RSDR6	(PSI-5)			
0	1	0	1	0	1	1	1	0x57	R	RSDR7				
0	1	0	1	1	0	0	0	0x58	R	RSDR8				
0	1	0	1	1	0	0	1	0x59	R	RSDR9				
0	1	0	1	1	0	1	0	0x5A	R	RSDR10				
0	1	0	1	1	0	1	1	0x5B	R	RSDR11				
0	1	0	1	1	1	0	0	0x5C	R	RSTHR0_L				
0	1	0	1	1	1	0	1	0x5D	R	RSTHR1_L	Remote sensor 1 registers			
0	1	0	1	1	1	1	0	0x5E	R	RSTHR2_L	(PSI-5)			
0	1	0	1	1	1	1	1	0x5F	R	RSTHR3_L				
0	1	1	0	0	0	0	0	0x60						
0	1	1	0	0	0	0	1	0x61						
0	1	1	0	0	0	1	0	0x62						
0	1	1	0	0	0	1	1	0x63						
0	1	1	0	1	0	1	0	0x6A						
1	1	1	1	1	1	1	1	0xFF						

6.6 Remote sensor SPI tables

A summary of all the registers contained within the remote sensor SPI map is shown below and is referenced throughout the specification they apply to. The SPI register tables also specify the effect of the internal reset signals assertion on each bit field.

Note: The symbol '-' is used to indicate that the register is not affected by the relevant reset signal.

6.6.1 Remote sensor SPI global status word

The remote sensor SPI contains an 11-bit word that returns global status information. The Global Status Word (GSW) of the remote sensor SPI is the most significant 11 bits of MISO_RS data.

Table 10. GSW - Remote sensor SPI global status word

MISO_RS	GSW	Name	POR	WSM	SSM	Description
31	10	SPIFLT	0	0	0	SPI Fault, set if previous SPI frame had wrong parity check or wrong number of bits, cleared upon read 0: No fault 1: Fault
30	9	0	0	0	0	Unused
29	8	RSFLT	0	0	0	Remote sensor Interface Fault Present, logical OR of the corresponding FLTBIT bits in RSDRx (bit 15) for all faults but NODATA 0: All the RSDRx-FLTBIT bits are 0 1: At least one of the RSDRx-FLTBIT bits is 1 and the associated fault code is different from NODATA
28	7	0	0	0	0	Unused
27	6	0	0	0	0	Unused
26	5	0	0	0	0	Unused
25	4	0	0	0	0	Unused
24	3	0	0	0	0	Unused
23	2	0	0	0	0	Unused
22	1	0	0	0	0	Unused
21	0	ERR_RID	0	0	0	Read address received in the actual SPI frame is unused so data in the response is don't care 0: No Error 1: Error

RSDRx(x=0 to 11) @FLT = 0

Remote sensor data/fault registers ch_x (x=0 to 3) slot_x (x=1 to 3)

Note: The value in Bit15 (FLT) will re-define the use of the other bits, hence the tables below are divided into two groups

ch0 slot 1 (RSDR0); ch1 slot 1 (RSDR1); ch2 slot 1 (RSDR2); ch3 slot 1 (RSDR3);

ch0 slot 2 (RSDR4); ch1 slot 2 (RSDR5); ch2 slot 2 (RSDR6); ch 3 slot 2 (RSDR7)

ch0 slot 3 (RSDR8); ch1 slot 3 (RSDR9); ch2 slot 3 (RSDR10); ch3, slot 3 (RSDR11)

Note: Bit 15 = 0 NO FAULT Condition

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI_RS					X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO_RS (PSI5)	CRC			0	FLT=0	On/Off	LCID [3:0]				DATA [9:0]									

ID: 50 (RSDR0), 51 (RSDR1), 52 (RSDR2), 53 (RSDR3), 54 (RSDR4), 55 (RSDR5), 56 (RSDR6), 57 (RSDR6), 58 (RSDR8), 59 (RSDR9), 5A (RSDR10), 5B (RSDR11)

Type: R

Read: 5000 (RSDR0), 5100 (RSDR1), 5200 (RSDR2), 5300 (RSDR3), 5400 (RSDR4), 5500 (RSDR5), 5600 (RSDR6), 5700 (RSDR7), 5800 (RSDR8), 5900 (RSDR9), 5A00 (RSDR10), 5B00 (RSDR11)

Write: -

	POR	WSM	SSM	
[19:17]	-	-	-	CRC[2:0]: CRC based on bits [16:0] Updated based on bits [16:0]
[15]	1	1	1	FLT: Fault Status - Depending on Fault Status, the DATA bits are defined differently Cleared when all of the following bits are '0': STG, STB, CURRENT_HI, OPENDET, RSTEMP, INVALID, SLOT_ERROR, NODATA Set when any of the following bits are '1': STG, STB, CURRENT_HI, OPENDET, RSTEMP, INVALID, SLOT_ERROR, NODATA 0: No fault 1: Fault
[14]	0	0	0	On/Off: Channel On/Off Status Cleared by SSM_RESET or when channel is commanded OFF via SPI RSCTRL or when the STG bit is set or the RSTEMP bit is set Set when channel is commanded ON by SPI RSCTRL 0 Off 1 On

[13:10]	-	-	-	LCID[3:0]: Logical Channel ID Updated based on SPI read request 0000: RSU0 SLOT1 0001: RSU0 SLOT2 0010: RSU0 SLOT3 0100: RSU1 SLOT1 0101: RSU1 SLOT2 0110: RSU1 SLOT3 1000: RSU2 SLOT1 1001: RSU2 SLOT2 1010: RSU2 SLOT3 1100: RSU3 SLOT1 1101: RSU3 SLOT2 1110: RSU3 SLOT3
[9:0]	$000	$000	$000	DATA[9:0]: 10-bit data from Manchester decoder Cleared by SSM_RESET or SPI read or when channel is commanded OFF via SPI RSCTRL updated when a valid PSI5 frame is received

RSDRx (x=0 to 11) @FLT=1

Remote sensor data/fault registers ch_x (x=0 to 3) slot_x (x=1 to 3)

ch0 slot 1 (RSDR0); ch1 slot 1 (RSDR1); ch2 slot 1 (RSDR2); ch3 slot 1 (RSDR3);
ch0 slot 2 (RSDR4); ch1 slot 2 (RSDR5); ch2 slot 2 (RSDR6); ch 3 slot 2 (RSDR7)
ch0 slot 3 (RSDR8); ch1 slot 3 (RSDR9); ch2 slot 3 (RSDR10); ch3, slot 3 (RSDR11)

Note: Bit 15 = 1 FAULTED condition

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOS_RSI	'				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO_RS	CRC			X	FLT =1	On/Off	LCID [3:0]				STG	STB	CURRENT_HI	OPENDET	RSTEMP	INVALID	NODATA	SLOT_ERROR	X	X

ID: 50 (RSDR0), 51 (RSDR1), 52 (RSDR2), 53 (RSDR3), 54 (RSDR4), 55 (RSDR5), 56 (RSDR6), 57 (RSDR6), 58 (RSDR8), 59 (RSDR9), 5A (RSDR10), 5B (RSDR11)

Type: R

Read: 5000 (RSDR0), 5100 (RSDR1), 5200 (RSDR2), 5300 (RSDR3), 5400 (RSDR4), 5500 (RSDR5), 5600 (RSDR6), 5700 (RSDR7), 5800 (RSDR8), 5900 (RSDR9), 5A00 (RSDR10), 5B00 (RSDR11)

Write: -

	POR	WSM	SSM	
[19:17]	-	-	-	CRC[2:0]: CRC based on bits [16:0] Updated based on bits [16:0]
[15]	1	1	1	FLT=1: Fault Status Cleared when all of the following bits are '0': STG, STB, CURRENT_HI, OPENDET, RSTEMP, NODATA, INVALID, SLOT ERROR, PULSE OVERFLOW ERROR Set when any of the following bits are '1': STG, STB, CURRENT_HI, OPENDET, RSTEMP, NODATA, INVALID, SLOT ERROR, PULSE OVERFLOW ERROR 0: No fault 1: Fault
[14]	0	0	0	On/Off: Channel on/off status Cleared by SSM_RESET or when channel is commanded OFF via SPI RSCTRL or when the STG bit is set or the RSTEMP bit is set Set when channel is commanded ON by SPI RSCTRL 0: Off 1: On

[13:10]	0000	0000	0000	LCID[0:3]: Logical Channel ID Updated based on SPI read request 0000: RSU0 SLOT1 0001: RSU0 SLOT2 0010: RSU0 SLOT3 0100: RSU1 SLOT1 0101: RSU1 SLOT2 0110: RSU1 SLOT3 1000: RSU2 SLOT1 1001: RSU2 SLOT2 1010: RSU2 SLOT3 1100: RSU3 SLOT1 1101: RSU3 SLOT2 1110: RSU3 SLOT3
[9]	0	0	0	STG: Short to ground (in current limit condition) Cleared by SSM_RESET or when channel is commanded OFF via SPI RSCTRL 0: No fault 1: Fault
[8]	0	0	0	STB: Short to Battery Cleared by SSM_RESET or SPI read or when channel is commanded OFF via SPI RSCTRL Not cleared by channel OFF caused by STG or RSTEMP Set when channel voltage exceeds SATBUCK for a time greater than T_{STBTH} 0: No fault 1: Fault
[7]	0	0	0	CURRENT_HI: Current high Cleared by SSM_RESET or SPI read or when channel is commanded OFF via SPI RSCTRL Set when channel current exceeds ITHGND for a time determined by an up/down counter 0: No fault 1: Fault
[6]	0	0	0	OPENDET: Open sensor detected Cleared by SSM_RESET or SPI read or when channel is commanded OFF via SPI RSCTRL Set when channel current exceeds ITHOPEN for a time determined by an up/down counter 0: No fault 1: Fault
[5]	0	0	0	RSTEMP: Over temperature detected Cleared by SSM_RESET or when channel is commanded OFF via SPI RSCTRL Set when over-temp condition is detected 0: No fault 1: Fault
[4]	0	0	0	INVALID: Invalid Data

				Cleared by SSM_RESET or SPI read or when channel is commanded OFF via SPI RSCTRL or if one of the following is set: STG, STB, CURRENT_HI, OPEN_DET, RSTEMP, SLOT ERROR (PSI5) or if a new valid data is received. Set in PSI5 configuration when two valid start bits are received and a Manchester error (# of bits, bit timing) or parity error is detected 0: No fault 1: Fault
[3]	1	1	1	NODATA: No Data in buffer Cleared when a valid PSI5/WSS frame is received or if one of the following is set: STG, STB, CURRENT_HI, OPEN_DET, RSTEMP, SLOT ERROR, PULSE OVERFLOW ERROR, INVALID Set upon SPI read of RSDRx and none of the following bits are set: STG, STB, CURRENT_HI, OPEN_DET, RSTEMP, SLOT ERROR, PULSE OVERFLOW ERROR, INVALID 0: No fault 1: Fault
[2]	0	0	0	SLOT ERROR: Slot error fault (valid only for PSI5 sensors) Cleared by SSM_RESET or SPI read or when channel is commanded OFF via SPI RSCTRL or if one of the following is set: STG, STB, CURRENT_HI, OPEN_DET, RSTEMP or if a new valid data is received Set in case of slot control enabled and frame not completely inside slot or more than one frame inside the slot 0: No fault 1: Fault

RSTHRx_L

Remote sensor x current registers

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI_RS	-				x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
MISO_RS	DELTA 1ST TOP [9:0]										BASE CURRENT [9:0]									

ID: **ID:** 5C (RSTHR0_L), 5D (RSTHR1_L), 5E (RSTHR2_L), 5F (RSTHR3_L)

Type: **Type:** R

Read: **Read:** 5C00 (RSTHR0_L), 5D00 (RSTHR1_L), 5E00 (RSTHR2_L), 5F00 (RSTHR3_L)

Write: -

	POR	WSM	SSM	
[19:10]	$82	$82	$82	DELTA 1ST TOP [9:0]: Delta measured by internal converter respect to base current (93.75 µA ±9% each LSB) to get top low threshold Low threshold = base current+(DELTA_1ST_TOP)
[9:0]	$A1	$A1	$A1	BASE CURRENT [9:0]: Base current measured by internal converter (93.75 µA ±9% each LSB).

7 Deployment drivers

The squib/pyroswitch deployment block consists of 8 independent high-side drivers and 8 independent low-side drivers. Squib/Pyroswitch deployment logic requires a deploy command received through SPI communications and proper FENx input pins assessment. Both conditions must exist in order for the deployment to occur. Once a deployment is initiated, it can only be terminated by an SSM_RESET event.

L9679E allows all 8 squib/pyroswitch loops to be deployed at the same time or in any other possible timing sequence. Deployment drivers are capable of granting a successful deployment also in case of short to ground on low-side circuit (SRx pins). Firing voltage capability across high-side circuit is maximum 25 V on high side, and low-side drivers account for a maximum series total resistance of R_{DSON_HSLS} Ω. Each loop is granted for a minimum number of 15 deployments, under all normal operating conditions and with a deployment repetition time higher than 10s. Both the high- and the low-side FET drivers are equipped with passive gate turn-off circuitries to guarantee the FETs are kept in off state also when the device is unpowered or during power-up/down transients.

7.1 Control logic

A block diagram representing the deployment driver logic is shown below. Deployment driver logic features include:

- Deploy command logic
- Deployment current selection
- Deployment current monitoring and deploy success feedback
- Diagnostic control and feedback

Figure 9. Deployment driver control blocks

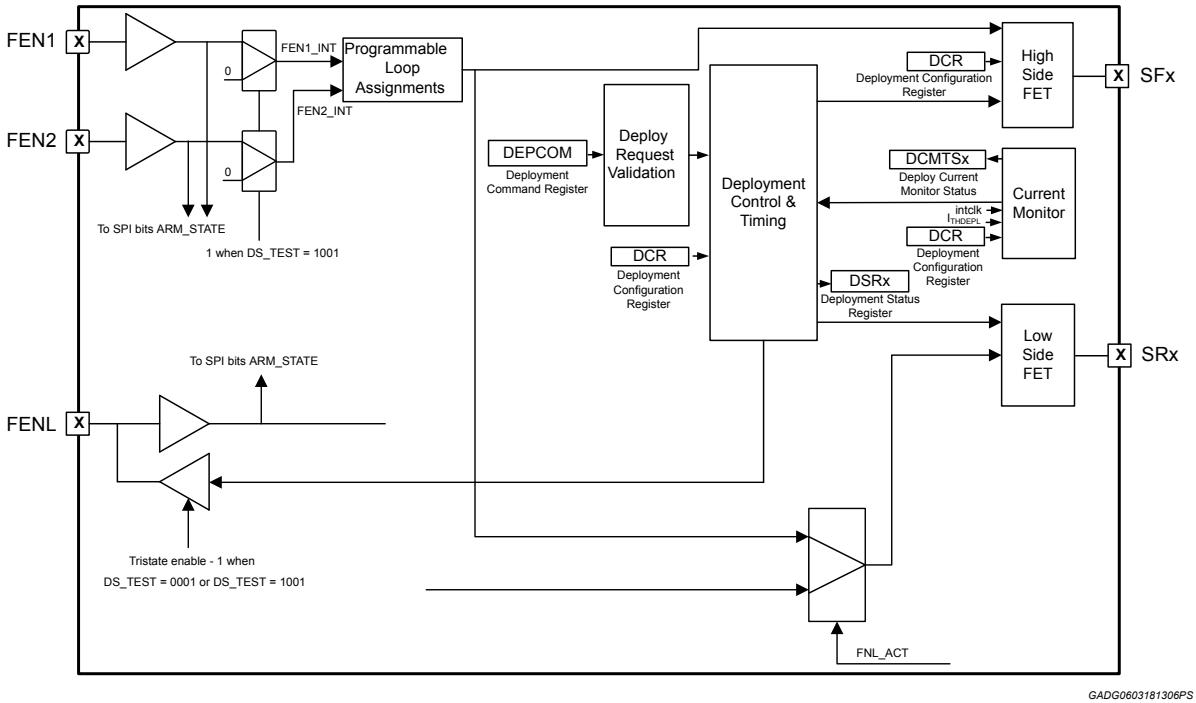


Figure 10. **Deployment driver control logic – Enable signals**

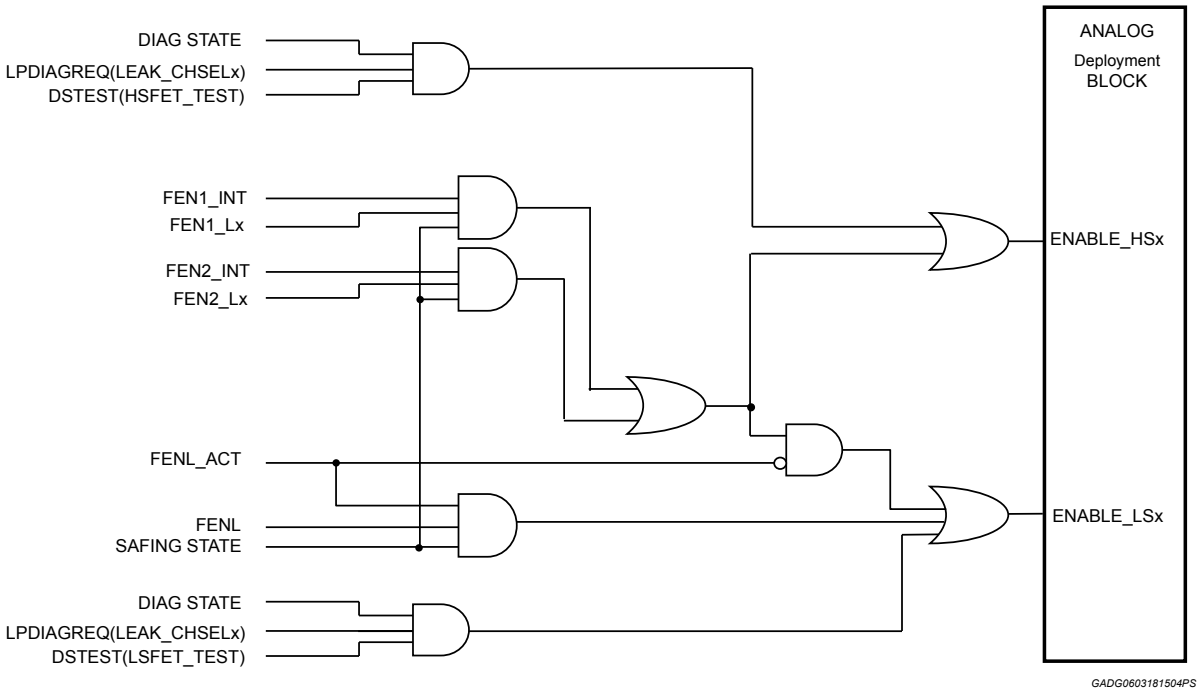
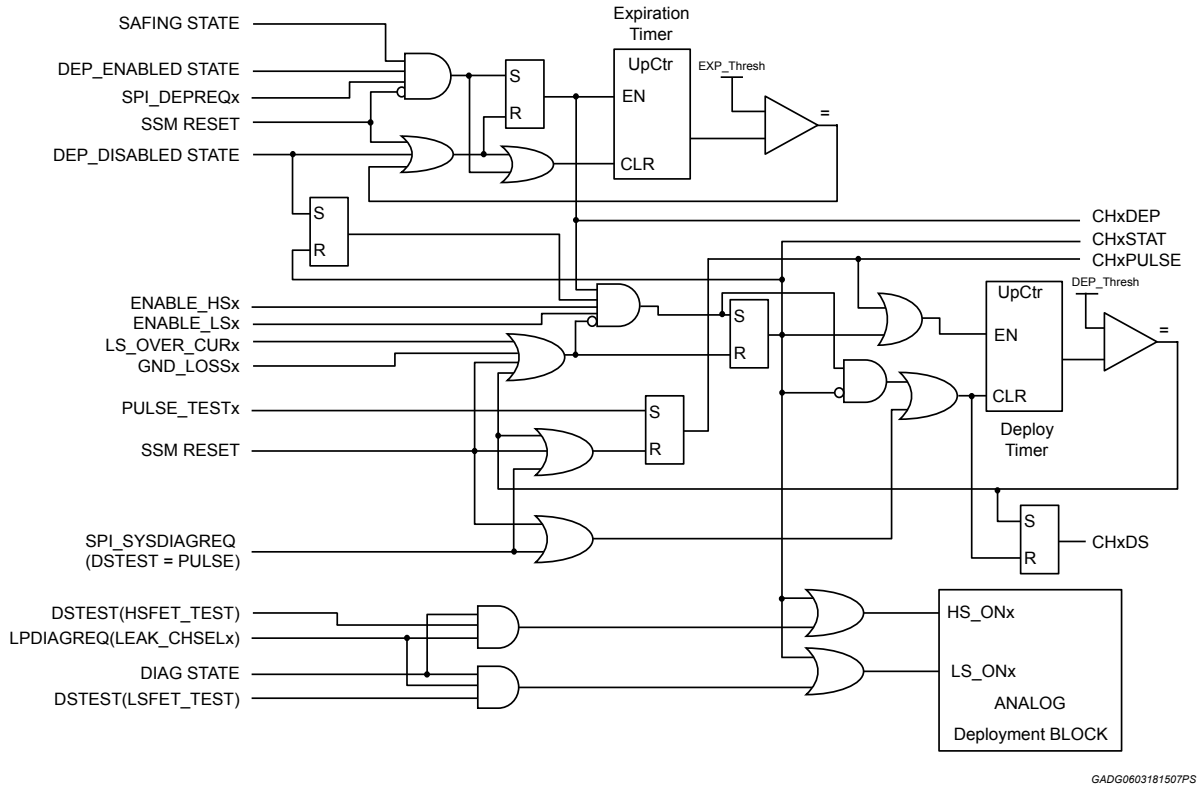
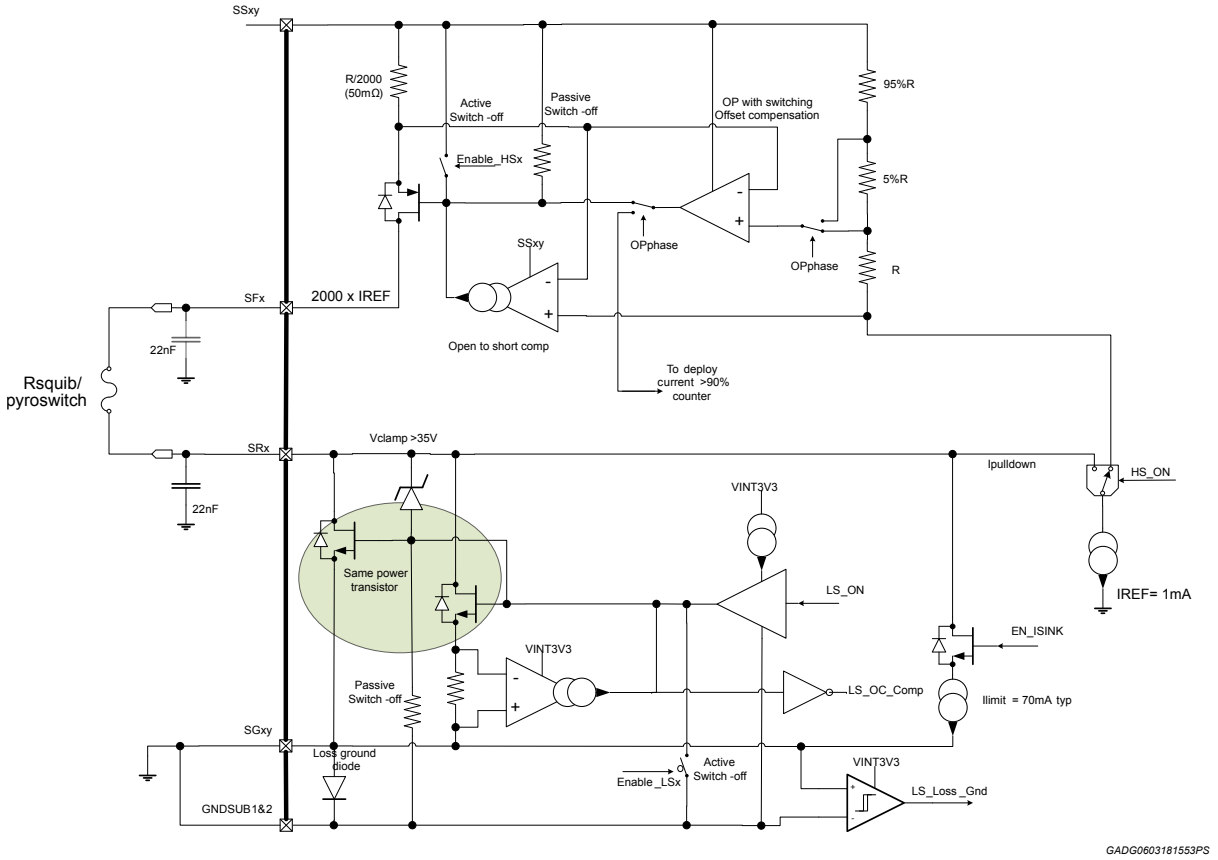


Figure 11. **Deployment driver control logic - Turn-on signals**



The high level block diagram for the deployment drivers is shown below:

Figure 12. **Analog deployment block diagram**



7.1.1 Safe operating area vs deployment current profiles

Deployment current is programmed for each channel using the Deploy Configuration Register (DCRx) shown in DCR_x(x=0, 2, 4, 6) and DCR_x(x=1, 3, 5, 7).

In the same register the Deploy Time Selection allows the device to deploy for a time up to 4.032 ms.

In order to prevent device damage, a constraint on squib/pyroswitch supply voltage versus maximum T_j at the deployment start shall be specified as following:

Squib/Pyroswitch Deploy current profile = 1.2 A / 2 ms (DCR_Deploy_Time ≤ 34):

6 V ≤ V_SSxy ≤ 22.75 V with -40 °C ≤ T_j_start ≤ 130 °C;

6 V ≤ V_SSxy ≤ 21.5 V with -40 °C ≤ T_j_start ≤ 150 °C;

Squib/Pyroswitch Deploy current profile = 1.75 A / 700 µs (DCR_Deploy_Time ≤ 13):

9 V ≤ V_SSxy ≤ 25 V with -40 °C ≤ Tj_start ≤ 115 °C;

9 V ≤ V_SSxy ≤ 23.75 V with -40 °C ≤ Tj_start ≤ 130 °C;

9 V ≤ V_SSxy ≤ 22.5 V with -40 °C ≤ Tj_start ≤ 150 °C;

Squib/Pyroswitch Deploy current profile = 1.75 A / 500 µs (DCR_Deploy_Time ≤ 10):

9 V ≤ V_SSxy ≤ 25 V with -40 °C ≤ Tj_start ≤ 150 °C;

Squib/Pyroswitch Deploy current profile = 1.2 A / 3.2 ms (DCR_Deploy_Time ≤ 54):

6 V ≤ V_SSxy ≤ 20.1 V with -40 °C ≤ Tj_start ≤ 130 °C;

6 V ≤ V_SSxy ≤ 19.3 V with -40 °C ≤ Tj_start ≤ 150 °C;

Squib/Pyroswitch Deploy current profile = 1.75 A / 2 ms (DCR_Deploy_Time ≤ 34):

6 V ≤ V_SSxy ≤ 16.7 V with -40°C ≤ Tj_start ≤ 130°C;

6V ≤ V_SSxy ≤ 16V with -40°C ≤ Tj_start ≤ 150°C;

Squib/Pyroswitch Deploy current profile = 1.75 A / 3.2 ms (DCR_Deploy_Time ≤ 54):

6 V ≤ V_SSxy ≤ 14.7 V with -40 °C ≤ Tj_start ≤ 130 °C;

6 V ≤ V_SSxy ≤ 13.9 V with -40 °C ≤ Tj_start ≤ 150 °C;

These requirements are valid considering also the case where all loops are shorted to ground during deployment (SFx = 0 V or SRx = 0 V).

7.1.2 Deploy command expiration timer

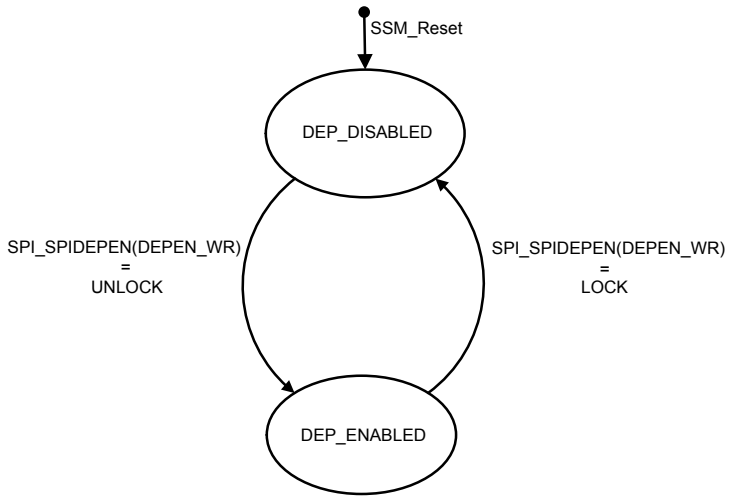
Deploy commands are received for all channels using SPI communications. Once a deploy command is received, it will remain valid for a specified time period selected in the Deploy Configuration Register (DCRx). The deploy status and deploy expiration timer can be read through the Deploy Status Register (DSRx). The deploy expiration timer is selectable via 2 bits and the maximum programmable time is 500 ms nominal.

7.1.3 Deployment control flow

Deployment control logic requires the following conditions to be true to successfully operate a deployment:

- POR = 0
- SSM to be in Safing State
- A valid arming condition by FENx signals to be set
- Channel-specific deploy command request bits to be set via SPI in the Deploy command Register (DEPCOM)
- A global deployment state has to be active, as described in the following figure.

Figure 13. Global SPI deployment enable state diagram



In case a multiple deployment request is needed, i.e. deploying the same channel in sequence, a toggle on DEP_DISABLED has to be performed and a new DEPCOM command on the same channel has to be sent.

The SPI DEPCOM command is ignored if the device is in the DEP_DISABLED state and the deploy command is not set. While in DEP_ENABLED state, the following functionalities that could be active are forced to their reset state:

- All squib/pyroswitch diagnostic current or voltage sources
- All squib/pyroswitch and ADC diagnostic MUX settings, state machine, etc.

The SPI_LOCK and SPI_UNLOCK signals are available in the SPIDEPEN command:

The arming valid condition is assessed by using the 3 arming discrete input pins FEN1, FEN2 and FENL. All of these three pins are active high. The device allows two configurations:

- Config 1 (default): FENL is not used; FEN1 and FEN2 are enablers for any or all the loops, each input controlling both HS and LS of those loops
- Config 2: FENL is used and enables all LSs; FEN1 and FEN2 enable for any or all the loops, this time controlling only HSs

FEN1/2 input pins are assigned to the desired channels by means of the programmable loop matrix.

Deploy commands in the Deploy Command Register (DEPCOM) are channel specific.

Deployment requires a valid arming condition from FENx signals to be set any time before, during or after the specific sequence of deploy commands is received. It is feasible for a deploy command to be received without a valid arming condition from the FENx being set. In this case, the deploy command will be terminated according to the Section 7.1.2: Deploy command expiration timer

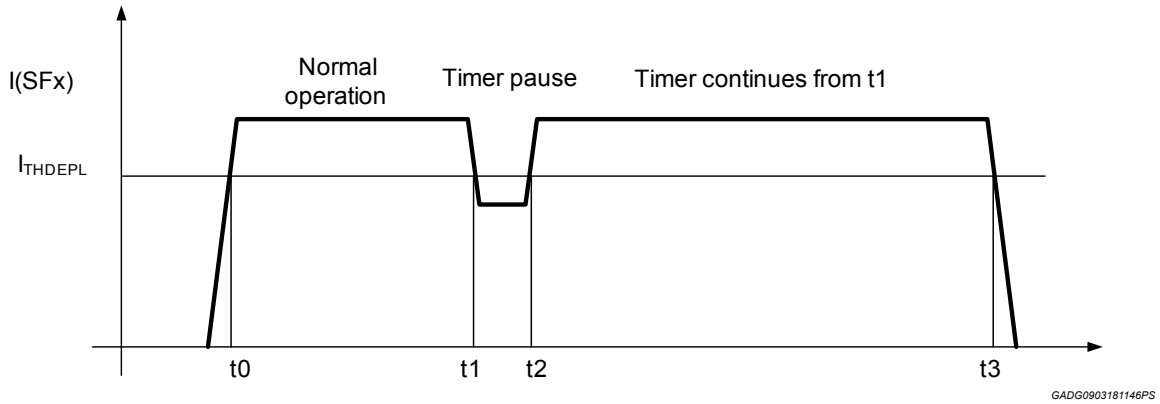
Arming signals coming from FENx pins are not stretched by the device so active state of these pins must be kept during the entire duration of the deployment event to complete it successfully.

7.1.4 Deployment current monitoring

A current comparator is used to indicate when the output current from the HSD, SFx, exceeds the deployment current threshold, I_{THDEPL}. The timer signal remains active and increments while the current meets the programmed deploy current as set in the Deploy Configuration Register. The deployment current counter value is stored in the Deploy Current Monitor Timer Register XY (DCMTSxy). There is a unique timer register for each channel.

If the deploy current falls below the specified current threshold momentarily and recovers, the deployment current counter will pause during the drop-out and continue once the current exceeds the threshold. The deployment current counter will not be reset by the presence or absence of current in the deployment channel.

Figure 14. Current monitor counter behavior



The deploy current counter is reset to $0000 as soon as a toggle on DEP_DISABLED is performed and a new DEPCOM command on the same channel is received.

7.1.5 Deployment success

Deploy success flag is set when the deploy timer elapses. This bit (CHxDS) is contained in the Deploy Status Register. Within the Global Status Word register (GSW), a single bit (DEPOK) is also set once any of the 8 deployment channels sets a deploy success flag.

7.2 Deployment voltage

One deployment voltage source pin is used for adjacent channels (e.g. SS23 for channels 2 and 3). These pins are directly connected to the high side drivers for each channel.

7.3 Deployment driver protections

7.3.1 Delayed low side deactivation

To control voltage spikes at the squib/pyroswitch pins during drivers deactivation at the end of a deployment, the low/side driver is switched off after $T_{DEL\_SD\_LS}$ delay time with respect to the high side deactivation.

7.3.2 Low-side voltage clamp

The low-side driver is protected against overvoltage at the SRx pins by means of a clamping structure as shown in Figure 12. Analog deployment block diagram. When the low-side driver is turned off, voltage transients at the SRx pin may be caused by squib/pyroswitch inductance. In this case a low-side FET drain to gate clamp will reactivate the low-side FET allowing for residual inductance current recirculation, thus preventing potential low-side FET damage by overvoltage.

7.3.3 Short-to-battery

The low-side driver is equipped with current limitation and overcurrent protection circuitry. In case of short-to-battery at the squib/pyroswitch pins, the shortcircuit current is limited by the low-side driver to I_{LIMSRx}. If this condition lasts for longer than $T_{FLT\_ILIM\_LS}$ deglitch filter time then the low- and high-side drivers will be switched off and latched in this state until a new deployment is commanded after SPI_DEPEN is retriggered.

7.3.4 Short-to-ground

The squib/pyroswitch driver is designed to stand a short-to-ground at the squib/pyroswitch pins during deployment. In particular, the current flowing through the short circuit is limited by the high-side driver (deployment current) and the high-side FET is sized to handle the related energy.

In case the short-to-ground during deployment occurs after an open circuit, a protection against damage is also available. The high-side current regulator would have normally reacted to the open circuit by increasing the Vgs of the high-side FET. Thanks to a dedicated fast comparator detecting the open condition, the driver is able to discharge the FET gate quickly in order to reduce current overshoot and prevent potential driver damage when the short-to-ground occurs.

7.3.5 Intermittent open squib/pyroswitch

A dedicated protection is also available in case of intermittent open load during deployment. In this case, if load is restored after an open circuit, due to slow reaction of the high-side current regulation loop, the current through the squib/pyroswitch is limited only to I_{LIMSRx} by the low-side driver. If this condition lasts for longer than $T_{FLT\_OS\_LS}$ then the high side is turned off for $T_{OFF\_OS\_HS}$ and then reactivated. By this feature, intermittent open squib/pyroswitch and short-to-battery faults may be distinguished and handled properly by the drivers.

7.4 Diagnostics

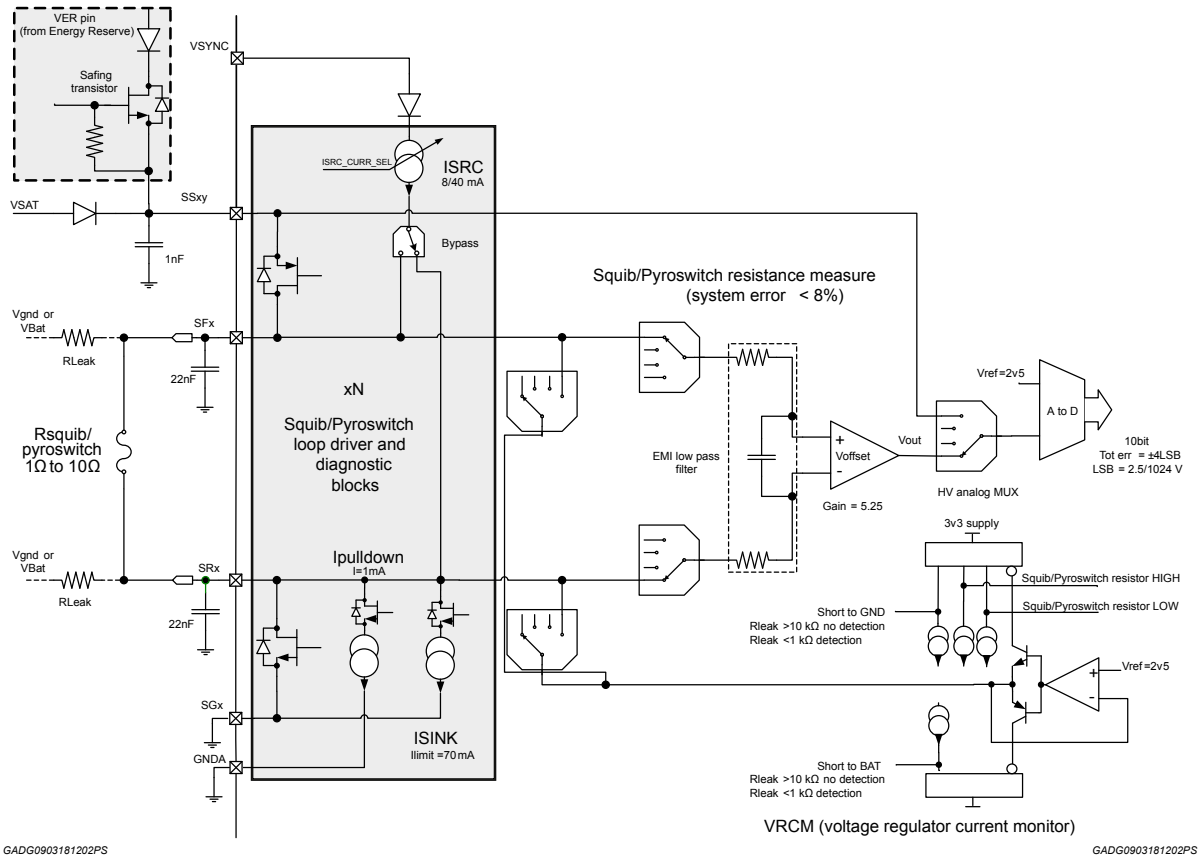
The L9679E provides the following diagnostic feedback for all deployment channels:

- High-voltage leakage test for oxide isolation check on SFx and SRx
- Leakage to battery and ground on both SFx and SRx pins with or without a squib/pyroswitch
- Short between loops diagnostics
- Squib/Pyroswitch resistance measurement with leakage cancellation and selectable range (10/50 Ω)
- High squib/pyroswitch resistance with range from 500 Ω to 2000 Ω
- SSxy, SFx voltage status
- High- and low-side FET diagnostics
- Loss of ground return diagnostics
- High-side safing FET diagnostics

The above diagnostic results are processed through a 10-bit analog-to-digital algorithmic converter. These tests can be addressed in two different ways, with a high-level approach or a low-level one. The main difference between the two approaches is that with the low-level approach the user is allowed to precisely control the diagnostic circuitry, also deciding the proper timings involved in the different tests. On the other hand, the high-level approach is an automatic way of getting diagnostic results for which an internal state machine is taking care of instructions and timings (reduced number of SPI frames required to run the diagnostic).

The following figure shows the block diagram of the squib/pyroswitch diagnostics.

Figure 15. Deployment loop diagnostics



The leakage diagnostic includes short-to-battery, short-to-ground and shorts between loops. The test is applied to each SFx and SRx pin so shorts can be detected regardless of the resistance between the squib/pyroswitch pins.

7.4.1 Low-level diagnostic approach

In this approach, each of the test steps described in the sections below requires user intervention by issuing the proper SPI command.

High-voltage leakage test for oxide isolation check

This test is mandatory to address possible leakages that could not be experienced at low voltages on SFx or SRx pins. The I_{source} current generator (ISRC) is enabled on the chosen SFx pin. To confirm that the SFx pin has then reached a suitable voltage level, a dedicated ADC measurement on the SFx pin can be requested. Once this test is performed, a leakage test on SFx and SRx pins can be issued to double check possible leakages.

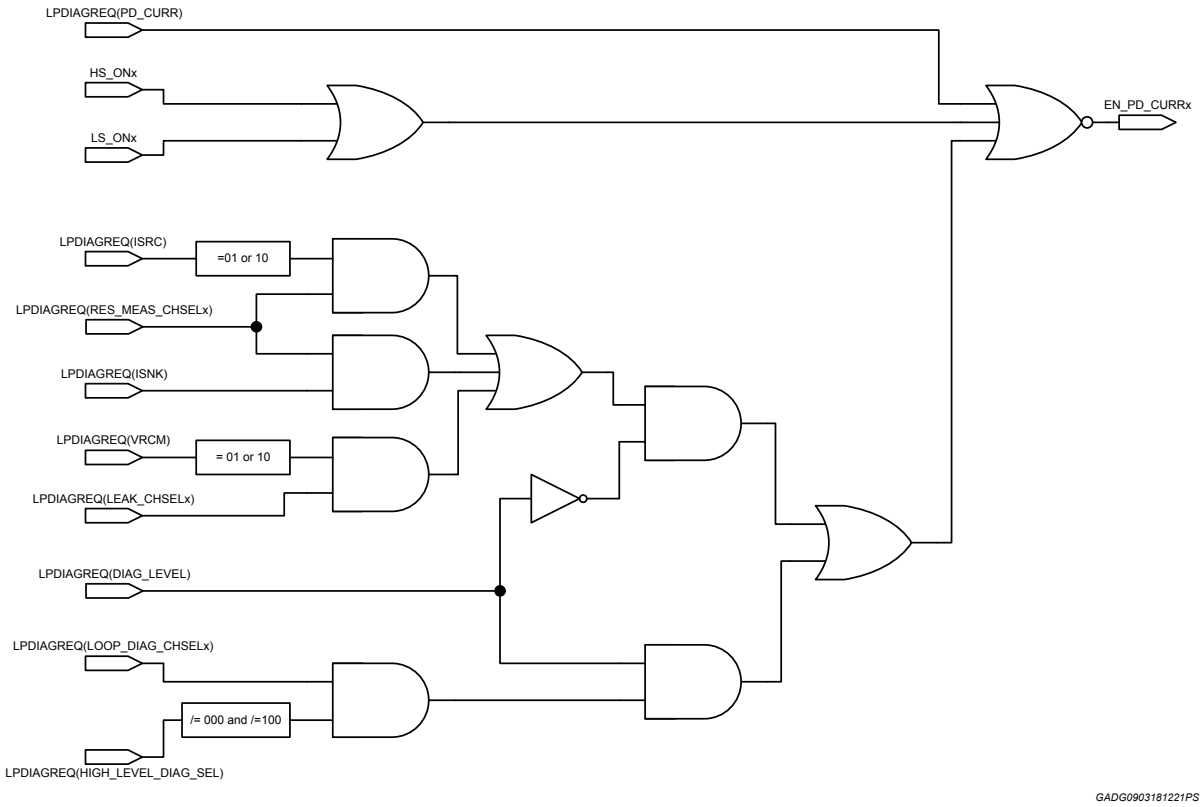
Leakage-to-battery/Ground diagnostics

Prior to the real test, the voltage regulator current monitor block (VRCM) has to be tested and validated. The validation of VRCM goes into verifying both the short-to-battery and short-to-ground flags.

The I_{source} current generator (ISRC) is first connected to the SFx pin to raise its voltage to VSYNC. Then, the VRCM is enabled and connected to the selected SFx pin. The I_{sink} current limited switch (ISNK) is turned off, as well as the pull-down current generator. If the VRCM block works properly, the short to battery flag would be asserted.

Then, the I_{sink} current limited switch (ISNK) is connected to the SRx pin, the VRCM is enabled and connected to the selected SRx pin. The I_{source} current generator (ISRC) is turned off, as well as the pull-down current generator. If the VRCM block works properly, the short to ground flag would be asserted.

Figure 16. SRx pull-down enable logic



Once the VRCM block is validated, the real leakage tests can be performed. ISRC and ISNK currents have to be kept switched off. The VRCM shall be connected to the desired pin (either SFx or SRx pins); by doing this, also the pull-down current on the selected SRx pin is automatically deactivated. During the test, if no leakage is present the voltage on the selected SFx or SRx pin will be forced by the VRCM to the VREF level and no current is detected or sourced by the VRCM. If there is a leakage to ground or battery, the VRCM will sink or source current trying to maintain VREF. Two current comparators, ISTB and ISTG, will detect the abnormal current flow and the relative flags will be given in the LPDIAGSTAT. These flags are not latched and report the real time status of the relevant comparators in case of low-level leakage diagnostic test. Voltage conversion is not required to have these flags updated.. In LPDIAGSTAT register are also reported the channel and the pin (SFx or SRx) under test, respectively with LEAK_CHSEL and SQP bit fields.

The pull-down currents on the other SRx pins are still active. Therefore, the leakage test that would show a leakage to ground may depend on a real leakage on the pin under test or on a short between loops.

Short between loops diagnostics

In case the previous test has reported a leakage to ground fault, the short between loops diagnostics shall be run. The same procedure is followed as described for normal leakage tests except the fact that in this case all the pull-down current generators have to be deactivated (not only the one for the pin under test), by means of the PD_CURR bit in the Diagnostic Request Register (LPDIAGREQ). If a leakage or ground fault is not present, then the channel under test has a short to another squib/pyroswitch loop.

Table 11. **Short between loops diagnostics decoding**

Fault condition on squib/ pyroswitch channel	Channel leakage diagnostics with PD_CURR on (for other channels than the one under test)	Channel leakage diagnostics with PD_CURR off (for all channels)
No shorts	No fault	No fault
Short to battery	STB fault	STB fault
Short to ground	STG fault	STG fault
Short between Loops	STG fault	No fault

The condition of two open channels, i.e. without squib/pyroswitch resistance connecting SFx to SRx, that have a short between loops on SFx cannot be detected. If only one of the two shorted SFx pins is open, the fault will be indicated on the open channel.

Squib/Pyroswitch resistance measurement

During a resistance measurement, a two-step process is performed.

At the first step, both the ISRC current generator and the ISNK current limited switch are enabled and connected to the selected SFx and SRx channel, through ISRC, ISRC_CURR_SEL, ISNK and RES_MEAS_CHSEL bit fields in the Loop Diagnostic Request Register (LPDIAGREQ). The ISRC current can be configured to either 40 mA or 8 mA nominal value through the ISRC_CURR_SEL bit in the LPDIAGREQ register providing the user with two different measurement range options. A differential voltage is created between the SFx and SRx pin based on the ISRC current and squib/pyroswitch resistance between the pins. The SPI interface will provide the first resistance measurement voltage (Vdiff1) based on the amplifying factor of the differential amplifier and a 10 bit internal ADC conversion.

The second measurement step (bypass measurement) is performed redirecting ISRC to the selected SRx pin, while keeping ISNK on; this way, the differential amplifier and following ADC will output the offset measurement through SPI (Vdiff2). Microcontroller is then allowed to calculate the mathematical difference between first and second measurements to obtain the real squib/pyroswitch resistance value.

$$Vdiff1 = G_{RSQ} \times \left[I_{SRC\_*} \times \left(\frac{R_{LKG\_SF} \times R_{SQ}}{R_{LKG\_SF} + R_{SQ}} \right) + \frac{R_{SQ}}{R_{LKG\_SF} + R_{SQ}} \times \left(V_{LKG\_SF} - V_{SRx\_RM} \right) \right] + V_{off\_RSQ}$$

$$V_{diff2} = \frac{G_{RSQ} \times R_{SQ}}{R_{LKG\_SF} + R_{SQ}} \times \left(V_{LKG\_SF} - V_{SRx\_RM} \right) + V_{off\_RSQ}$$

$$R_{SQ} = \frac{V_{diff1} - V_{diff2}}{G_{RSQ} \times I_{RSC\_*}} \quad (\text{assuming} R_{LKG\_SF} \gg R_{SQ})$$

The simplification in the calculation method reported above can result in some amount of error that is already incorporated in the overall tolerance of the squib/pyroswitch resistance measurement reported in the electrical parameters table.

Values of each measurement step can be required addressing the proper ADCREQx code in the Diagnostic Control command (DIAGCTRLx) on Table 14. Diagnostics control register (DIAGCTRLx).

This calculation is tolerant to leakages and, thanks to a dedicated EMI low-pass filter, also to high frequency noises on squib/pyroswitch lines. Moreover, L9679E features a slew rate control on the ISRC current generator to mitigate emissions.

The ISRC current generator is connected to VSYNC input pin. Special care shall be considered in programming the duty cycle of the squib/pyroswitch measurements to keep the power dissipation under control, in the event VSYNC line is supplied with high voltage.

High squib/pyroswitch resistance diagnostics

With this test, the device is able to understand if the squib/pyroswitch resistance value is below 200 Ω, between 500 Ω and 2000 Ω or beyond 5000 Ω. During a high squib/pyroswitch resistance diagnostics, VRCM and ISNK are enabled and connected respectively to SFx and SRx on the selected channel. VREF voltage level will be output on SFx. Current flowing on SFx will be measured and compared to I_{SRlow} and I_{SRhigh} thresholds to identify if the resistance is above or below R_{SRlow} or R_{SRhigh} levels. The results are reported in the LPDIAGSTAT register. The relative flags (HSR_HI and HSR_LO) are not latched and reflect the current status of the comparators.

High- and low-side FET diagnostics

This couple of tests can only be run during the diagnostic mode of the power-up sequence (as described in Figure 6. IC operating state diagram). Tests are performed individually for HS driver or LS driver, with two dedicated commands. Prior to either the HS or LS FET diagnostics being run, the VRCM has to be first enabled. Within the command to enable the VRCM, also the channel onto which the FET test will be run has to be selected with the LEAK_CHSEL bit field. Running the leakage diagnostics with the appropriate delay time prior to either the HS or LS FET diagnostics will precondition the squib/pyroswitch pin to the appropriate voltage level. When the FET diagnostic command is issued with the Diagnostic Register SPI command (SYSDIAGREQ), the VRCM flags will be cleared, the VRCM deglitch filter time is switched from the leakage diagnostic deglitch filter time (T_{FLT_LKG}) to the FET test deglitch filter time ($T_{FLT\_LKGB\_FT}$) for both HS and LS and the output of the VRCM deglitch filter is now allowed to disable the appropriate HS or LS squib/pyroswitch driver during FET test.

The device monitors the current through the VRCM. If the FET is working properly, this current will exceed $I_{HS\_FET\_TH}$ or $I_{LS\_FET\_TH}$ current threshold, respectively for HS or LS FET test for the deglitch filter time of $T_{FLT\_LKGB\_FT}$, and the driver under test is turned off immediately and automatically.

If there is a substantial leakage fault to Vbat or Gnd present during the FET test, leading this leakage current to exceed the IHS_FET_TH or ILS_FET_TH current threshold, for the deglitch filter time of $T_{FLT\_LKGB\_FT}$, then the driver under test is turned off immediately and automatically, and the corresponding VRCM flag, STG or STB, is set.

If the current does not exceed the current threshold, the test will be terminated and the driver is anyway turned off within $T_{FETTIMEOUT}$.

Table 12. HS FET TEST

VRCM Flags		Result
STG	STB	
0	0	FET test fail
0	1	FET test pass OR Leakage to Vbat
1	0	FET test disabled due to Leakage to Gnd
1	1	State not possible

Table 13. LS FET TEST

VRCM Flags		Result
STG	STB	
0	0	FET test fail
0	1	FET test disabledd due to Leakage to Vbat
1	0	FET test pass OR Leakage to Gnd
1	1	State not possible

During $T_{FETTIMEOUT}$ period, the bit stating that the FET is enabled will be set (FETON=1) and will be cleared as soon as the FET is switched back off.

For all conditions the current on SFx/SRx pins will not exceed the VRCM current limitation value ($I_{LIM\_VRCM\_SINK}$ or $I_{LIM\_VRCM\_SRC}$). There may be higher currents on the squib/pyroswitch lines due to the presence of filter capacitors. During these FET tests, energy available to the squib/pyroswitch is limited to less than E_{FET_TEST}. For high side FET diagnostics, if no faults were indicated in the preceding leakage diagnostics then a normal result would be [STB=1, STG=0]. If the returned result for the high side FET test is not as the previous then either the FET is not functional, a short to ground occurred during the test, or there is a missing SSxy connection for that channel.

For low-side FET diagnostics if no faults were indicated in the preceding leakage diagnostics then a normal result would be [STB=0, STG=1]. If the returned result for the low-side FET test is not as the previous then either the FET is not functional or a short to battery occurred during the test. In case of ground loss the low-side FET diagnostic would not indicate a FET fault.

The VRCM flags will be given in the LPDIAGSTAT register. The status of the VRCM flags after FET test is latched and can be cleared upon either LPDIAGREQ or SYSDIAGREQ SPI commands.

Finally, after FET test is completed, the VRCM deglitch filter time is switched from the FET test deglitch filter time ($T_{FLT\_LKGB\_FT}$) to the leakage diagnostic test deglitch filter time (T_{FLT_LKG}) for both HS and LS and the output of the VRCM deglitch filter is now not allowed to disable the appropriate HS or LS squib/pyroswitch driver anymore.

Loss of ground return diagnostics

This diagnostics is available during a squib/pyroswitch measurement. This test is based on the voltage drop across the ground return, if the voltage drop exceeds SG_{xy_OPEN}, ground connection is considered as lost. Should the ground connection on the squib/pyroswitch driver circuit be missing, the bit related to the channel under test by the two above diagnostics will be activated in the LP_GNDLOSS register. The flag is latched after a proper filter time T_{FLT_SGOPEN} and cleared upon read.

High-side safing FET diagnostics

The user can measure the voltage levels of the SSxy nodes. If the safing FET is properly switched on, the voltage on SSxy will be regulated.

The measurement request is done via Diagnostic Control command (DIAGCTRLx), while results will be reported through ADCRESx bit fields.

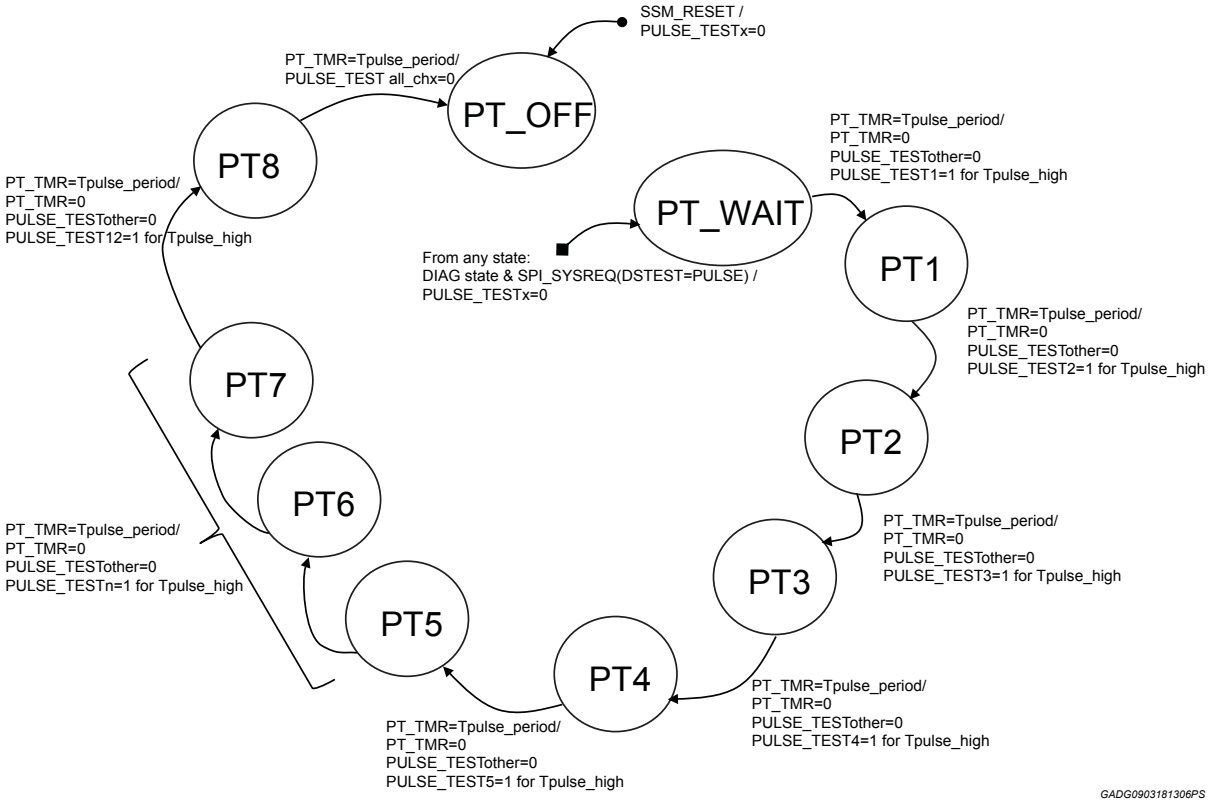
Deployment timer diagnostic

This test allows to verify the correct functionality and duration of the timers used to control the deployment times. This test can be executed only when the IC is in the Diag state by setting the appropriate code in the DSTEST field of the SYSDIAGREQ register. When the test is launched, the IC sequentially triggers the activation of the deployment timers of the various channels (each of them separated by 8ms idle time) and outputs the relevant waveform to the FENL output discrete pin, which will act as an output pin only for this test (put an external resistor to limit the current if double driver condition is present).

Additional test is available to check operation of FENL output buffer through dedicated value of DSTEST field.

To understand the sequence of deployment timer test look at Figure 17. Deployment timer diagnostic sequence. The µC can therefore test the deployment times by measuring the duration of the high pulses sent by the IC on the FENL pin. The deployment time configuration used during this test is the latest one programmed in the DCRx registers. In case the test is run on a channel with no DCRx deployment time previously configured, a default 8 µs high pulse is output on FENL for the relevant channel.

Figure 17. **Deployment timer diagnostic sequence**



Squib/Pyroswitch diagnostic with common SRx connected loops

In case of two SRx pins which are intentionally connected together, the PD_CURR_CSR bit of the Deployment Configuration register (DCR_x, where x = 0, 2, 4, 6) must be used to indicate which loop pairs have the common SRx connection. The purpose of this additional bit is to control the pull-down current on each channel to be consistent with or without the Common SRx connected loops. When the DCR_x(PD_CURR_CSR) bit is set for one loop pair and the Deployment diagnostic is run on that loop pair, the pull-down current is disabled on both channels of the loop pair selected.

For the squib/pyroswitch channel pair with common SRx connection, to understand if the two SFx pins are shorted together, the squib/pyroswitch resistance measurement must be required with the following setting: LPDIAGREQ[12:11]=11. In this way the ISRC current generator is enabled on the channel selected by RES_MEAS_CHSEL[3:0] bits while the Differential Operational Amplifier is connected on the other channel of the squib/pyroswitch channel pair. If the short between the two SFx pin is not present then the squib/pyroswitch resistance measurement results will be close to 0, otherwise it will be half the real squib/pyroswitch resistance.

Loop diagnostics control and results registers

Diagnostic tests and channels for each test are controlled through the Loop Diagnostic Request Register (LPDIAGREQ), diagnostic results are stored in the Loop Diagnostic Status Register (LPDIAGSTAT).

7.4.2 High-level diagnostic approach

In this approach, the test steps described in the sections below are coded into a dedicated state machine that helps reducing the user intervention to a minimum.

The high-level diagnostic commands are contained in the LPDIAGREQ, LOOP_DIAG_SEL, and LOOP_DIAG_CHSEL registers. The high-level diagnostic response is available in the LPDIAGSTAT register.

The concept is depicted in the following figures.

Figure 18. High-level loop diagnostic flow 1

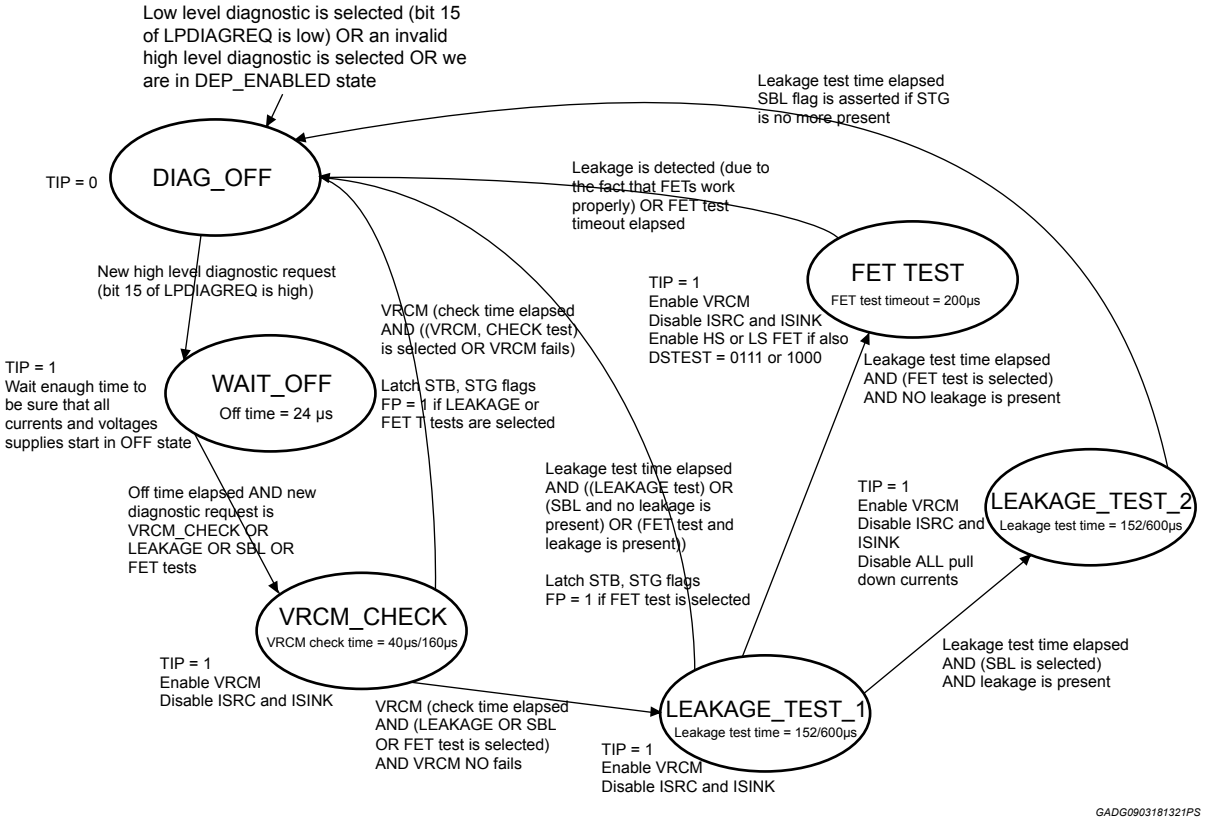
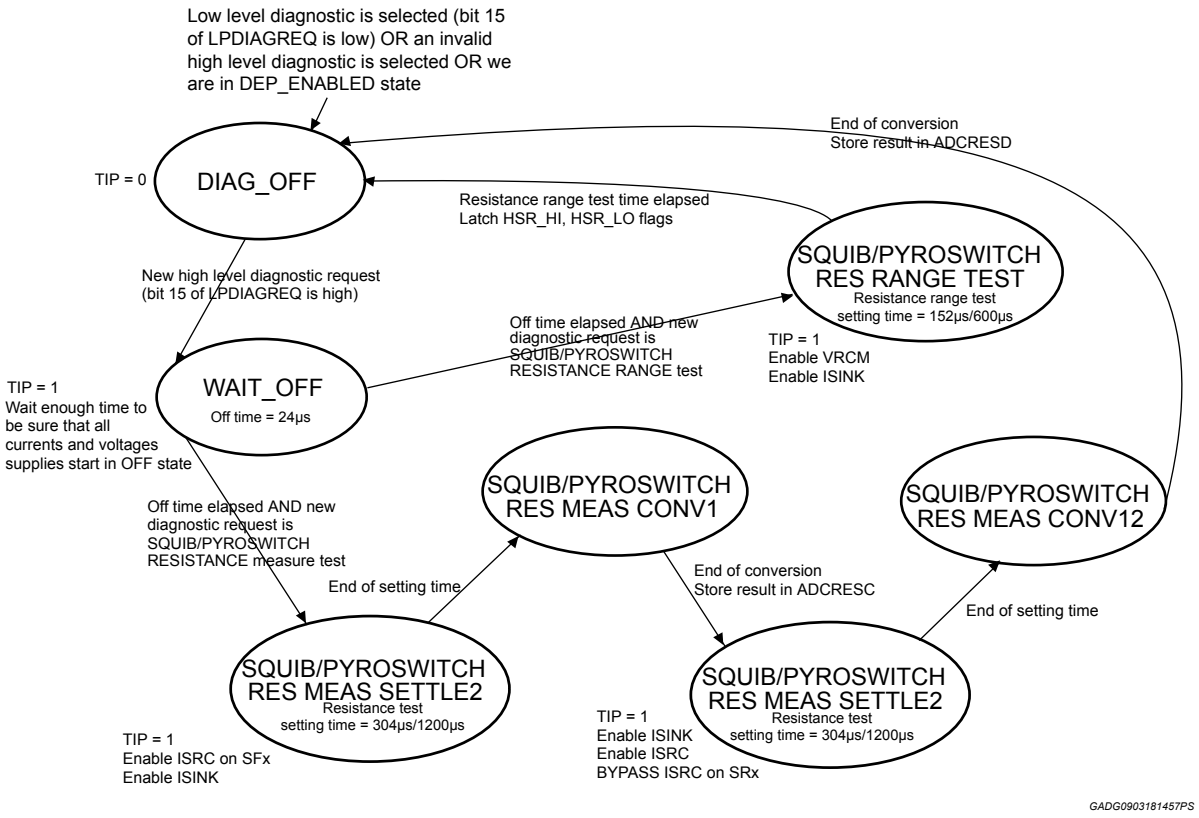


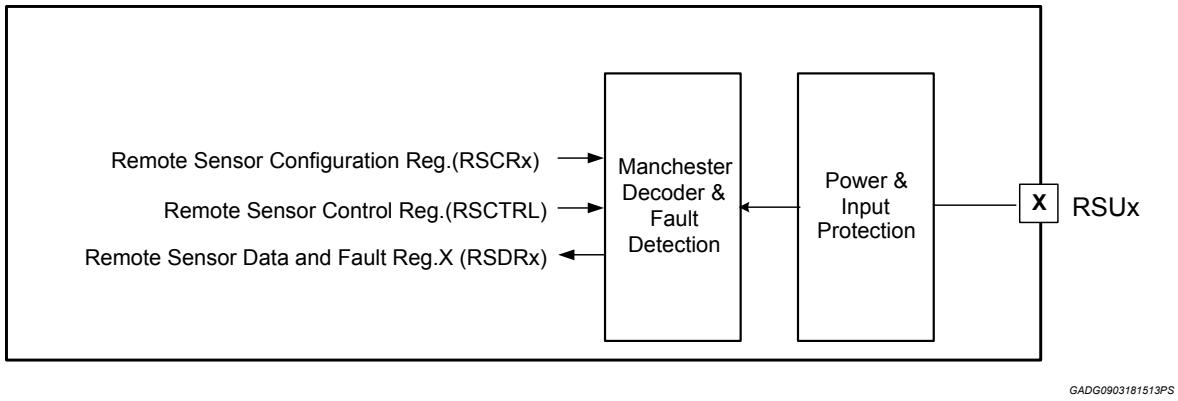
Figure 19. High-level loop diagnostic flow 2



8 Remote sensor interface

The L9679E contains 4 remote sensor interfaces, capable of supporting PSI-5 protocol (asynchronous and synchronous modes, increased voltage, extended range). A simplified block diagram of the interface is shown below. The interface supply is given on the VSAT pin. The circuitry consists of a power interface that mirrors current flowing in the external sensor and transmits this current information to the decoder, which produces a digital value for each remote sensor channel. The voltage at the RSUx pins can be limited by the power interface in case of VSAT supply overvoltage to protect the external sensors. Decoded data are then output through the Remote sensor data registers (RSDRx). The power interface also contains error detection circuitry. When a fault is detected, the error code is stored in a global SPI data buffer in the Remote sensor data registers (RSDRx).

Figure 20. Remote sensor interface control blocks



Remote sensor configuration can be addressed via the Remote sensor configuration registers (RSCRx). In particular, TSxDIS bit allows overriding the time slot control for PSI5 I/F and BLKTxSEL allows selection between 5 ms and 10 ms for the blanking time applied to the current limitation fault detection each time a channel is activated.

The Remote sensor control register (RSCTRL) allows for interface channels to be switched on and off and for Sync Pulse control via SPI.

Channels can be switched on only if VSAT voltage is above a certain threshold (VSAT_OK). This condition is necessary only when microcontroller is requesting the activation of the channel (for example at power up or after the recovery from fault condition). If channel is already active and VSAT goes below this threshold the channel is NOT switched off.

The value of this threshold can be changed via SPI. Two configurations are possible (VSAT_OK_TH0 and VSAT_OK_TH1).

The remote sensor interface reports both data information and fault information in the Remote sensor data register (RSDRx).

The device accommodates for a total of 12 data registers (3 for each interface). Independent data registers are defined for each remote sensor interface.

In case asynchronous mode is selected for one interface only the first data register of the three is used.

If the device detects an error on the sensor interface, the MSB in RSDRx (FLTBIT) will be set to ‘1’ and the following bits will be used to report the detected errors. Otherwise, the register will contain only data information. Detailed information on data and fault reporting are explained in the following sections.

When a fault condition is detected, the RSFLT bit of the global status word (GSW) is set to 1. Faults other than Short-to-ground and Over-temperature will only clear after read, not by the disabling of channel.

Data is cleared upon reading the RSDRx register.

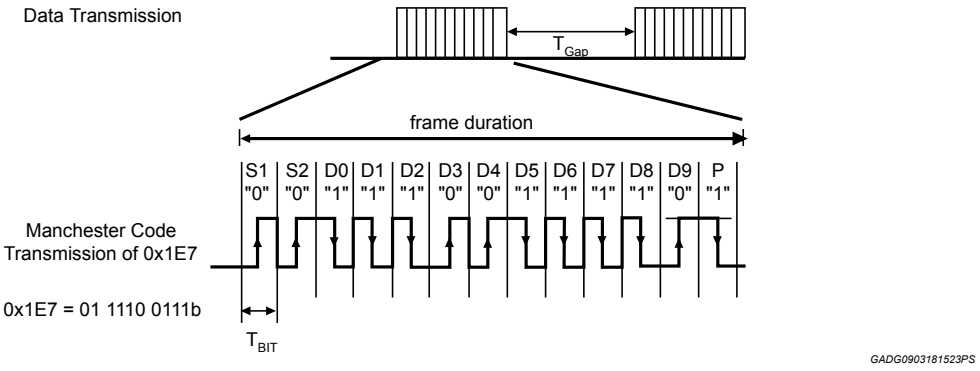
8.1 PSI-5 mode

All channels are compliant to the PSI-5 v1.3 specification as described below:

- Two-wire current interface
- Manchester coded digital data transmission
- High data transmission speeds of 125 kbps and 189 kbps
- Variable data word length (8- and 10-bit only)
- 1-bit parity
- Asynchronous operating mode with 3 stage input data buffers
- Synchronous operating mode with 3 time slots

An example of the data format for one possible PSI-5 protocol configuration is shown below. Data size and the error checking may vary, but the presence of 2 sync start bits (referenced below as sync bits) and 2 TGap time is consistent regardless.

Figure 21. PSI-5 remote sensor protocol (10-bit, 1-bit parity)



8.1.1 Functional description

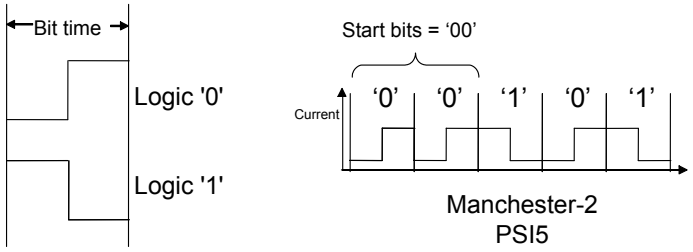
The remote sensor interface block provides a hardware connection between the microcontroller and up to twelve remote sensors (maximum three per channel). Each channel is independent from the others, and is not influenced by possible fault conditions occurring on other channels, such as shortcircuits to ground or to vehicle battery. Each channel is supplied by a current limited DC voltage derived from VSAT pin, and monitors the current sunk from its supply in order to extract encoded data. The remote sensor modulates the current draw to transmit Manchester-encoded data back to the receiver. The current level detection threshold for all channels is internally computed by the IC in order to adapt the signal level to the sensors quiescent current.

All channels can be enabled or disabled independently via SPI commands. The operational status of all channels can also be read via SPI command. All channels support individual selective sync-pulse control to allow communication back to the remote sensor via sync-pulse voltage modulation as described in the PSI5 v1.3 specification.

In case asynchronous mode is selected for one interface the sync pulse is not generated (sync pulse control bit is don’t care).

The message bits are encoded using a Manchester format, in which logic values are determined by a current transition in the middle of the bit time. When configured for PIS5 sensors each interface supports Manchester 2 encoding as shown in Figure 22. Manchester bit encoding.

Figure 22. Manchester bit encoding



To reject glitches on decoded signal that could compromise message decoding a deglitch filter is implemented after current transition detection. This means that a delay is present until the threshold crossing is detected by decoder. The filter time can be configured in 15 steps by PSI5FILT bits through the Remote Sensor Configuration Register and can be selected individually for each channel.

Each RSDRx register is updated after a certain delay ($T_{WRITE\_EN\_DELAY}$) from the end of relative sensor message. All the bits inside the register itself are simultaneously updated upon reception of the remote sensor message to prevent partial frame data from being sampled via the SPI interface. After the data for a given channel is read via the SPI interface, subsequent requests for data from this channel will result in an error response.The remote sensor interface is also able to detect faults occurring on the sensor interface. The remote sensor data register (RSDRx) will report multiple fault flags.

When the number of bits decoded is incorrect (either too many or too few), a bit error is indicated. When any bit error is detected (bit time, too many bits, too few bits), the decoder will revert to the minimum bit time of the selected range and the message is discarded.

Error bit INVALID is an OR-ed combination of the following errors:

- Start bit error outside of selected operating range
- Data length error or stop bit error
- Parity error of received remote sensor message
- Bit time error (a data bit edge is not received inside the expected time window)

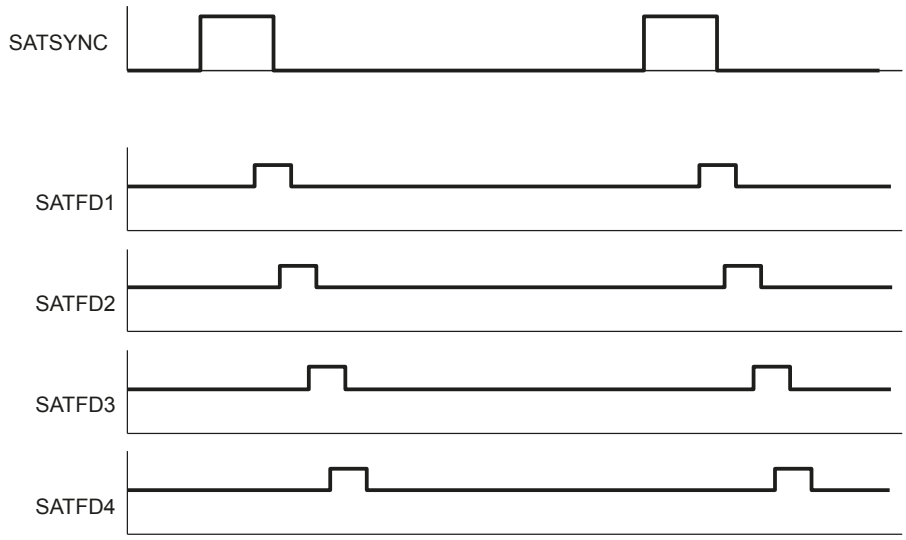
Synchronous mode

The received message data is stored in input data registers that are read out by the microcontroller via the SPI interface. For PSI-5 synchronous mode, three data registers per channel are used to store remote sensor messages received during time slots 1, 2, and 3 respectively.

In case of a fault related to a channel, the fault bit is loaded in all the 3 time slot register and has the priority, so the fault overwrites valid data.

To allow the sampling synchronization of remote sensor data with the software in the microcontroller, the remote sensor interface block includes sync-pulse circuitry to signal initiation of sampling in the remote sensor. The sync-pulse is output to the remote sensors in the form of an increased voltage level on the RSUx pins when sampling is to be conducted. The higher voltage level required for the sync-pulse is sourced from the VSYNC pin. Pulse shaping is used to limit the slew rate of the pulses to reduce EMI. Feedback protection is provided to prevent fault conditions on one channel from affecting the others during sync-pulse generation. The microcontroller schedules the activation of the sync pulses to the four channels by providing a periodic signal to the SATSYNC pin. When a rising edge is detected on SATSYNC pin, the remote sensor interface block outputs sync pulses on output channels RSUx in sequence to reduce the average current inrush to the remote sensors as shown in Figure 23. Remote sensor synchronization pulses. The voltage source in the remote sensor interface block can source and sink current and is used to discharge the bus capacitance at the end of the sync pulse. The pull down device used to sink current is current limited.

Figure 23. **Remote sensor synchronization pulses**



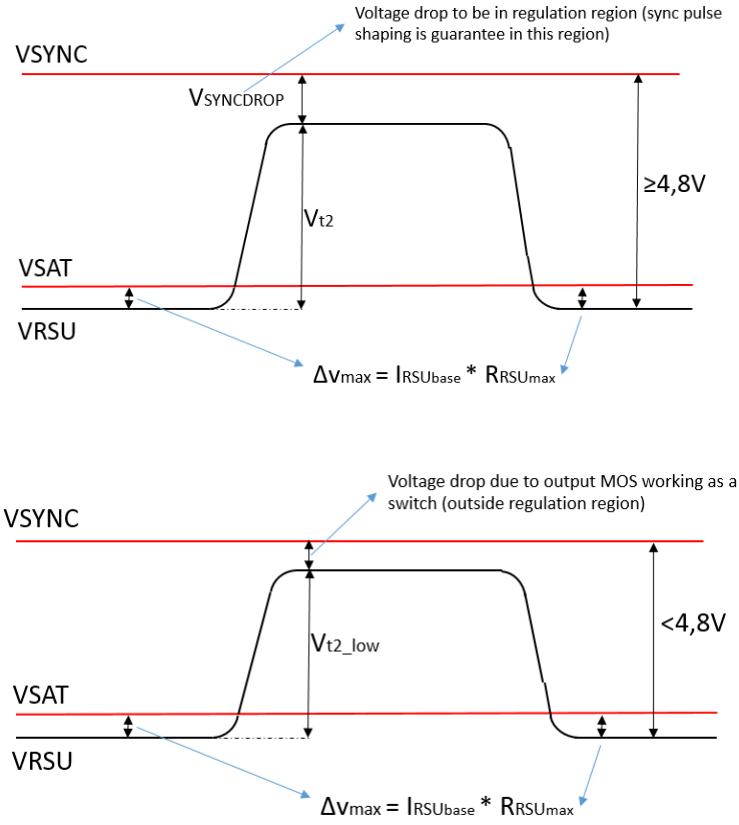
To guarantee sync pulse shaping and minimum sync pulse amplitude (V_{t2}) there are constraints on the minimum delta voltage between VSYNC and VSAT supplies.

For VSYNC supply large enough (VSYNC ≥ VRSUbase + 4.8 V), the interface regulate the sync pulse (regulation mode) and V_{t2} amplitude is guaranteed.

For VSYNC supply lower, the sync pulse amplitude is limited by the drop across the FET RDSon so designer shall consider a lower amplitude for it.

In case L9679E IC is supplied directly by the SB1 system chip, the worst case in terms of delta between VSYNC and VSAT can be considered equal to 4.2 V. In this case the min V_{t2} that the IC is able to guarantee is indicated by parameter V_{t2_low}.

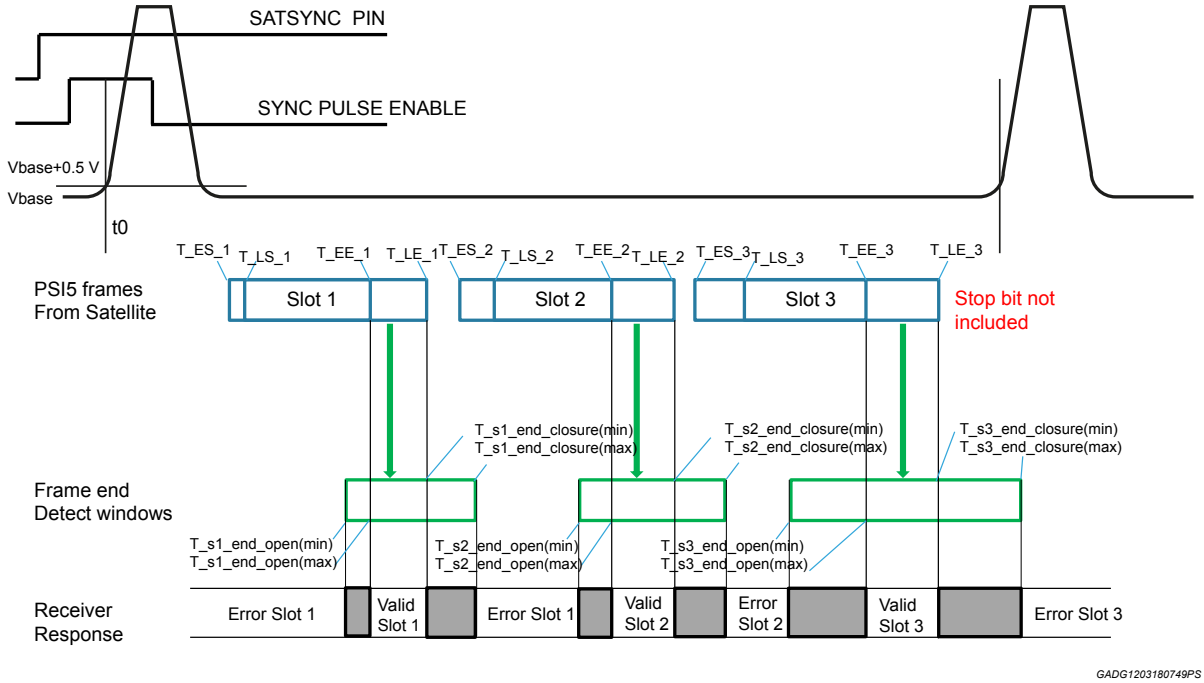
Figure 24. Sync pulse dependence by supplies



GADG1203180733PS

L9679E supports three time slots in a sync period with associated RSDRx registers. The messages received within one sync period are routed to the corresponding RSDRx register associated to each time slot. A time slot control is performed to check if the incoming messages fall within the valid time slots reported in Table 34. PSI-5 Satellite Transceiver - AC Specifications and sketched in Figure 25. PSI5 Slot Timing Control. If the end of the received message occurs outside a valid time slot, a SLOT_ERROR fault will be detected and stored in the related RSDRx register. Slot error assignment is described in Figure 25. PSI5 Slot Timing Control. For instance, if the end of second message falls before expected valid time window the error slot 1 is asserted and then also the data received with the first message is lost. If two messages end within the same slot, the second message will be assigned to that slot, regardless of its validity. The time slot control can be disabled by setting the TSxDIS bit in the RSCRx register.

Figure 25. PSI5 Slot Timing Control



Asynchronous mode

For PSI-5 asynchronous mode, three data registers per channel are used to store a maximum of three remote sensor messages.

In this way the frequency of SPI access of the microcontroller to read data can be reduced assuming that during each phase of data reading the microcontroller is able to send consecutive SPI frames to read all accumulated data.

This data buffer works as a FIFO, so the microcontroller reads always the oldest data message.

In case the microcontroller is not fast enough to read the three accumulated data, the IC will discard the oldest data when new data is incoming.

SPI access to read data is asynchronous respect to writing of data registers, so the IC has been designed to prevent data losses in case these two events occur at the same time.

There is only one SPI register address for each channel that the microcontroller has to read to get all the data.

This address is the one related to slot1 in the equivalent synchronous mode.

Trying to read addresses related to slot2 and slot3 will respond with all zeros in READ[19:16] field of MISO_RS.

8.1.2 Sensor data integrity: LCID and CRC

Each RSDRx data register contains a Logical Channel ID which is a 4/2-bit field for remote sensors used to link the received data to the corresponding logical channel number.

In case of asynchronous mode, the two LSB of the LCID field are stuck to “00”.

Each RSDRx register contains also a CRC bit field computed on the data packet for data integrity check. To satisfy functional safety requirements, the LCID, DATA and CRC bit fields propagate through the same data path as a single item to the SPI output.

The polynomial calculation implemented for PSI-5 data is described as in PSI-5 specification

g(x)=1+x+x^3 with initialization value equal to "111".

These are the equations to calculate the CRC in combinatorial way:

CRC[2] = CRCext[0]+D[0]+D[1]+D[3]+D[6]+D[7]+D[8]+D[10]+D[13]+D[14]+D[15]

CRC[1] = CRCext[2]+D[0]+D[1]+D[2]+D[4]+D[7]+D[8]+D[9]+D[11]+D[14]+D[15]+D[16]

CRC[0] = CRCext[1]+CRCext[0]+D[0]+D[2]+D[5]+D[6]+D[7]+D[9]+D[12]+D[13]+D[14]+D[16]

Where D[16:0]= RSDR[16:0] and CRCext[n] are the starting seed values (all '1').

8.1.3 Detailed description

Manchester decoding

The Manchester decoder will support remote sensor communication as per *PSI specification rev 1.3* for the modes configurable via the STS bits in the RSCRx registers. The Manchester decoder checks the duty-cycle and period of the start bits to determine their validity, depending on the configuration of the PERIOD_MEAS_DISABLE bit in the RSCRx registers. The expected time windows for the mid bit transitions of each subsequent bit within the received frame are determined by means of the internal oscillator time base. Glitches shorter than 25% of the minimum bit time duration are rejected.

A Manchester decoder error occurs if one or more of the following are true:

- Two valid start bits are detected, and at least one of the expected 13 mid-bit transitions are not detected;
- Two valid start bits are detected, and more than 13 mid-bit transitions are detected;
- When the number of bits decoded is incorrect (either too many or too few), a bit error is indicated. When any bit error is detected (bit time, too many bits, too few bits), the decoder will revert to the minimum bit time of the selected range and the message is discarded.

All errors are readable through the Sensor fault status register and the RSFLT bit in the Global status word register.

When a valid message is correctly decoded, the 10/8 data bits are stored into the appropriate RSDRx register together with the related LCID. The RSDRx register contains the 10/8 bits data as they are received from the sensor (no data range check/mask is done at this stage). The 8-bit data word is right-justified inside the 10-bit data field in the RSDRx registers.

Current sensor w/ auto-adjust trip current

The current sensor is responsible for translating the current drawn by the sensor into a digital state. Each remote sensor channel has a dedicated current sensor.

The current flowing through the RSU power stage is internally downscaled by a factor 100, sent to a 10 bits A/D converter and digitally processed to extract both the sensor quiescent and delta currents.

The delta current threshold for signal detection is auto-adjusted to the actual calculated sensor delta current.

The current trip point is dynamically determined by adding the delta current threshold (auto-adjusted) to the quiescent current (auto-adjusted). The RSU current is compared against the current trip point to determine the current demodulator digital output. A logic ‘1’ represents the sensor current above the current trip point. The current demodulator output is fed into the Manchester decoder.

Thanks to the quiescent and delta current tracking features the receiver is capable of automatically adapting to different nominal sensor currents and/or of being tolerant to sensor current drifts over lifetime.

Compared with other products of the same family (L9679 and L9680), L9679E follows only one approach to adjust base and delta current. This approach can be selected also in L9679 and L9680 by setting high the AVG/SSDIS bit of RSCRx.

9 Remote sensor interface fault protection

9.1 Short-to-ground, current limit

Each output is shortcircuit-protected by an independent current limit. Should the output current level reach or exceed the I_{LIMTH} for a time period greater than T_{ILIMTH} or the remote sensor interface the output stage is disabled. An internal up-down counter will count in 25 µs increment up to T_{ILIMTH}. The filter time is chosen in order to avoid false current limit detection for in-rush current that may happen at interface switch-on. When the output is turned off due to current limit, the appropriate fault code STG is set in the Remote sensor data register (RSDR). The fault timer latch is cleared when the sensor channel is first disabled and then re-enabled through the Remote sensor control register (RSCTRL). This fault condition does not interfere either with the normal operation of the IC, or with the operation of the other channels. When a sensor fault is detected, the RSFLT bit of the GSW is set indicating that a fault has occurred and can be decoded by addressing the RSDR register.

In order to fulfil the blanking time requirement at channel activation as per the PSI-5 specification, a dedicated masking time is applied to the current limitation fault detection each time a channel is activated.

9.2 Short-to-battery

All outputs are independently protected against a short-to-battery condition. Short-to-battery protection disconnects the channel from its supply rail to guarantee that no adverse condition occurs within the IC. The short-to-battery detection circuit has input offset voltage (10 mV, minimum) to prevent the output from disconnecting under an open circuit condition. A short-to-battery is detected when the output RSUx pin voltage increases above the VSAT or VSYNC (depending on operation) supply pin voltage for a T_{STBTH} time. An internal up-counter will count in 1.5 µs increment up to T_{STBTH}. The counter will be cleared if the short condition is not present for at least 1.5 µs. The channel in short-to-battery is not shut down by this condition. Other channels are not affected in case of short of one output pin. As in the case previously described, the STB fault code can be read from RSDR bits and any fault will set the RSFLT bit of the global status word register (GSW). The STB bit is cleared upon read or upon channel disabled via the SPI RSCTRL register.

9.3 Cross link

The device provides also the capability of a cross link check between outputs, in order to reveal conditions where two output channels are in short. This functionality is allowed by enabling one output channel, while asking for voltage measurement on any of the other ones.

9.4 Leakage-to-battery, sensor open

The sensor interface offers also open sensor detection. The auto-adjusting counter for remote sensor current sensing will drop to 0 in case the current flowing through the RSUx pin is lower than 2.5 mA typ. The OPENDET fault flag is asserted when the fault condition lasts for longer than the $T_{FLT\_OPEN\_RSU}$ deglitch filter time. This fault flag can be read from the RSDR bits and any fault will set the RSFLT bit of the global status word register (GSW). The channel in this condition is not shut down. This fault bit is cleared upon read or upon channel disabled via the SPI RSCTRL register.

9.5 Leakage-to-ground

The sensor interface also offers the detection of a leakage-to-ground condition, which will possibly raise the sensor current higher than 42 mA typ. The CURRENT_HI fault flag is asserted when the fault condition lasts for longer than the $T_{FLT\_LKG\_RSU}$ deglitch filter time. This fault flag can be read from the RSDR bits and any fault will set the RSFLT bit of the global status word register (GSW). The channel in this condition is not shut down. This fault bit is cleared upon read or upon channel disabled via SPI RSCTRL register.

9.6 Thermal shutdown

Each output is protected by an independent over-temperature detection circuit. Should the remote sensor interface thermal protection be triggered, the output stage is disabled and a corresponding thermal fault is latched and reported through the RSTEMP flag in the Remote sensor data register (RSDRx). The thermal fault flag is cleared when the sensor channel is first disabled and then re-enabled through the Remote sensor configuration register (RSCRx).

10 System voltage diagnostics

L9679E has an integrated dedicated circuitry to provide diagnostic feedback and processing of several inputs. These inputs are addressed with an internal analog multiplexer and just one internal ADC and made available through the SPI digital interface with the diagnostics data commands. In order to avoid saturation of high-voltage internal signals, an internal voltage divider is used. The diagnostics circuitry is activated by four SPI diagnostics control commands (DIAGCTRLx); each of them can address all the available nodes to be monitored, except for what mentioned in Table 14. Diagnostics control register (DIAGCTRLx).

The DIAGCTRLx SPI command bit fields are structured in the following way:

DIAGCTRL_A (ADDRESS HEX 3A)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI					x	x	x	x	x	x	x	x	x	ADCREQ_A [6:0]						
MISO	NEWDATA_A	0	0	ADCREQ_A[6:0]							ADCRES_A[9:0]									

DIAGCTRL_B (ADDRESS HEX 3B)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI					x	x	x	x	x	x	x	x	x	ADCREQ_B [6:0]						
MISO	NEWDATA_B	0	0	ADCREQ_B [6:0]							ADCRES_B [9:0]									

DIAGCTRL_C (ADDRESS HEX 3C)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI					x	x	x	x	x	x	x	x	x	ADCREQ_C [6:0]						
MISO	NEWDATA_C	0	0	ADCREQ_C [6:0]							ADCRES_C [9:0]									

DIAGCTRL_D (ADDRESS HEX 3D)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI					x	x	x	x	x	x	x	x	x	ADCREQ_D [6:0]						
MISO	NEWDATA_D	0	0	ADCREQ_D [6:0]							ADCRES_D [9:0]									

ADCREQ[A-D] bit fields, used to address the different measurements offered, are listed in Table 14. Diagnostics control register (DIAGCTRLx) for reference.

L9679E diagnostics is structured to take four automatic conversions at a time. In order to get four measurements, four different SPI commands have to be sent (DIAGCTRL_A, DIAGCTRL_B, DIAGCTRL_C and DIAGCTRL_D) in no particular order.

In case the voltage to be measured is not immediately available, the desired inputs for conversion have to be programmed by SPI in advance, to allow them to attain a stable voltage value. This case applies to the squib/pyroswitch resistance measurement and diagnostics (refer to Squib/Pyroswitch diagnostic with common SRx connected loops).

CONVRDY_0 bit in GSW is equal to (NEWDATA_A or NEWDATA_B), while CONVRDY_1 bit in GSW corresponds to (NEWDATA_C or NEWDATA_D).

Each NEWDATAx flag is asserted when conversion is finished and cleared when result is read out. However, the result is cleared only when a new result for that register is available.

When a new request is received, it is queued if other conversions are ongoing. The conversions are executed in the same order as their request arrived. The queue is 4 measures long so it is possible to send all 4 requests at the same time and then wait for the results. If a DIAGCTLRx command is received twice, the second conversion request will overwrite the previous one.

Requests are sent to the L9679E IC via the ADC measurement Registers (ADCREQx) as shown in Table 14. Diagnostics control register (DIAGCTRLx). All diagnostics results are available on the ADCRESx registers, when addressed by the related ADCREQx register (e.g. data requested by ADCREQA would be written to ADCRESA).

Table 14. Diagnostics control register (DIAGCTRLx)

ADC Request (ADCREQx)								Voltage Measurement Selection	ADC Results (ADCRESx)
Bit[6:0]							Hex		Bit[9:0]
0	0	0	0	0	0	0	0x00		
0	0	0	0	0	0	1	0x01	ADC ground reference	V_{ADC_GROUND}
0	0	0	0	0	1	0	0x02	ADC full scale reference	$V_{ADC\_FULLSCALE}$
0	0	0	0	0	1	1	0x03		
0	0	0	0	1	0	0	0x04		
0	0	0	0	1	0	1	0x05		
0	0	0	0	1	1	0	0x06	Squib/Pyroswitch measurement loop selected	Voutx
0	0	0	0	1	1	1	0x07	Internal reference Voltage	VBG1
0	0	0	1	0	0	0	0x08	Internal reference monitor Voltage	VBG2
0	0	0	1	0	0	1	0x09		
0	0	0	1	0	1	0	0x0A	Temperature Measurement	TEMP
0	0	0	1	0	1	1	0x0B		
0	0	0	1	1	0	0	0x0C		
0	0	0	1	1	0	1	0x0D		
0	0	0	1	1	1	0	0x0E		
0	0	0	1	1	1	1	0x0F		
0	0	1	0	0	0	0	0x10		
0	0	1	0	0	0	1	0x11		
0	0	1	0	0	1	0	0x12		
0	0	1	0	0	1	1	0x13		
0	0	1	0	1	0	0	0x14		
0	0	1	0	1	0	1	0x15		
0	0	1	0	1	1	0	0x16		
0	0	1	0	1	1	1	0x17		
0	0	1	1	0	0	0	0x18		
0	0	1	1	0	0	1	0x19		
0	0	1	1	0	1	0	0x1A		
0	0	1	1	0	1	1	0x1B		
0	0	1	1	1	0	0	0x1C		
0	0	1	1	1	0	1	0x1D		
0	0	1	1	1	1	0	0x1E		
0	0	1	1	1	1	1	0x1F		

ADC Request (ADCREQx)								Voltage Measurement Selection	ADC Results (ADCRESx)
Bit[6:0]							Hex		Bit[9:0]
0	1	0	0	0	0	0	0x20		
0	1	0	0	0	0	1	0x21		
0	1	0	0	0	1	0	0x22	Internal analog supply voltage (VINT3V3)	VINT3V3
0	1	0	0	0	1	1	0x23	Internal digital supply voltage (CVDD)	CVDD
0	1	0	0	1	0	0	0x24		
0	1	0	0	1	0	1	0x25	VSYNC pin voltage	VSYNC
0	1	0	0	1	1	0	0x26		
0	1	0	0	1	1	1	0x27	VSAT voltage	VSAT
0	1	0	1	0	0	0	0x28	VCC voltage	VCC
0	1	0	1	0	0	1	0x29		
0	1	0	1	0	1	0	0x2A		
0	1	0	1	0	1	1	0x2B	TEST pin voltage	TEST
0	1	0	1	1	0	0	0x2C		
0	1	0	1	1	0	1	0x2D		
0	1	0	1	1	1	0	0x2E		
0	1	0	1	1	1	1	0x2F		
0	1	1	0	0	0	0	0x30		
0	1	1	0	0	0	1	0x31		
0	1	1	0	0	1	0	0x32	RSU0 pin Voltage	RSU0
0	1	1	0	0	1	1	0x33	RSU1 pin Voltage	RSU1
0	1	1	0	1	0	0	0x34	RSU2 pin Voltage	RSU2
0	1	1	0	1	0	1	0x35	RSU3 pin Voltage	RSU3
0	1	1	0	1	1	0	0x36	SS0 pin voltage	SS0
0	1	1	0	1	1	1	0x37	SS1 pin voltage	SS1
0	1	1	1	0	0	0	0x38	SS2 pin voltage	SS2
0	1	1	1	0	0	1	0x39	SS3 pin voltage	SS3
0	1	1	1	0	1	0	0x3A	SS4 pin voltage	SS4
0	1	1	1	0	1	1	0x3B	SS5 pin voltage	SS5
0	1	1	1	1	0	0	0x3C	SS6 pin voltage	SS6
0	1	1	1	1	0	1	0x3D	SS7 pin voltage	SS7
0	1	1	1	1	1	0	0x3E		
0	1	1	1	1	1	1	0x3F		
1	0	0	0	0	0	0	0x40		
1	0	0	0	0	0	1	0x41		
1	0	0	0	0	1	0	0x42		
1	0	0	0	0	1	1	0x43		
1	0	0	0	1	0	0	0x44		
1	0	0	0	1	0	1	0x45		

ADC Request (ADCREQx)								Voltage Measurement Selection	ADC Results (ADCRESx)
Bit[6:0]							Hex		Bit[9:0]
1	0	0	0	1	1	0	0x46	SF0 pin voltage	SF0
1	0	0	0	1	1	1	0x47	SF1 pin voltage	SF1
1	0	0	1	0	0	0	0x48	SF2 pin voltage	SF2
1	0	0	1	0	0	1	0x49	SF3 pin voltage	SF3
1	0	0	1	0	1	0	0x4A	SF4 pin voltage	SF4
1	0	0	1	0	1	1	0x4B	SF5 pin voltage	SF5
1	0	0	1	1	0	0	0x4C	SF6 pin voltage	SF6
1	0	0	1	1	0	1	0x4D	SF7 pin voltage	SF7
1	0	0	1	1	1	0	0x4E		
1	0	0	1	1	1	1	0x4F		
1	0	1	0	0	0	0	0x50		
1	0	1	0	0	0	1	0x51		

Proper scaling is necessary for various measurements. The divider ratios vary by measurement and are summarized by function in the table below.

Table 15. Diagnostics divider ratios

Measurements	Divider Ratio				
	15:1	10:1	7:1	4:1	1:1
SSxy	√				
SFx	√				
VSYNC		√			
VSAT			√		
TEST			√		
RSUx			√		
VCC				√	
CVDD				√	
VINT3V3				√	
Bandgap (VBG1/VBG2)					√

For measurements other than voltage (current, resistance, temperature etc.) the ranges are specified in the electrical parameters section of the relevant block.

10.1 Analog-to-digital algorithmic converter

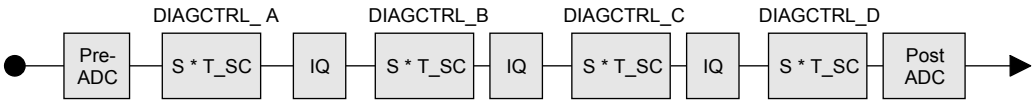
The device hosts one integrated 10-bit analog-to-digital converter, running at a clock frequency of 16 MHz. The ADC output is processed by a D-to-D converter with the following functions:

- Use of trimming bits to recover additional gain error due to resistor dividers mismatch;
- Digital low-pass filtering;
- Conversion from 12 to 10 bits.

10-bit data is filtered inside the digital section. The number of samples that are filtered varies depending on the chosen conversion. As SYS_CFG, the number of used samples in converting DC sensor, squib/pyroswitch or temperature measurements defaults to 8. The number of samples for all other measurements defaults to 4. The sample number can be configured by accessing the SYS_CFG register. After low pass filter, the residual total error is ±4 LSB. This error figure applies to the case of an ideal reference voltage: the spread of reference voltage causes a proportional error in the conversion output. The reference voltage of the ADC is set to 2.5 V.

The conversion time is comprised of several factors: the number of measurements loaded into the queue, the number of samples taken for any one measurement, and the various settling times. An example of conversion time calculation for a full ADC request queue is reported in Figure 26. ADC conversion time. The timings reported in the figure below are nominal ones, min/max values can be obtained by considering the internal oscillator frequency variation reported in the DC characteristics section.

Figure 26. ADC conversion time



Pre-AD C: I nitial ADC Settling Time = 4.81 µs
S: # of Samples (default = 4 for voltage only measurements)
T_SC: Single Sample Conversion Time = 2.25 µs
IQ: Intra-Queue Settling Time = 3.5 µs
Post-ADC: Final ADC Settling Time = 3.44 µs

GADG1203181038PS

11 Temperature sensor

The L9679E provides an internal analog temperature sensor. The sensor is aimed at having a reference for the average junction temperature on the silicon surface. The sensor is placed far away from power dissipating stages and squib/pyroswitch deployment drivers. The output of the temperature sensor is available via SPI through ADC conversion, as shown in Table 14. Diagnostics control register (DIAGCTRLx). The formula to calculate temperature from ADC reading is the following one:

$$\mathrm{T}(^{\circ}C) = 180 - \left\{\left(\frac{220}{1.652}\right) \times \left[\left(\frac{ADC_{REF}}{2^{ADC_{RES}}} \times \mathrm{DIAGCTRLn(ADCRESn)}\right) - 0.739\right]\right\} \qquad @\mathrm{DIAGCTRLn(ADCREQn)} = 0A_{hex}$$

All parametric requirements for this block can be found in specification tables.

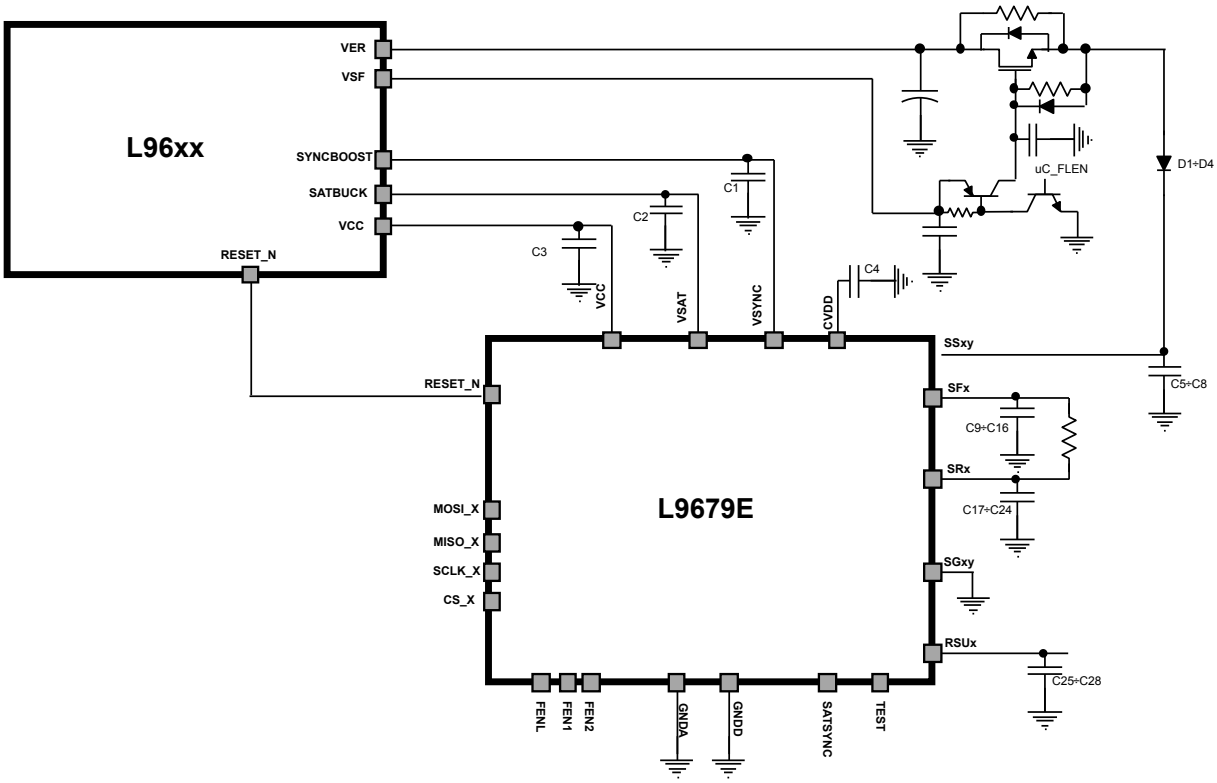
12 Applications

The main applications for this IC are two:

- as user configurable airbag IC;
- as pyro fuse manager IC.

12.1 Application circuit

Figure 27. **Application circuit**



12.2 Bill of materials

The following table summarizes the suggested BOM valid for both applications.

Table 16. Bill of materials

Component	Min	Typ	Max	Unit	Requirement	Notes
C1a	-	100	-	nF	35 V	VSYNC input capacitor
C1b	-	2.2	-	µF	35 V	VSYNC input capacitor
C2a	-	100	-	nF	25 V	VSAT input capacitor
C2b	-	2.2	-	µF	25 V	VSAT input capacitor
C3a	-	100	-	nF	16 V	VCC input capacitor
C3b	-	2.2	-	µF	16 V	VCC input capacitor
C4	-	100	-	nF	16 V	CVDD capacitor
D1..D4	-	1	-	A	-	SSxy diode
C5..C8	-	-	10	nF	25 V	SSxy capacitor
C9..C16	-	22	-	nF	25 V	SFx capacitor
C17..C24	-	22	-	nF	25 V	SRx capacitor
C25..C28	-	3.3	-	nF	25 V	RSUx capacitor

13 Electrical characteristics

The GNDA pin is used as ground reference for the voltage measurements performed within the device, unless otherwise stated.

All tables or parameters declared “Design Info” are not tested during production testing.

13.1 Operating supply range

All electrical characteristics are valid for the following conditions unless otherwise noted:

-40 °C ≤ T_{amb} ≤ +105 °C

Table 17. Operating supply range

Symbol	Parameter	Conditions / Comments	Min	Typ	Max	Unit
VCC_3	VCC input voltage range	Design Info	3.0	3.3	3.6	V
VCC_5	VCC input voltage range	Design Info	4.5	5	5.5	V
VSAT	VSAT input voltage range	-	6.72	7.2	9.36	V
VSYNC	VSYNC input voltage range	-	11.40	12	35	V
$I_{VCC\_DISABLED}$	VCC current consumption output disabled	DC state w/o sensor loads; not considering running diagnostics, nor fault conditions. MISO_G, MISO_RS, FENL outputs disabled.	-	-	5	µA
I_{VCC}	VCC current consumption output enabled	DC state w/o sensor loads; not considering running diagnostics, nor fault conditions. MISO_G, MISO_RS, FENL outputs enabled.	-	-	5	mA
$I_{VSAT\_NO\_RSU}$	VSAT current consumption NO RSU	DC state with RSU channels DISABLED; not considering running diagnostics, nor fault conditions	-	-	25	mA
I_{VSAT}	VSAT current consumption	DC state with all RSU channels ENABLED but w/o sensor loads; not considering running diagnostics, nor fault conditions	-	-	41	mA
$I_{VSYNC\_NO\_RSU}$	VSYNC current consumption NO RSU	DC state with RSU channels DISABLED; not considering running diagnostics, nor fault conditions	-	-	0.5	mA
I_{VSYNC}	VSYNC current consumption	DC state with all RSU channels ENABLED but w/o sensor loads; not considering running diagnostics, nor fault conditions	-	-	3	mA
I_{VSYNC_SLEEP}	VSYNC current consumption in OFF state	VSAT ≤ VSAT_ON(min)	-	-	5	µA
VSAT_OFF	VSAT OFF threshold	-	4.2	4.5	4.8	V
VSAT_ON	VSAT ON threshold	-	5.0	5.25	5.5	V
VSAT_OK_TH0	VSAT OK first threshold	-	6.2	6.5	6.8	V
VSAT_OK_TH1	VSAT OK second threshold	-	7.7	8.1	8.5	V
$VSYNC\_OK_{RISE}$	VSYNC_OK threshold on VSYNC rising edge	-	9	10	11	V
$VSYNC\_OK_{FALL}$	VSYNC_OK threshold on VSYNC falling edge	-	8	9	10	V
$VSYNC\_OK_{HYST}$	VSYNC_OK threshold hysteresis	-	0.6	-	1.2	V
V_{TEST_TH}	TEST threshold	Test go no go	10	12	14	V
V_{TEST_HYST}	TEST hysteresis	Design Info	0.2	0.4	0.5	V
I_{PD_TEST}	TEST Pull Down	V_{TEST} ≤ 5 V	20	45	70	µA
T_{VSAT_FILT}	VSAT filter time	-	900	-	1150	µs

Table 18. **Open ground detection DC specifications**

Symbol	Parameter	Conditions / Comments	Min	Typ	Max	Unit
$GNDA_{OPEN}$	GNDA open threshold	GNDD = 0	100	200	300	mV
$GNDD_{OPEN}$	GNDD open threshold	GNDA = 0	100	200	300	mV

Table 19. **Open ground detection AC specifications**

Symbol	Parameter	Conditions / Comments	Min	Typ	Max	Unit
$T_{FLT\_GNDREFOPEN}$	GNDA and GNDD Open Deglitch Filter Time	-	10	17	25	µs

13.2 Internal analog reference

All electrical characteristics are valid for the following conditions unless otherwise noted:
-40 °C ≤ T_{amb} ≤ +105 °C
$V_{SAT\_OFF(min)} \leq V_{SAT} \leq V_{SAT(max)}$

Table 20. **Internal analog reference**

Symbol	Parameter	Conditions / Comments	Min	Typ	Max	Unit
V_{BG1}	Bandgap reference	-	-1%	1.2	+1%	V
V_{BG2}	Bandgap monitor	-	-1%	1.2	+1%	V
V_{ADC_GROUND}	ADC ground reference	ADC total error included	90	104	120	mV
$V_{ADC\_FULLSCALE}$	ADC full scale reference	-	-1.5%	2.5	+1.5%	V

13.3 Internal regulators

All electrical characteristics are valid for the following conditions unless otherwise noted:
-40 °C ≤ T_{amb} ≤ +105 °C
$V_{SAT\_ON(max)} \leq V_{SAT} \leq V_{SAT(max)}$

Table 21. **Internal regulator DC specifications**

Symbol	Parameter	Conditions / Comments	Min	Typ	Max	Unit
$V_{OUT\_VINT3V3}$	VINT3V3 output voltage	-	3.14	3.3	3.46	V
$V_{OV\_VINT3V3}$	VINT3V3 over voltage	-	3.47		3.7	V
$V_{UV\_VINT3V3}$	VINT3V3 under voltage	-	2.97		3.13	V
V_{OUT_CVDD}	CVDD output voltage	-	3.14	3.3	3.46	V
I_{OUT_CVDD}	CVDD current capability	External load is not allowed	-	-	50	mA
I_{LIM_CVDD}	CVDD current limit	-	80	-	-	mA
V_{OV_CVDD}	CVDD over voltage	-	3.47	-	3.7	V
V_{UV_CVDD}	CVDD under voltage	-	2.7	-	2.9	V
C_{CVDD}	CVDD output capacitance	Design Info	60	100	140	nF

Table 22. **Internal regulators AC specifications**

Symbol	Parameter	Comments / Conditions	Min	Typ	Max	Unit
$T_{FLT\_VINT\_CVDD\_OV}$	Internal regulator over voltage	-	10	17	25	µs

Symbol	Parameter	Comments / Conditions	Min	Typ	Max	Unit
	deglitch filter time					
$T_{FLT\_VINT\_CVDD\_UV}$	Internal regulator under voltage deglitch filter time	-	10	17	25	µs

13.4 Oscillators

All electrical characteristics are valid for the following conditions unless otherwise noted:
-40 °C ≤ T_{amb} ≤ +105 °C
$V_{SAT\_ON(max)} \leq V_{SAT} \leq V_{SAT(max)}$

Table 23. Oscillators AC specifications

Symbol	Parameter	Conditions / Comments	Min	Typ	Max	Unit
f_{OSC}	Main oscillator average frequency	-	15.2	16	16.8	MHz
f_{MOD_OSC}	Main oscillator modulation frequency	SPI_CLK_CNF (MAIN_SS_DIS=0) Design Info	f_{OSC}(min)/128	f_{OSC}(typ)/128	f_{OSC}(max)/128	MHz
I_{MOD_OSC}	Main oscillator modulation index	SPI_CLK_CNF (MAIN_SS_DIS=0)	2	4	6	%
f_{AUX}	Aux oscillator average frequency	-	7.125	7.5	7.875	MHz
f_{MOD_AUX}	Aux oscillator modulation frequency	SPI_CLK_CNF (AUX_SS_DIS=0) Design Info	f_{AUX}(min)/128	f_{AUX}(typ)/128	f_{AUX}(max)/128	MHz
I_{MOD_AUX}	Aux oscillator modulation index	SPI_CLK_CNF (AUX_SS_DIS=0)	2	4	6	%
$f_{OSC\_LOW\_TH}$	Main oscillator low frequency detection threshold	-	f_{AUX}(min)*(128/174)	f_{AUX}(typ)*(128/174)	f_{AUX}(max)*(128/174)	MHz

13.5 Reset

All electrical characteristics are valid for the following conditions unless otherwise noted:
-40 °C ≤ T_{amb} ≤ +105 °C
$V_{SAT\_ON(max)}$ ≤ V_{SAT} ≤ $V_{SAT(max)}$

Table 24. Reset Specifications

Symbol	Parameter	Comments / Conditions	Min	Typ	Max	Unit
V_{IH_RESET}	RESET high level input voltage	-	2	-	-	V
V_{IL_RESET}	RESET low level input voltage	-	-	-	0.8	V
I_{PD_RESET}	RESET pull down current	RESET = VCC	20	45	70	uA
$T_{FLT\_RESET\_N}$	RESET deglitch filter time	-	26	30	34	µs

13.6 SPI interface

All electrical characteristics are valid for both Global and Remote Sensor SPI and for the following conditions unless otherwise noted:
-40 °C ≤ T_{amb} ≤ +105 °C
$V_{SAT\_ON(max)}$ ≤ V_{SAT} ≤ $V_{SAT(max)}$
$V_{CCx(min)}$ ≤ V_{CCx} ≤ $V_{CCx(max)}$
V_{CC} = 3.3 V or 5 V

Table 25. Global and remote sensor SPI DC specifications

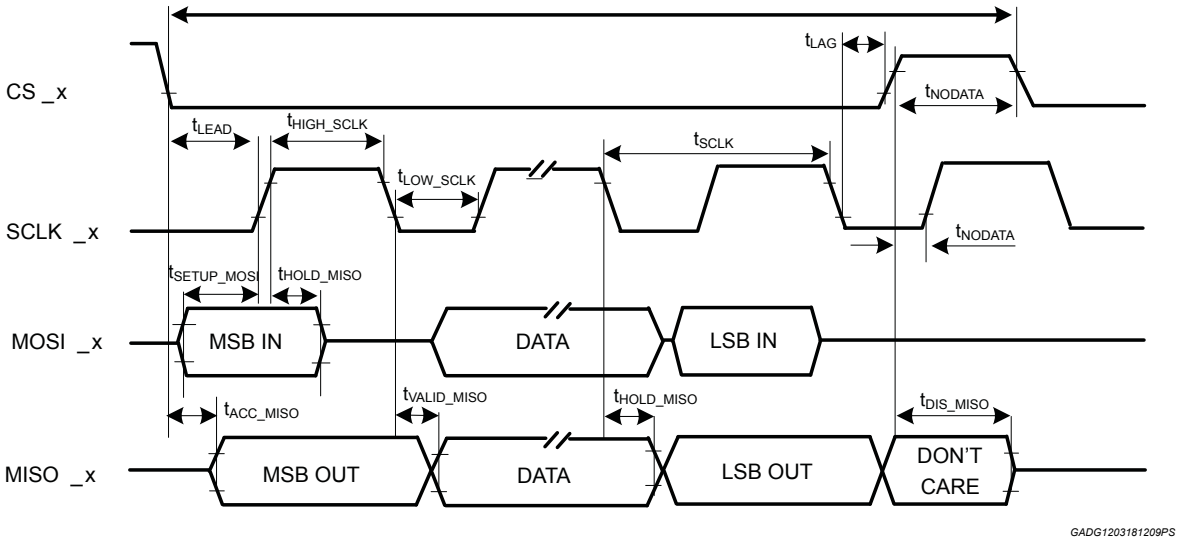
Symbol	Parameter	Comments / Conditions	Min	Typ	Max	Unit
$V_{IH\_CS\_G}$ $V_{IH\_CS\_RS}$	CS_x high level input voltage	-	2	-	-	V
$V_{IL\_CS\_G}$ $V_{IL\_CS\_RS}$	CS_x low level input voltage	-	-	-	0.8	V
$I_{PU\_CS\_G}$ $I_{PU\_CS\_RS}$	CS_x pull-up current	CS_x = 0 V	-70	-45	-20	µA
$V_{IH\_MOSI\_G}$ $V_{IH\_MOSI\_RS}$	MOSI_x high level input voltage	-	2	-	-	V
$V_{IL\_MOSI\_G}$ $V_{IL\_MOSI\_RS}$	MOSI_x low level input voltage	-	-	-	0.8	V
$I_{PD\_MOSI\_G}$ $I_{PD\_MOSI\_RS}$	MOSI_x pull-down current	MOSI_x = V_{CC}	20	45	70	µA
$V_{IH\_SCLK\_G}$ $V_{IH\_SCLK\_RS}$	SCLK_x high level input voltage	-	2	-	-	V
$V_{IL\_SCLK\_G}$ $V_{IL\_SCLK\_RS}$	SCLK_x low level input voltage	-	-	-	0.8	V
$I_{PD\_SCLK\_G}$ $I_{PD\_SCLK\_RS}$	SCLK_x pull-down current	SCLK_x = V_{CC}	20	45	70	µA
$V_{OH\_MISO\_G}$ $V_{OH\_MISO\_RS}$	MISO_x high level output voltage	I_{LOAD} = -800 µA	VCC-0.5	-	VCC	V
$V_{OL\_MISO\_G}$ $V_{OL\_MISO\_RS}$	MISO_x Low level output voltage	I_{LOAD} = 2.0 mA	-	-	0.4	V
$I_{LKG\_MISO\_G}$ $I_{LKG\_MISO\_RS}$	MISO_x output leakage	Tri-state leakage	-10	-	10	µA

Table 26. SPI AC specifications

Symbol	Parameter	Comments / Conditions	Min	Typ	Max	Unit
F_{SCLK}	SPI transfer frequency	-	-	8	8.08	MHz
t_{SCLK}	SCLK_x period	-	123.8	-	-	ns
t_{LEAD}	Enable lead time	-	250	-		ns
t_{LAG}	Enable lag time	-	50	-	-	ns
t_{HIGH_SCLK}	SCLK_x high time (5)	-	40	-	-	ns
t_{LOW_SCLK}	SCLK_x low time	-	40	-	-	ns
t_{SETUP_MOSI}	MOSI_x input setup time	-	20	-	-	ns
t_{HOLD_MOSI}	MOSI_x input hold time	-	20	-	-	ns
t_{ACC_MISO}	MISO_x access time	80 pF load	-	-	60	ns
t_{DIS_MISO}	MISO_x disable time	80 pF load	-	-	100	ns
t_{VALID_MISO}	MISO_x output valid time	80 pF load	-	-	30	ns
t_{HOLD_MISO}	MISO_x output hold time	80 pF load Design info	0	-	-	ns
t_{NODATA}	SCLK_x hold time	-	20	-	-	ns
t_{FLT_CS}	CS_x noise glitch rejection time	-	50	-	300	ns
t_{NODATA}	SPI linterframe time	-	400	-	-	ns

Note: All timings are shown with respect to 10% and 90% of the actual delivered VCC voltage.

Figure 28. SPI timing diagram



13.7 Deployment drivers

All electrical characteristics are valid for the following conditions unless otherwise noted:
-40 °C ≤ T_{amb} ≤ +105 °C
$V_{SAT\_ON(max)}$ ≤ V_{SAT} ≤ $V_{SAT(max)}$
6 V ≤ SSxy ≤ 35 V
SSxy – SFx ≤ 25 V

Table 27. Deployment drivers – DC specifications

Symbol	Parameter	Comments / Conditions	Min	Typ	Max	Unit	Note
I_{DEPL_LO}	Deployment current	R = 2 ohms Considering 9 mA as not detected leakage with a 1 k Ohm equivalent resistance from SFx to GND	1.33	1.4	1.6	A	-
I_{DEPL_HI}	Deployment current	R = 2 ohms, 9 V ≤ SSxy Considering 13.5 mA as not detected leakage with a 1 kOhm equivalent resistance from SFx to GND,	1.94	1.99	2.3	A	-
I_{TH_DEPL}	Deployment current counter threshold	-	I_{DEPLx} * 90%			A	-
I_{OC_SR}	Low-side over current detection	-	2.2	3.1	4.0	A	-
I_{LIM_SR}	Low-side current limitation	-	2.2	3.1	4.0	A	-
$\Delta I_{LIM\_OC\_SR}$	Difference between current limitation and OC threshold	I_{LIM_SR} - I_{OC_SR}	0.1	-	-	mA	-
R_{DSON_HSLS}	Combined high-side MOS + low-side MOS on resistances	T_{amb} = 105 °C	-	-	2.2	Ω	-
I_{REV_SF}	Reverse current on SFx	Not to be tested in series production	-	-	-100	mA	Without device malfunction (1)
$I_{LKG\_SS\_OFF}$	SSxy leakage current	Device OFF SSxy ≤ 35 V SFx = SFy = 0 Assuming all SSxy at the same voltage.	-10	-	40	µA	-
$I_{LKG\_SS\_ON\_1CH}$	SSxy leakage current	Device ON SSxy ≤ 35 V SFx = 0 SSxy Leakage current of each channel (32 µA) plus 30 µA due to 600 KOhm between ESD SQUIB/ PYROSWITCH rail and ground. Assuming all SSxy at the same voltage. Not Tested.	20	62	75	µA	-
$I_{LKG\_SS\_ON}$	SSxy leakage current	Device ON SSxy ≤ 35 V SFx = SFy = 0 Total SSxy leakage current with both x and y channels NOT armed (= 2 * 32 µA) plus 30 µA due to 600 KOhm between ESD SQUIB/ PYROSWITCH rail and ground. Assuming all SSxy at the same voltage.	40	94	120	µA	-
$I_{LKG\_SS\_CH\_ARMED}$	SSxy leakage current	Device ON SSxy ≤ 35 V SFx = 0 Total SSxy leakage current with only one channel armed (=490 + 32 µA) plus 30 µA due to 600 KOhm between ESD SQUIB/PYROSWITCH rail and ground. Assuming all SSxy at the same voltage.	390	552	640	µA	-
$I_{LKG\_SS\_2CH\_ARMED}$	SSxy leakage current	Device ON SSxy ≤ 35 V SFx = SFy = 0 Total SSxy leakage current with both x and y channels armed (= 2* 490 µA) plus 30 µA due to 600 KOhm between ESD SQUIB/ PYROSWITCH rail and ground.	800	1010	1230	µA	-

Symbol	Parameter	Comments / Conditions	Min	Typ	Max	Unit	Note
		Assuming all SSxy at the same voltage. Not Tested					
$I_{LKG\_SF\_ON\_0V}$	SF leakage current	Device ON, VSYNC = SSxy = 35 V, SFx = 0 V	-5	-	5	µA	-
$I_{LKG\_SF\_ON\_35V}$	SF leakage current	Device ON, VSYNC = SSxy = 35 V, SFx = 35 V	-5	-	50	µA	-
$I_{LKG\_SF\_OFF\_0V}$	SF leakage current	Device OFF VSYNC = open, SSxy = open but all SSxy pins connected, SFx = 0V	-5	-	5	µA	-
$I_{LKG\_SF\_OFF\_35V}$	SF leakage current	Device OFF VSYNC = open, SSxy = open but all SSxy pins connected, SFx = 35 V	-5	-	50	µA	-
$I_{LKG\_SR\_ON}$	SR leakage current	Device ON, VSYNC = SSxy = 35 V, SRx = 0 V-35	-5	-	50	µA	-
$I_{LKG\_SR\_OFF}$	SR leakage current	DEVICE OFF, VSYNC=open, SSxy = open but all SSxy pins connected, SRx pull down current OFF SRx = 0 V-20V	-5	-	50	µA	-
$I_{LKG\_SR\_OFF\_H}$	SR leakage current_H	DEVICE OFF, VSYNC=open, SSxy = open but all SSxy pins connected, SRx pull down current OFF SRx = 35 V	-5	-	30	mA	-
V_{SR_CLAMP}	SR voltage clamp		35	-	40	V	-
L_{DEPL}	Load inductance	Design info	0	-	56	µH	Maximum load inductance(2)
C_{SFx}	Load capacitance	Maximum capacitance to GND Design info	13	-	455	nF	-
C_{SRx}	Load capacitance	Maximum capacitance to GND Design info	13	-	455	nF	-
C_{SSxy}	SSxy capacitance	Maximum capacitance to GND connected directly to SSxy pin Design info	-	-	10	nF	-
R_{SFLx}	Load impedance	Design info	-	-	6.5	Ω	-
-	Wire length	Squib/Pyroswitch Loops containing a clock spring shall be limited to a maximum length of 3m	1		10	m	-
R_{Wirex}	Wire resistance	Design info	16.8		63.4	mΩ/m	-
L_{Wirex}	Wire Inductance	Design info	0.6		1.8	µH/m	-
R_{CSx}	Clock spring resistance	Maximum number of clock springs is 3 for any IC Design Info	0		0.7	Ω	
L_{CSx}	Clock spring inductance	Design Info	0		42.9	µH	
$k_{L_{CS1} - L_{CS2}}$	Clock spring coupling	Design Info	0.739		0.903		
L_{EMI}	Squib/Pyroswitch EMI protection	Design Info	0		7.7	µH	

1. *In case of an unsupplied device and shorted deployment pins (e.g. to battery voltage), the dynamic reverse current through the high side power stage depends on CSSxy.*
2. *see LDEPL calculation*

LDEPL calculation

LDEPL could be calculated in the following way:

- Non-Clock Spring Loops
  $L_{DEPL}(max) = L_{Wire}(10m \times 2) + L_{EMI} = (3.6\mu H/m \times 10m) + 7.7\mu H = 43.7\mu H$
- Clock Spring Loops
  $L_{Wire}(3m \times 2) + 2 \times L_{CSx} + L_{EMI} - \left(2 \times k_{L\_Cx} \times \sqrt{(L_{\_CS1} \times L_{\_CS2})}\right) = (3.6\mu H/m \times 3m) + (2 \times 42.9\mu H) + 7.7\mu H - (2 \times 0.739 \times 42.9\mu H) = 40.9\mu H$
- Clock Spring Loops with short to ground
  $L_{DEPL}(max) = L_{Wire}(3m) + L_{CSx} + L_{EMI} = (1.8\mu H/m \times 3m) + 49.2\mu H + 7.7\mu H = 56\mu H$

Figure 29. Deployment drivers diagram

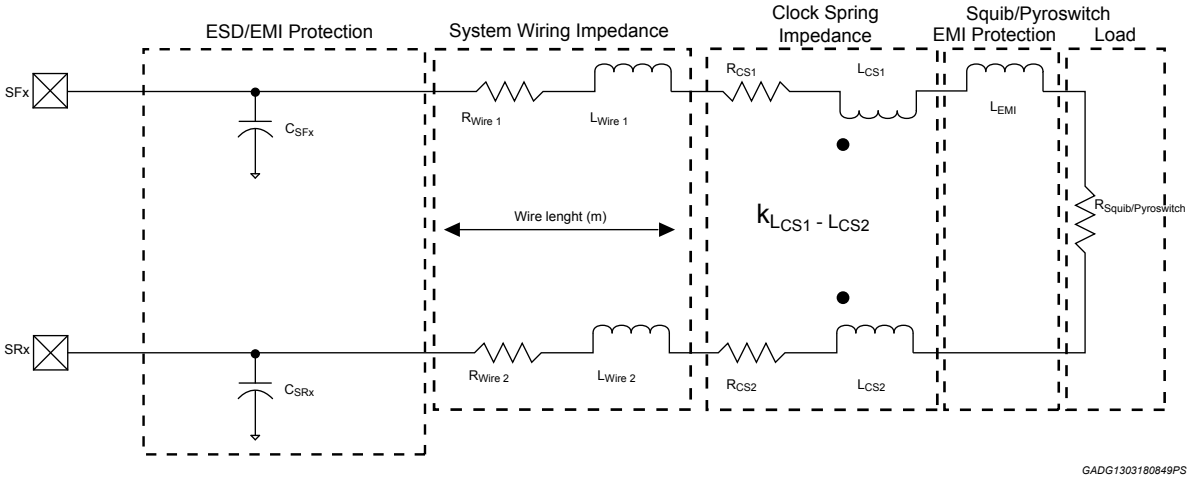


Table 28. Deployment Drivers – AC Specifications

Symbol	Parameter	Comments / Conditions	Min	Typ	Max	Unit
T_{DEPL}	Deployment time	DCR_x(Dep_Current) = I_{DEPL_LO} ≥ 1.209 A rising to 1.209 A falling; DCR_x(Dep_Current) = I_{DEPL_HI} ≥ 1.764 A rising to 1.764 A falling T_{DEPL} = DCR_x(Deploy_Time)* $T_{DEP\_TIME\_RES}$ - TDEL_IDEP	DCR_x(Deploy_Time)* $T_{DEP\_TIME\_RES}$ - 65	-	DCR_x(Deploy_Time)* $T_{DEP\_TIME\_RES}$	µs
$T_{DEP\_TIME\_RES}$	DCR_x deploy time resolution	-	1024/F_{OSC}(min)	1024/ F_{OSC}(typ)	1024/F_{OSC}(max)	µs
$T_{DEP\_CC\_RES}$	Deployment current counter resolution	-	256/F_{OSC}(min)	256/ F_{OSC}(typ)	256/F_{OSC}(max)	µs
T_{RISE_IDEPL}	Rise time 10% - 90% of I_{DEPL}	SSxy = 25 V, R_{SQ} = 2.2 ohm, C = 22 nF L = 44 µH	-	-	32	µs
T_{DEL_IDEP}	Delay time SPI_CS to 90% I_{DEPL}	SSxy = 25 V, R_{SQ} = 2.2 ohm, C = 22 nF L = 44 µH	-	-	65	µs
T_{FALL_IDEPL}	Fall time 90% - 10% I_{DEPL}	SSxy = 25 V, R_{SQ} = 2.2 ohm, C = 22 nF L = 44 µH	-	-	32	µs
$T_{DEL\_SD\_LS}$	Low-side shutdown delay time (with respect to high-side deactivation)	-	50	-	-	µs

Symbol	Parameter	Comments / Conditions	Min	Typ	Max	Unit
$T_{FLT\_ILIM\_LS}$	Low-side Overcurrent to low-side deactivation deglitch time in short to battery condition	-	80	100	120	µs
$T_{FLT\_OS\_LS}$	Low-side overcurrent to high-side deactivation deglitch time in case of intermittent open to squib/pyroswitch condition	-	-	-	20	µs
$T_{OFF\_OS\_HS}$	High-side off time in case of intermittent open to squib/ pyroswitch condition	-	4	-	12	µs

13.8 Deployment driver diagnostic

13.8.1 Squib/Pyroswitch resistance measurement

All electrical characteristics are valid for the following conditions unless otherwise noted:

$-40\ °C \le T_{amb} \le +105\ °C$

$V_{SAT\_ON(max)} \le V_{SAT} \le V_{SAT(max)}$

$6\ V \le SSxy \le 35\ V$

$7\ V \le V_{SYNC} \le 35\ V$

Table 29. Deployment drivers diagnostics - squib/pyroswitch resistance measurement

Symbol	Parameter	Comments / Conditions	Min	Typ	Max	Unit
$R_{SQ\_RANGE\_1}$	Squib/Pyroswitch resistance range 1	LPDIAGREQ(ISRC_CURR_SEL)=0	0		10.0	Ω
$R_{SQ\_RANGE\ 2}$	Squib/Pyroswitch resistance range 2	LPDIAGREQ(ISRC_CURR_SEL)=1	0		50.0	Ω
G_{RSQ}	Squib/Pyroswitch resistance measurement differential amplifier gain	$V_{OUT\_RSQ} = G_{RSQ} \times [(V_{SF} - V_{SR})] + V_{off\_RSQ}$	-2%	5.2	+2%	V/V
V_{off_RSQ}	Squib/Pyroswitch resistance measurement differential amplifier offset	$V_{OUT\_RSQ} = G_{RSQ} \times [(V_{SF} - V_{SR})] + V_{off\_RSQ}$	200		400	mV
$I_{SRC\_HI\_SF}$ $I_{SRC\_HI\_SR}$	Squib/Pyroswitch resistance measurement high current source	LPDIAGREQ(ISRC_CURR_SEL)=0 LPDIAGREQ(ISRC)="01" or "10"	-5%	40	+5%	mA
$I_{SRC\_LO\_SF}$ $I_{SRC\_LO\_SR}$	Squib/Pyroswitch resistance measurement low current source	LPDIAGREQ(ISRC_CURR_SEL)=1 LPDIAGREQ(ISRC)="01" or "10"	-10%	8	+10%	mA
I_{SRC_DELTA}	Squib/Pyroswitch resistance measurement delta current source	$I_{SRC\_HI\_x} - I_{SRC\_LO\_x}$	-5%	32	+5%	mA
SR_{ISRC}	Squib/Pyroswitch resistance measurement current source slew-rate	-	3	7.5	12	mA/µs
V_{SRx_RM}	SRx voltage during resistance measurement	LPDIAGREQ(ISRC)="01" or "10" LPDIAGREQ(ISINK)=1	0.4	0.7	1.2	V
$I_{SINK\_HI\_SR}$	SRx current sink limit high	LPDIAGREQ(ISRC_CURR_SEL)=0 LPDIAGREQ(ISINK)=1	50	75	100	mA

Symbol	Parameter	Comments / Conditions	Min	Typ	Max	Unit
$I_{SINK\_LO\_SR}$	SRx current sink limit low	LPDIAGREQ(ISRC_CURR_SEL)=1 LPDIAGREQ(ISINK)=1	10	17.5	25	mA
$I_{PD\_SR\_L}$	SRx current pull-down	SYS_CTL(PD&VRCM_SEL) = 0	0.7	1	1.3	mA
$I_{PD\_SR\_H}$	SRx current pull-down	SYS_CTL(PD&VRCM_SEL) = 1	4.5	6	7.5	mA
R_{LKG_SF}	SFx leakage resistance	Design info	1	-		kΩ
V_{LKG_SF}	SFx leakage voltage source	Design info	-1	-	18	V
R_{SQ_ACC}	Squib/Pyroswitch resistance measurement accuracy	After software calculation. All errors included R_{SQ} between 1.0 Ω and 10.0 Ω With High Current Source (40 mA)	-8%	-	+8	%
-	EMI Input Low-pass filter	Design Info	50	-	100	kHz

13.8.2 Squib/Pyroswitch leakage test (VRCM)

All electrical characteristics are valid for the following conditions unless otherwise noted:
-40 °C ≤ T_{amb} ≤ +105 °C
$V_{SAT\_ON(max)} \le V_{SAT} \le V_{SAT(max)}$

Table 30. Squib/Pyroswitch leakage test (VRCM)

Symbol	Parameter	Comments / Conditions	Min	Typ	Max	Unit
$V_{OUT\_VRCM\_0}$	Output voltage on SF or SR pins during leakage test	I_{OUT} = 0 mA	-10%	2.5	+10%	V
V_{OUT_VRCM}		I_{OUT} = 6.6 mA	1.9	-	2.5	V
$R_{LKG\_GSG\_TH}$	Detection threshold, leakage to GND	Leakage detected if $R_{LKG\_GSG} \le 1$ kΩ and not detected if $R_{LKG\_GSG} \ge 10$ kΩ Design info	1	-	10	kΩ
$I_{LKG\_GSQ\_TH\_L}$	Detection threshold, leakage to GND	Equivalent to resistance range SYS_CTL(PD&VRCM_SEL) = 0 -25 °C ≤ T_j ≤ +150 °C guaranteed by design/characterization	-15.5%	450	+20%	µA
		Equivalent to resistance range SYS_CTL(PD&VRCM_SEL) = 0 -40 °C ≤ T_j ≤ +150 °C	-17%	450	+20%	µA
$I_{LKG\_GSQ\_TH\_H}$	Detection threshold, leakage to GND	SYS_CTL(PD&VRCM_SEL) = 1	-15%	2	15%	mA
$T_{FLT\_LKG\_G}$	Leakage to GND deglitch filter time	-	17	20	23	µs
$R_{LKG\_BSQ\_TH}$	Detection threshold, leakage to battery	Leakage detected if $R_{LKG\_GSG} \le 1$ kΩ and not detected if $R_{LKG\_GSG} \ge 10$ kΩ Design info	1	-	10	kΩ
$I_{LKG\_BSQ\_TH}$		Equivalent to resistance range -25 °C ≤ T_j ≤ +150 °C guaranteed by design/characterization	-12%	1.8	+15%	mA
		-40 °C ≤ T_j ≤ +150 °C	-12%	1.8	+20%	mA
$T_{FLT\_LKG\_B}$	Leakage to BAT deglitch filter time	-	17	20	23	µs
$I_{LIM\_VRCM\_SRC}$	VRCM current limitation	-	-20	-	-10	mA
$I_{LIM\_VRCM\_SINK}$	VRCM current limitation	-	10	-	20	mA
V_{SHIFT}	External ground or battery shift	Design info	-1	-	+1	V
$R_{SQ\_LOW\_TH}$	Detection Threshold for “resistance too low”	Design Info	200	-	500	Ω

Symbol	Parameter	Comments / Conditions	Min	Typ	Max	Unit
$I_{RSQ\_LOW\_TH}$	Detection threshold for “resistance too low”	Equivalent to resistance range -25 °C ≤ T_j ≤ +150 °C guaranteed by design/characterization	-12%	6	+17%	mA
		-40 °C ≤ T_j ≤ +150 °C	-12%	6	+22%	mA
T_{FLT_RLOW}	“Resistance too low” deglitch filter time	-	12	15	18	µs
R_{SQ_HIGH}	Detection threshold for “resistance too high”	Design info	2	-	5	kΩ
I_{RSQ_HIGH}	Detection threshold for “resistance too high”	Equivalent to resistance range -25 °C ≤ T_j ≤ +150 °C guaranteed by design/characterization	-17%	700	+20%	µA
		-40 °C ≤ T_j ≤ +150 °C	-17%	700	+22%	µA
T_{FLT_RHIGH}	“Resistance too high” deglitch filter time	-	12	15	18	µs
$T_{delay\_STG\_selection}$	Time needed to change the VRCM STG thresholds (450 µA-to-2 mA or 2 mA-to-450 µA)	guaranteed by design	-	-	2	µs

13.8.3 High/low-side FET test

All electrical characteristics are valid for the following conditions unless otherwise noted:

-40 °C ≤ T_{amb} ≤ +105 °C

$V_{SAT\_ON(max)} \leq V_{SAT} \leq V_{SAT(max)}$

6 V ≤ SSxy ≤ 35 V

7 V ≤ V_{SYNC} ≤ 35 V

Table 31. High/low-side FET test

Symbol	Parameter	Comments / Conditions	Min	Typ	Max	Unit
$I_{HS\_FET\_TH}$	Detection threshold high side FET test		-12%	1.8	+12%	mA
$I_{LS\_FET\_TH}$	Detection threshold low side FET test	SYS_CTL(PD&VRCM_SEL) = 0	-15.5%	450	+15.5%	µA
$I_{LS\_FET\_TH\_HIGH}$		SYS_CTL(PD&VRCM_SEL) = 1	-15%	2	15%	
E_{FET_TEST}	Energy transferred to squib/pyroswitch during HS/LS FET tests	Design info	-	-	170	µJ
T_{DRIVER_DIS}	Driver disable time	Guaranteed by design	-	-	1.5	µs
$T_{TOT\_FETTEST\_ACTIVE}$	Total FET test activation time in case of no fault condition	Guaranteed by design	-	-	4	µs
$T_{FETTIMEOUT}$	HS/LS FET test timeout	-	190	200	210	µs
$T_{FLT\_LKGB\_FT}$	Deglitch filter time during FET test on IHS_FET_TH / ILS_FET_TH current thresholds	-	0.8	1	1.2	µs
$SGxy_{\_OPEN}$	Squib/Pyroswitch open ground detection	GNDD as ground reference	300	450	600	mV
T_{FLT_SGOPEN}	Squib/Pyroswitch open ground detection filter time	-	46	50	54	µs

13.8.4 Deployment timer test

All electrical characteristics are valid for the following conditions unless otherwise noted:
-40 °C ≤ T_{amb} ≤ +105 °C
$V_{SAT\_ON(max)}$ ≤ V_{SAT} ≤ $V_{SAT(max)}$

Table 32. Deployment timer test - AC specifications

Symbol	Parameter	Comments / Conditions	Min	Typ	Max	Unit
t_{PULSE_PERIOD}	Deployment timer pulse test period time	SYSDIAGREQ(DSTEST)=PULSE	7	8	9	ms
t_{PULSE_HIGH}	Deployment timer pulse test high time	SYSDIAGREQ(DSTEST)=PULSE	-	DCR_x(Deploy_Time)* $T_{DEP\_TIME\_RES}$	-	µs

13.9 Remote sensor interface

All electrical characteristics are valid for the following conditions unless otherwise noted:

$-40\ °C \le T_{amb} \le +105\ °C$

$V_{SAT\_ON(max)} \le V_{SAT} \le V_{SAT(max)}$

$V_{VSAT}(min) \le VSAT$

$V_{VSYNC}(min) \le VVSYNC$

13.9.1 PSI-5 interface

Table 33. PSI-5 satellite transceiver - DC specifications

Symbol	Parameter	Comments / Conditions	Min	Typ	Max	Unit
I_{RSU}	Interface quiescent current	Design info	-35	-	-4	mA
V_{RSU_MAX}	Max. output voltage excluding sync. pulse	(internal regulation, VSAT=VSYNC)	-	-	11	V
$V_{RSU\_SYNC\_MAX}$	Max. output voltage including sync. pulse	(internal regulation)	-	-	16.5	V
R_{RSU}	RSU Output resistance	From I_{RSU} = -4 mA to -65 mA	3	-	9.5	Ω
I_{STB_TH}	Static reverse current into VSAT or VSYNC pin (V_{SUPPLY})	$V_{RSUx} > V_{SUPPLY} + V_{RSU\_STB}$	0.0	-	10	mA
V_{RSU_STB}	Output short to battery threshold	-	10.0	-	100	mV
I_{OCTH_PSI5}	Over current detection threshold	Interface disabled after $T_{FLT\_OCTH\_PSI5}$	-130	-	-66	mA
I_{LIM_PSI5}	Output Current Limit	I_{RSUx}	-130	-	-80	mA
$\Delta I_{LIM\_OC\_PSI5}$	Difference between current limitation and OC threshold	$ABS(I_{LIM\_RSU}) – ABS(I_{OC\_RSU})$	1	-	-	mA
I_{BO}	Base Current	Default value	-15%	-15	+15%	mA
I_{THGND}	Leakage to ground fault current detection	To ground; detected by I_B	-50.4	-42	-35	mA
I_{THOPEN}	Output open load detection threshold	Tested with tighter limits at HOT (-3.5 mA < ITHOPEN < -0.5 mA)	-4.2	-	-0.2	mA
DAC_{RES}	DAC resolution	Design info	-	10	-	Bit
I_{LSB}	LSB current	Design info	-	93.75	-	µA
V_{t2}	Sync pulse amplitude	$I_{RSUbase}$ = -4 mA to - 35 mA $V_{VSYNC} \ge V_{RSUbase}$ +4.8 V Referred to V_{RSUx} voltage before sync pulse ($V_{RSUbase}$)	3.8	-	-	V
V_{t2_low}	Sync pulse amplitude for min VSYNC-VSAT	$I_{RSUbase}$ = -4 mA to - 35 mA $V_{VSYNC} \ge V_{RSUbase}$ +4.2 V Referred to V_{RSUx} voltage before sync pulse ($V_{RSUbase}$)	3.61	-	-	V
$V_{SYNCDROP}$	Sync Drop-out voltage	$V_{VSYNC} - V_{t2} - V_{RSUx}$ Design info	1	-	-	V
$I_{LIM\_SYNC\_LS}$	Sync pulse current limit (LS driver)	-	50	-	80	mA
I_{LIM_SYNC}	Static current limitation for each transceiver output RSUx	During sync pulse generator V_{RSUx} = GND $V_{VSYNC} \le 14.75$ V	-240	-	-120	mA
I_{LIM_SYNC}	Static current limitation for each transceiver output RSUx	During sync pulse generator V_{RSUx} = GND	-260	-	-120	mA

Symbol	Parameter	Comments / Conditions	Min	Typ	Max	Unit
		V_{VSYNC} ≤ 35 V				
C_1	Capacitor on RSUx pin	22 nF nominal Design info	13	-	-	nF
R_{E2}	RSU damping resistance	Design info	-	2.5	-	Ω
C_2	ECU pin capacitance	5 nF nominal Design information, not tested	4	-	6	nF
-	Total number of sensors connected to bus	Design info	1	-	3	-
$V_{IH\_SATSYNC}$	SATSYNC high level input voltage	-	2	-	-	V
$V_{IL\_SATSYNC}$	SATSYNC low level input voltage	-	-	-	0.8	V
$I_{PD\_SATSYNC}$	SATSYNC Pull-down current	SATSYNC = VCC	20	45	70	µA
T_{JSD_RSU}	Thermal shutdown threshold	-	150	175	190	°C
T_{HYS_TSDRSU}	Thermal shutdown threshold hysteresis		5	10	15	°C

Table 34. PSI-5 Satellite Transceiver - AC Specifications

Symbol	Parameter	Comments / Conditions	Min	Typ	Max	Unit
T_{Bit_125k}	Bit time (125 kbps mode)	At the sensor connector	7.6	8	8.4	µs
T_{Bit_189k}	Bit time (189 kbps mode)	At the sensor connector	5	5.3	5.6	µs
$T_{FLT\_OCTH\_PSI5}$	Over current detection deglitch filter time	Normal operation	500	-	600	µs
$T_{BLK\_OCTH\_PSI5}$	Over current detection blanking time	At interface power on (BLKTxSEL = 0)	4.6	-	5.4	ms
		At interface power on (BLKTxSEL = 1)	9.4	-	10.8	ms
T_{STBTH}	Reverse battery blocking enable time	-	12	-	16	µs
t_0	Reference time	@0.5 V on top of $VRSU_{base}$	-	0	-	-
t_1	Sync signal earliest start	@ VRSU+150 mV relative to t_0	-3	-	-	µs
T_{SYNC_START}	Start delay time	From SATSYNC to t_0 of channel 0	1.5	-	5	µs
t_2	Sync signal sustain start	@ VRSU+3.8 V relative to t_0	-	-	7	µs
SR_{RISE_RSU}	Sync slope rising slew rate	-	0.43	-	1.5	V/µs
SR_{FALL_RSU}	Sync slope falling slew rate	-	-1.5	-	-	V/µs
t_3	Sync signal sustain time	From t_0 to VRSU+3.8 V of falling edge	16	-	-	µs
t_4	Discharge time limit	From t0 to VRSU+150 mV of falling edge	-	-	35	µs
T_{BLANK}	Decoder blanking time(decoding disabled)	Design info	-	-	42	µs
T_{SYNC}	Time between two sync pulses	Design info	400	500	-	µs
$T_{FLT\_PSI5\_HF}$	PSI5 Deglitch filter time	F = 189 kbaud Configurable by SPI (4 bits)	1	-	2	µs

Symbol	Parameter	Comments / Conditions	Min	Typ	Max	Unit
$T_{FLT\_PSI5\_LF}$	PSI5 Deglitch filter time	F = 125 kbaud Configurable by SPI (4 bits)	1.5	-	2.5	µs
$T_{\_ES\_1}$, $T_{\_LS\_1}$	Message start time, Slot 1	Related to t_0, Sensor Side, P8P-500-3L	44	-	58.6	µs
		Related to t_0, Sensor Side, P8P-500-3H	44	-	58.6	µs
		Related to t_0, Sensor Side, P8P-500-4H	44	-	58.6	µs
		Related to t_0, Sensor Side, P10P-500-3L	44	-	58.6	µs
		Related to t_0, Sensor Side, P10P-500-3H	44	-	58.6	µs
		Related to t_0, Sensor Side, P10P-500-4H	44	-	58.6	µs
$T_{\_ES\_2}$, $T_{\_LS\_2}$	Message start time, Slot 2	Related to t_0, Sensor Side, P8P-500-3L	181.3	-	210.4	µs
		Related to t_0, Sensor Side, P8P-500-3H	181.3	-	210.4	µs
		Related to t_0, Sensor Side, P8P-500-4H	139.5	-	164.2	µs
		Related to t_0, Sensor Side, P10P-500-3L	181.3	-	210.4	µs
		Related to t_0, Sensor Side, P10P-500-3H	181.3	-	210.4	µs
		Related to t_0, Sensor Side, P10P-500-4H	139.5	-	164.2	µs
$T_{\_ES\_3}$, $T_{\_LS\_3}$	Message start time, Slot 3	Related to t_0, Sensor Side, P8P-500-3L	328.9	-	373.5	µs
		Related to t_0, Sensor Side, P8P-500-3H	328.9	-	373.5	µs
		Related to t_0, Sensor Side, P8P-500-4H	245.5	-	281.3	µs
		Related to t_0, Sensor Side, P10P-500-3L	328.9	-	373.5	µs
		Related to t_0, Sensor Side, P10P-500-3H	328.9	-	373.5	µs
		Related to t_0, Sensor Side, P10P-500-4H	245.5	-	281.3	µs
$T_{\_s1\_end\_open}$	Slot 1 End valid window, opening time	Related to t_0, Sensor Side, P8P-500-3L	107.2	-	127.6	µs
		Related to t_0, Sensor Side, P8P-500-3H	82.0	-	99.4	µs
		Related to t_0, Sensor Side, P8P-500-4H	82.0	-	99.4	µs
		Related to t_0, Sensor Side, P10P-500-3L	121.0	-	142.8	µs
		Related to t_0, Sensor Side, P10P-500-3H	91.0	-	109.4	µs
		Related to t_0, Sensor Side, P10P-500-4H	91.0	-	109.4	µs
$T_{\_s1\_end\_closure}$	Slot 1 End valid window, closure time	Related to t_0, Sensor Side, P8P-500-3L	151	-	174.6	µs
		Related to t_0, Sensor Side, P8P-500-3H	119.8	-	139.9	µs
		Related to t_0, Sensor Side, P8P-500-4H	119.8	-	139.9	µs
		Related to t_0, Sensor Side, P10P-500-3L	167.8	-	193.0	µs
		Related to t_0, Sensor Side, P10P-500-3H	131	-	152.5	µs
		Related to t_0, Sensor Side, P10P-500-4H	131	-	152.5	µs
$T_{\_s2\_end\_open}$	Slot 2 End valid window, opening time	Related to t_0, Sensor Side, P8P-500-3L	231.6	-	264.9	µs
		Related to t_0, Sensor Side, P8P-500-3H	206.0	-	236.7	µs
		Related to t_0, Sensor Side, P8P-500-4H	168.0	-	194.9	µs
		Related to t_0, Sensor Side, P10P-500-3L	245.4	-	280.1	µs
		Related to t_0, Sensor Side, P10P-500-3H	215.0	-	246.7	µs
		Related to t_0, Sensor Side, P10P-500-4H	177.5	-	205	µs

Symbol	Parameter	Comments / Conditions	Min	Typ	Max	Unit
$T_{\_s2\_end\_closure}$	Slot 2 End valid window, closure time	Related to t_0, Sensor Side, P8P-500-3L	302.8	-	342.1	µs
		Related to t_0, Sensor Side, P8P-500-3H	271.6	-	308.0	µs
		Related to t_0, Sensor Side, P8P-500-4H	225.4	-	256.5	µs
		Related to t_0, Sensor Side, P10P-500-3L	319.6	-	360.5	µs
		Related to t_0, Sensor Side, P10P-500-3H	282.7	-	320.0	µs
		Related to t_0, Sensor Side, P10P-500-4H	236.5	-	269.0	µs
$T_{\_s3\_end\_open}$	Slot 3 End valid window, opening time	Related to t_0, Sensor Side, P8P-500-3L	365.1	-	412.5	µs
		Related to t_0, Sensor Side, P8P-500-3H	339.4	-	384.3	µs
		Related to t_0, Sensor Side, P8P-500-4H	263.9	-	300.9	µs
		Related to t_0, Sensor Side, P10P-500-3L	378.9	-	427.7	µs
		Related to t_0, Sensor Side, P10P-500-3H	348.5	-	394.3	µs
		Related to t_0, Sensor Side, P10P-500-4H	273.0	-	311	µs
$T_{\_s3\_end\_closure}$	Slot 3 End valid window, closure time	Related to t_0, Sensor Side, P8P-500-3L	465.9	-	522.7	µs
		Related to t_0, Sensor Side, P8P-500-3H	434.7	-	488.0	µs
		Related to t_0, Sensor Side, P8P-500-4H	342.5	-	386.1	µs
		Related to t_0, Sensor Side, P10P-500-3L	482.7	-	541.1	µs
		Related to t_0, Sensor Side, P10P-500-3H	445.9	-	500.0	µs
		Related to t_0, Sensor Side, P10P-500-4H	353.7	-	398.2	µs
$T_{SYNC\_DLY\_SHORT}$	Sync pulse start delay	SYS_CFG(RSU_SYNCPULSE_SHIFT_CONF)=1 Related to digital command that starts Sync Pulse on ch. N-1	-	160/ FOSC(typ)	-	µs
$T_{SYNC\_DLY\_LONG}$	Sync pulse start delay	SYS_CFG(RSU_SYNCPULSE_SHIFT_CONF)=0 Related to digital command that starts Sync Pulse on ch. N-1	-	288/ FOSC(typ)	-	µs
$T_{FLT\_OPEN\_RSU}$	Open detection deglitch filter time	-	10	-	15	µs
$T_{FLT\_LKG\_RSU}$	Leakage deglitch filter time	-	10	-	15	µs
$T_{WRITE\_EN\_DELAY\_LF}$	Data register write delay	Design info F = 125 kbaud Calculated from transition of last sensor data bit to when data is available in SPI register	9	-	19	µs
$T_{WRITE\_EN\_DELAY\_HF}$	Data register write delay	Design info F = 189 kbaud Calculated from transition of last sensor data bit to when data is available in SPI register	6	-	14	µs

13.10 Arming interface

All electrical characteristics are valid for the following conditions unless otherwise noted:
-40 °C ≤ T_{amb} ≤ +105 °C
$V_{SAT\_ON(max)}$ ≤ V_{SAT} ≤ $V_{SAT(max)}$
V_{CCx}(min) ≤ V_{CCx} ≤ V_{CCx}(max)
V_{CC} = 3.3 V or 5 V

Table 35. Arming interface – DC specifications

Symbol	Parameter	Comments / Conditions	Min	Typ	Max	Unit
V_{IH_FENx}	FENx high level input voltage	-	2	-	-	V
V_{IL_FENx}	FENx low level input voltage	-	-	-	0.8	V
I_{PD_FENx}	FEN1/FEN2 pull down current	FENx = V_{CC}	20	45	70	µA
I_{PD_FENL}	FENL passive pull down	FENL = V_{CC}	40	100	160	k
V_{OH_FENL}	FENL high level output voltage	I_{LOAD} = -800 µA	V_{CC}-0.5		V_{CC}	V
V_{OL_FENL}	FENL low level output voltage	I_{LOAD} = 2.0 mA			0.4	V

13.11 Analog-to-digital converter

All electrical characteristics are valid for the following conditions unless otherwise noted:
-40 °C ≤ T_{amb} ≤ +105 °C
$V_{SAT\_ON(max)}$ ≤ V_{SAT} ≤ 17.5 V

Table 36. Analog-to-digital converter

Symbol	Parameter	Comments / Conditions	Min	Typ	Max	Unit
V_{ADC_RANGE}	ADC input voltage range	Design info	0.1	-	2.5	V
V_{ADC_REF}	ADC reference voltage	-	-1.5%	2.5	+1.5%	V
ADC_RES	ADC resolution(1)	Design info	-	10	-	bit
DNL	Differential non linearity error (DNL)	Separation between adjacent levels, measured bit to bit of actual and an ideal output step. No missing codes	-1	-	+1	LSB
INL	Integral non linearity error (INL)	Maximum difference between the actual analog value at the transition between 2 adjacent steps and its ideal value	-3	-	+3	LSB
E_{QUANT}	Quantization error	Design info	-0.5	-	0.5	LSB
TotErr	Total error	Includes INL, DNL, ADC reference voltage tolerance and quantization error	-15	-	+15	LSB
TotErr_0v1	ADC total error for 0.1 V input voltage	-	-5	-	+5	LSB
TotErr_2v4	ADC total error for 2.4V input voltage	-	-15	-	+15	LSB
R_{LSB_1}	Reproducibility: conversion result variation for constant input signal	1x sampling measurements. Guaranteed by design	-6	-	6	LSB
R_{LSB_4}	Reproducibility: conversion result variation for constant input signal	4x sampling measurements. Guaranteed by design	-3	-	3	LSB
R_{LSB_8}	Reproducibility: conversion result variation for constant input signal	8x sampling measurements. Guaranteed by design	-2.5	-	2.5	LSB
Pre-ADC	Pre-ADC settling time	-	-	4.81	-	µs
T_SC	Single conversion time	-	-	2.25	-	µs

Symbol	Parameter	Comments / Conditions	Min	Typ	Max	Unit
IQ	Intra-queue settling time	-	-	3.5	-	µs
Post-ADC	Post- ADC settling time	-	-	3.44	-	µs
-	ADC conversion time - voltage	4x sampling for each of the 4 conversions in the queue Design info	-	54.75		µs
-	ADC conversion time – current and voltage	8x sampling for DCS, temperature and squib/ pyroswitch loop resistance measurements + 4x sampling for remaining 2 conversions in the queue Design info	-	51.25	-	µs

1. *LSB = (2.5 V / 1024) = 2.44 mV*

13.12 Voltage diagnostics (Analog MUX)

All electrical characteristics are valid for the following conditions unless otherwise noted:
-40 °C ≤ T_{amb} ≤ +105 °C
$V_{SAT\_ON(max)}$ ≤ V_{SAT} ≤ 17.5 V

Table 37. Voltage diagnostics (Analog MUX)

Symbol	Parameter	Comments / Conditions	Min	Typ	Max	Units
Ratio_1	Divider ratios	$V_{IN\_RANGE\_1}$ = 0.1 V … 2.5 V	-	1	-	V/V
Ratio_4	Divider ratios	$V_{INPUT\_RANGE\_4}$ = 1 V … 5.5 V	-3%	4	+3%	V/V
Ratio_7	Divider ratios	$V_{INPUT\_RANGE\_7}$ = 1.5 V … 17.5 V	-3%	7	+3%	V/V
Ratio_10	Divider ratios	$V_{INPUT\_RANGE\_10}$ = 2 V … 25 V	-3%	10	+3%	V/V
Ratio_15	Divider ratios	$V_{INPUT\_RANGE\_15}$ = 3 V … 35 V	-3%	15	+3%	V/V
Offset	Divider offset	High impedance	-10	-	10	mV
R_{RATIO_4}	Multiplexer input resistance	Multiplexer input to GNDA	80	-	-	kΩ
R_{RATIO_7}	Multiplexer input resistance	Multiplexer input to GNDA	120	-	-	kΩ
R_{RATIO_10}	Multiplexer input resistance	Multiplexer input to GNDA	160	-	-	kΩ
R_{RATIO_15}	Multiplexer input resistance	Multiplexer input to GNDA	200	-	-	kΩ
$I_{LEAK\_MUX\_ON}$	Additional multiplexer ON-state input leakage current	For all divider ratio expect Ratio_1	-	-	60	µA
V_{MEAS_ACC}	Voltage measurement accuracy	ADC total error (±15LSB) plus analog divider error (±3%)	-	-	-	-

13.13 Temperature sensor

All electrical characteristics are valid for the following conditions unless otherwise noted:
-40 °C ≤ T_{amb} ≤ +105 °C
$V_{SAT\_ON(max)}$ ≤ V_{SAT} ≤ 17.5 V

Table 38. Temperature sensor specifications

Symbol	Parameter	Comments / Conditions	Min	Typ	Max	Unit
T_{MON_RANGE}	Monitoring temperature range	-	-40	-	150	°C
T_{MON_ACC}	Monitoring temperature accuracy	-	-15	-	15	°C

14 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

14.1 TQFP48 (7x7x1 mm exp. pad down 5.0x5.0) package information

Figure 30. TQFP48 (7x7x1 mm exp. pad down 5.0x5.0) package outline

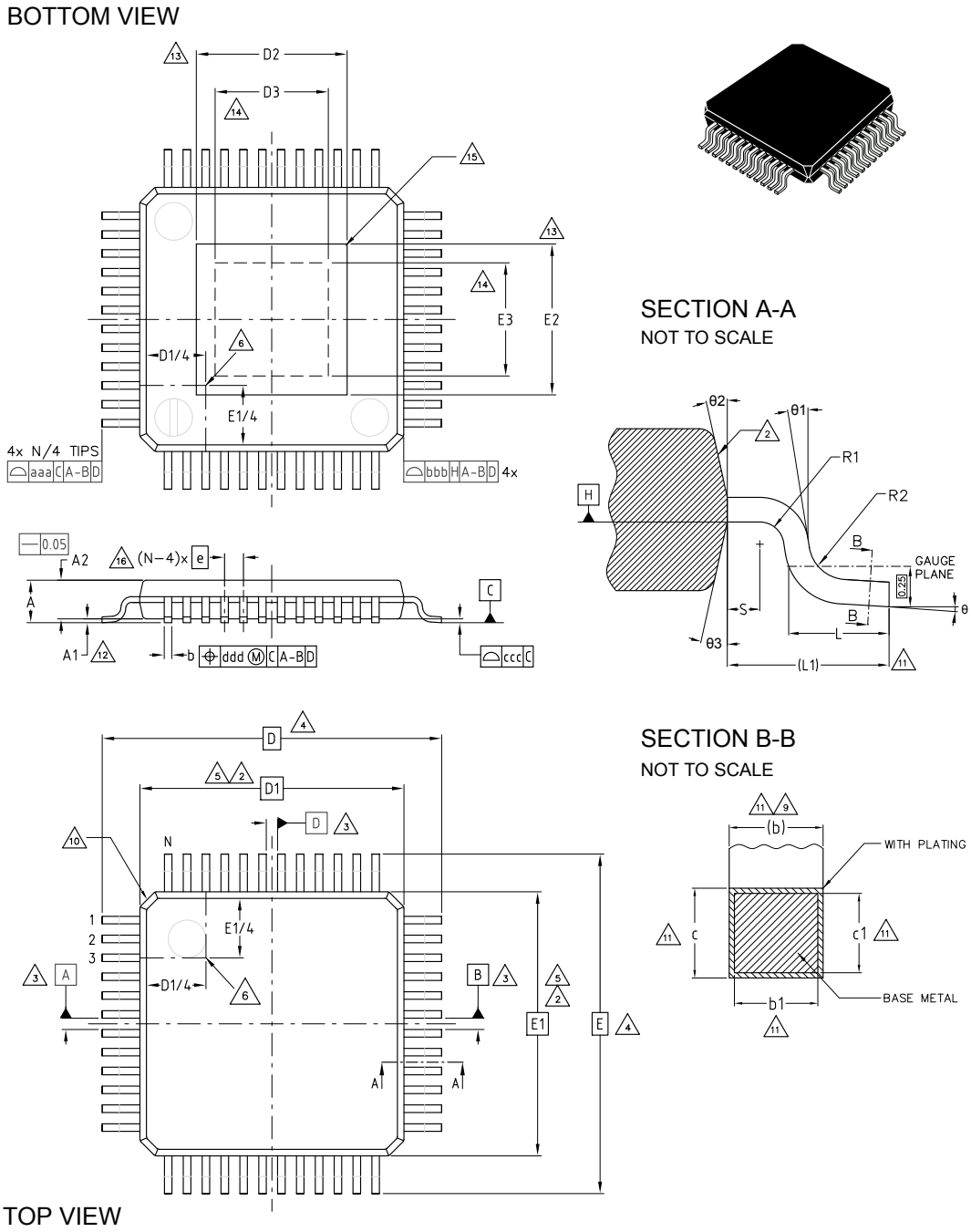


Table 39. **TQFP48 (7x7x1 mm exp. pad down 5.0x5.0) package mechanical data**

Symbol	Dimensions			Note
	Min.	Typ.	Max.	
Θ	0°	3.5°	7°	
Θ1	0°			
Θ2	11°	12°	13°	
Θ3	11°	12°	13°	
A			1.20	15
A1	0.05		0.15	12
A2	0.95	1.00	1.05	15
b	0.17	0.22	0.27	9, 11
b1	0.17	0.20	0.23	11
c	0.09		0.20	11
c1	0.09		0.16	11
D	9.00 BSC			4
D1	7.00 BSC			2, 5
D2			5.37	13
D3	3.4			14
e	0.50 BSC			
E	9.00 BSC			4
E1	7.00 BSC			2, 5
E2			5.37	13
E3	3.4			14
L	0.45	0.60	0.75	
L1	1.00 REF			
N	48			16
R1	0.08			
R2	0.08		0.20	
S	0.20			
Tolerance of form and position				
aaa	0.20			1, 7
bbb	0.20			
ccc	0.08			
ddd	0.08			

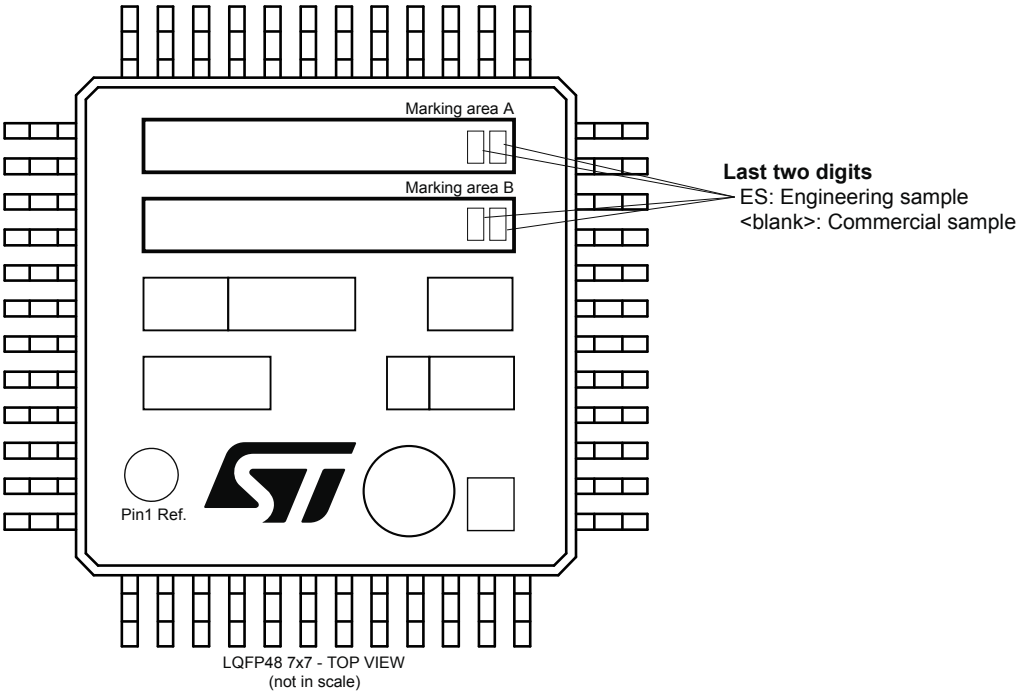
Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The top package body size may be smaller than the bottom package size up to 0.15 mm.
3. Datum A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All dimensions are in millimeters.

8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from exposed pad itself.
14. Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.
15. The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.
16. “N” is the number of terminal positions for the specified body size.

14.2 TQFP48 (7x7x1 mm exp. pad down) marking information

Figure 31. **TQFP48 (7x7x1 mm exp. pad down) marking information**



Parts marked as ‘ES’ are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

Revision history

Table 40. **Document revision history**

Date	Revision	Changes
02-Jul-2018	1	Initial release.
30-Nov-2018	2	Document partially reformatted, no content change.
04-Nov-2019	3	Added *Section Applications*. Removed "Quality information" section. Updated *Section 14.1 TQFP48 (7x7x1 mm exp. pad down 5.0x5.0) package information*. Minor text changes.
04-Dec-2019	4	Updated *Product summary* table.
08-Jul-2021	5	Added *Section 12 Applications*. Updated *Section Applications*. Minor text changes in: • *Table 33. PSI-5 satellite transceiver - DC specifications (ITHOPEN Symbol);* • *Section Features;* • *Section Description;* • *Section 4 Overview and block diagram*.
19-May-2023	6	Updated *Section 5.3 Oscillators*; *Section 5.4 Reset control*.
29-May-2024	7	Updated Figure 27. Application circuit. Minor text changes in Table 16. Bill of materials.

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