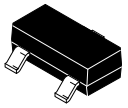
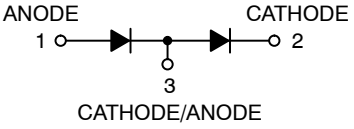
Low Capacitance Diode Array for ESD Protection in a Single Data Line

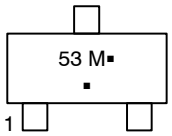
NUP1301ML3T1G is a MicroIntegration device designed to provide protection for sensitive components from possible harmful electrical transients; for example, ESD (electrostatic discharge).



SOT−23



MARKING DIAGRAM



53 = Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

Features

- Low Capacitance 0.9 pF Typ
- Single Package Integration Design
- Provides ESD Protection for JEDEC Standards JESD22
  - Machine Model = Class C
  - Human Body Model = Class 3B
- Protection for IEC61000−4−2 (Level 4)
  - 8.0 kV (Contact)
  - 15 kV (Air)
- Ensures Data Line Speed and Integrity
- Fewer Components and Less Board Space
- Direct the Transient to Either Positive Side or to the Ground
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- Pb−Free Package is Available*

Applications

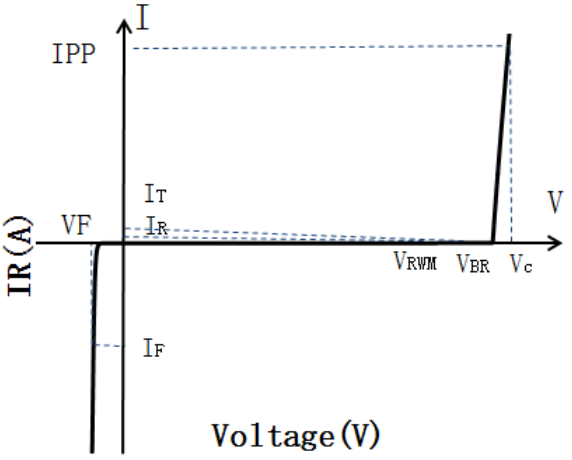
- T1/E1 Secondary IC Protection
- T3/E3 Secondary IC Protection
- HDSL, IDSL Secondary IC Protection
- Video Line Protection
- Microcontroller Input Protection
- Base Stations
- I^2C Bus Protection

Absolute Maximum Ratings (T_A=25°C unless otherwise specified)

Parameter	Symbol	Value	Unit
Peak Pulse Power (8/20μs)	Ppk	150	W
Peak Pulse Current (8/20μs)	IPP	15	A
ESD per IEC 61000−4−2 (Air) ESD per IEC 61000−4−2 (Contact)	VESD	±15 ±8	kV
Operating Temperature Range	TJ	−55 to +125	°C
Storage Temperature Range	Tstg	−55 to +150	°C

Portion Electronics Parameter

Symbol	Parameter
I_T	Test Current
I_{PP}	Maximum Reverse Peak Pulse Current
Vc	Clamping Voltage @Ic



Electrical Characteristics (T_A=25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}				100	V
Breakdown Voltage	V_{BR}	I_T = 1mA	110			V
Reverse Leakage Current	I_R	V_{RWM} =100V			0.1	μA
Clamping Voltage	Vc	I_{PP} = 1A (8 x 20μs pulse)			8	V
Clamping Voltage	Vc	I_{PP} = 15A (8 x 20μs pulse)			10	V
Junction Capacitance	C_J	VR = 0V, f = 1MHz		0.9		pF

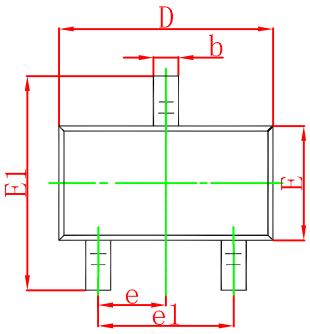
Figure 1. ESD Test Circuit

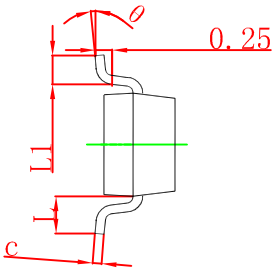
APPLICATION NOTE

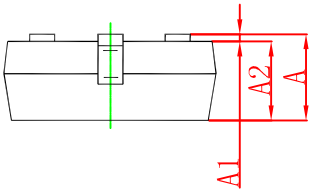
Electrostatic Discharge

A common means of protecting high−speed data lines is to employ low−capacitance diode arrays in a rail−to−rail configuration. Two devices per line are connected between two fixed voltage references such as V_{CC} and ground. When the transient voltage exceeds the forward voltage (V_F) drop of the diode plus the reference voltage, the diodes direct the surge to the supply rail or ground. This method has several advantages including low loading capacitance, fast response time, and inherent bidirectionality (within the reference voltages). See Figure 1 for the test circuit used to verify the ESD rating for this device.

SOT-23 Package Outline Dimensions

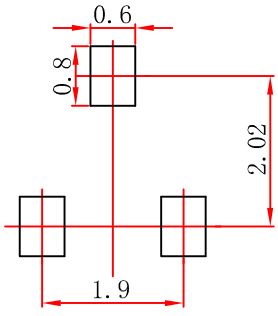






Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.550 REF		0.022 REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

SOT-23 Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.