MOSFET – N-Channel, SUPERFET® II, FRFET®

650 V, 76 A, 41 mΩ

FCH041N65EFL4

Description

SuperFET II Mosfet is ON Semiconductor's brand−new high voltage super−junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on−resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as PFC, server / telecom power, FPD TV power, ATX power and industrial power applications. SuperFET II FREFET MOSFET's optimized body diode reverse recovery performance can remove additional component and improve system reliability.

Features

- Typ. $R_{DS(on)}$ = 36 mΩ
- 700 V @ T_J = 150°C
- Ultra Low Gate Charge (Typ. Q_g = 229 nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 631 pF)
- 100% Avalanche Tested
- These Devices are Pb−Free and are RoHS Compliant

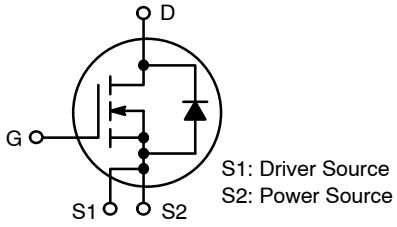
Applications

- AC−DC Power Supply
- LCD/LED/PDP TV
- Solar Inverter
- Telecom / Server Power Supplies

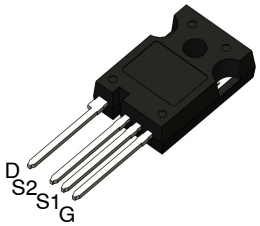
ON Semiconductor®

www.onsemi.com

V_{DS}	$R_{DS(ON)}$ MAX	I_D MAX
650 V	41 mΩ @ 10 V	76 A

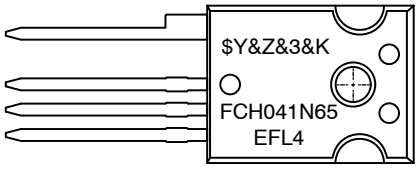


N-CHANNEL MOSFET



TO−247−4LD
CASE 340CJ

MARKING DIAGRAM



FCH041N65EFL4	= Specific Device Code
$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Data Code (Week & Year)
K	= Lot

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		650	V
V_{GSS}	Gate to Source Voltage	– DC	±20	V
		– AC (f > 1 Hz)	±30	
I_D	Drain Current:	– Continuous (T_C = 25°C)	76	A
		– Continuous (T_C = 100°C)	48.1	
I_{DM}	Drain Current:	– Pulsed (Note 1)	228	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		2025	mJ
I_{AS}	Avalanche Current (Note 2)		15	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		5.95	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		50	
P_D	Power Dissipation	(T_C = 25°C)	595	W
		– Derate Above 25°C	4.76	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		–55 to + 150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8″ from Case for 5 seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse−width limited by maximum junction temperature.
2. I_{AS} = 15 A, R_G = 25 Ω, starting T_J = 25 °C.
3. I_{SD} ≤ 38 A, di/dt ≤ 200 A/μs, V_{DD} ≤ 380 V, starting T_J = 25 °C.

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Reel Size	Tape Width	Quantity
FCH041N65EFL4	FCH041N65EF	TO−247 4L	Tube	N/A	N/A	30 Units

THERMAL CHARACTERISTICS

Symbol	Parameter	FCH041N65EFL4	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.21	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 10 mA, T_J = 25°C	650	–	–	V
		V_{GS} = 0 V, I_D = 10 mA, T_J = 150°C	700	–	–	
ΔBV_{DSS} /ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 10 mA, Referenced to 25°C	–	0.72	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V	–	–	10	μA
		V_{DS} = 520 V, T_C = 125 °C	–	145	–	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 7.6 mA	3	–	5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 38 A	–	36	4	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 38 A	–	71.7	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 100 V, V_{GS} = 0 V, f = 1 MHz	–	9446	12560	pF
C_{oss}	Output Capacitance		–	366	490	pF
C_{rss}	Reverse Transfer Capacitance		–	35	–	pF
C_{oss}	Output Capacitance	V_{DS} = 380 V, V_{GS} = 0 V, f = 1 MHz	–	197	–	pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	–	631	–	pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	V_{DS} = 380 V, I_D = 38 A, V_{GS} = 10 V (Note 4)	–	229	298	nC
Q_{gs}	Gate to Source Gate Charge		–	50	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	90	–	nC
ESR	Equivalent Series Resistance	f = 1 MHz	–	0.6	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 380 V, I_D = 38 A, V_{GS} = 10 V, R_g = 4.7 Ω (Note 4)	–	55	120	ns
t_r	Turn−On Rise Time		–	25	60	ns
$t_{d(off)}$	Turn-Off Delay Time		–	169	348	ns
t_f	Turn−Off Fall Time		–	18	46	ns
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuous Source to Drain Diode Forward Current		–	–	76	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	228	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 38 A	–	–	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 38 A, di_F/dt = 100 A/μs	–	207	–	ns
Q_{rr}	Reverse Recovery Charge		–	1.5	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL CHARACTERISTICS

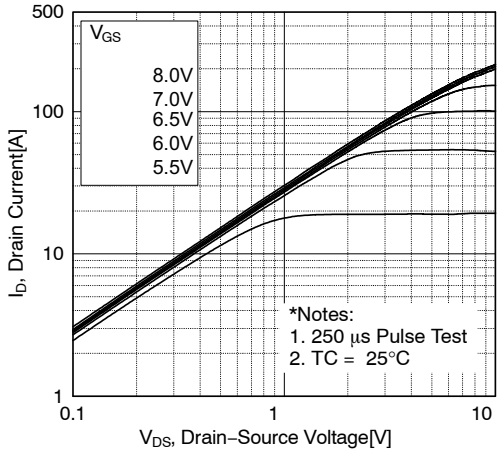


Figure 1. On−Region Characteristics

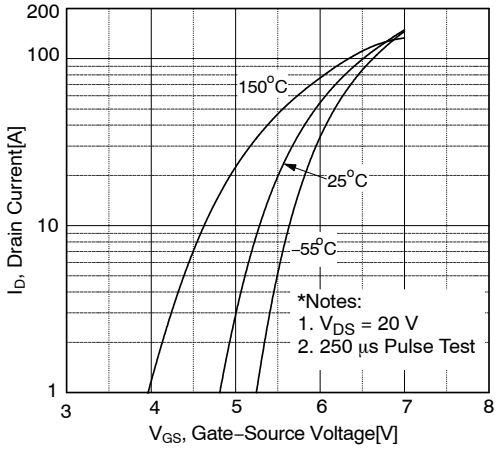


Figure 2. Transfer Characteristics

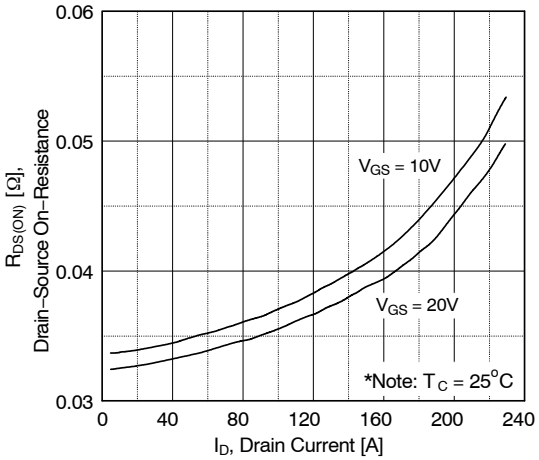


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

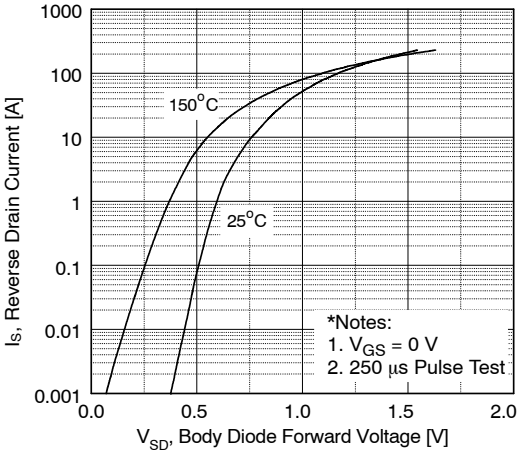


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

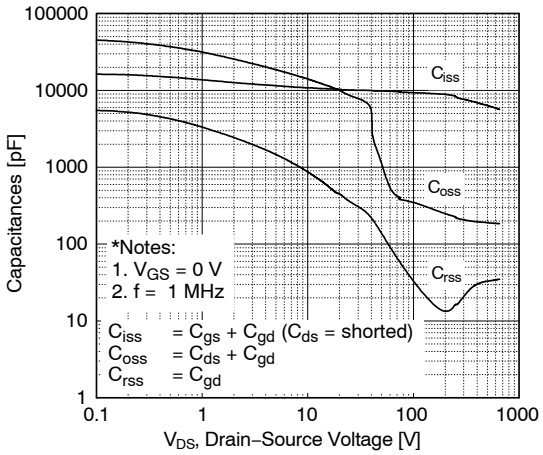


Figure 5. Capacitance Characteristics

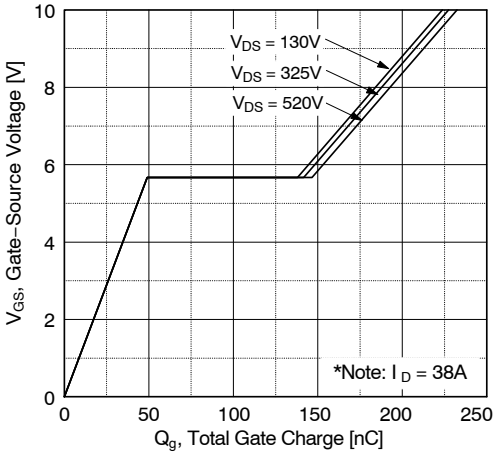


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS

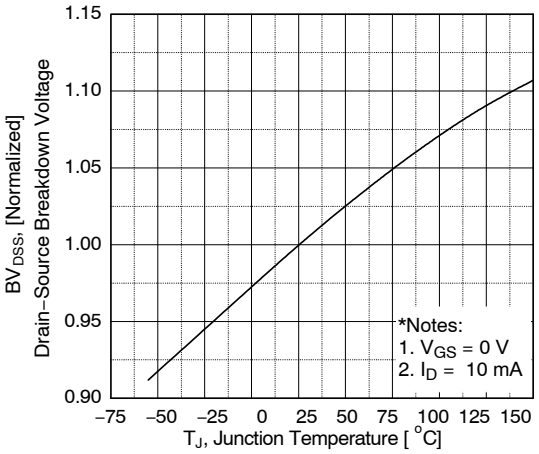


Figure 7. Breakdown Voltage Variation vs. Temperature

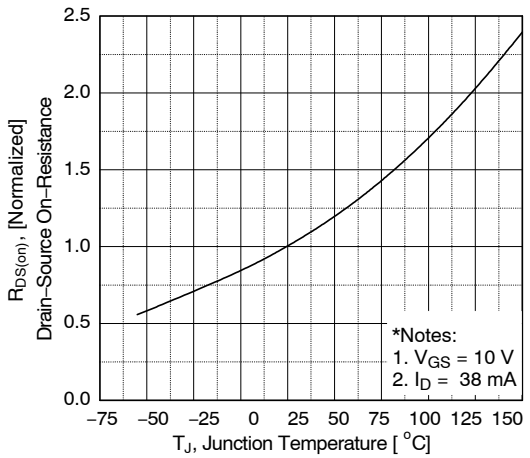


Figure 8. On−Resistance Variation vs. Temperature

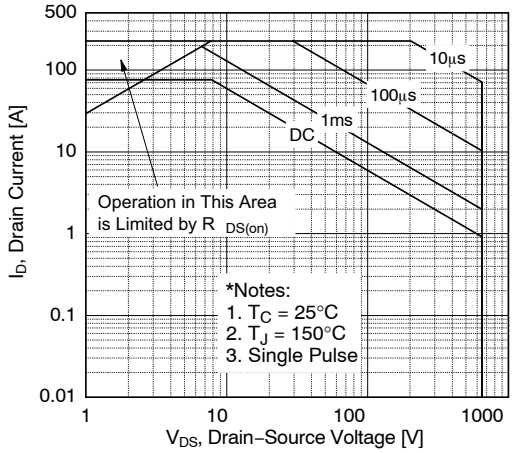


Figure 9. Maximum Safe Operating Area

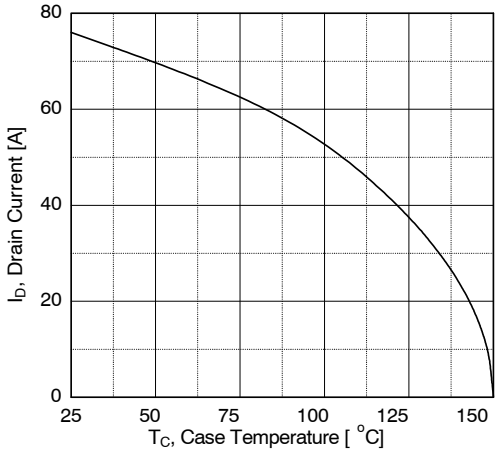


Figure 10. Maximum Drain Current vs. Case Temperature

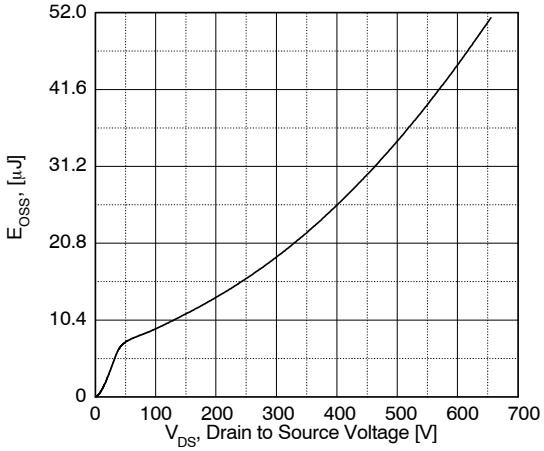


Figure 11. Eoss vs. Drain to Source Voltage

TYPICAL CHARACTERISTICS

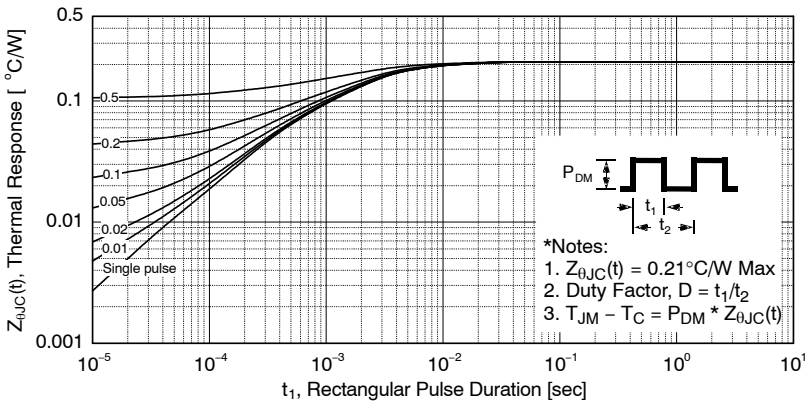


Figure 12. Transient Thermal Response Curve

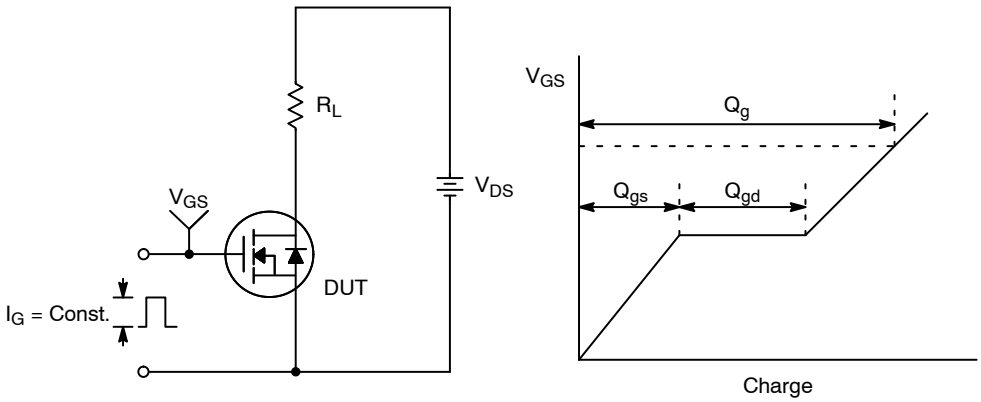


Figure 13. Gate Charge Test Circuit & Waveform

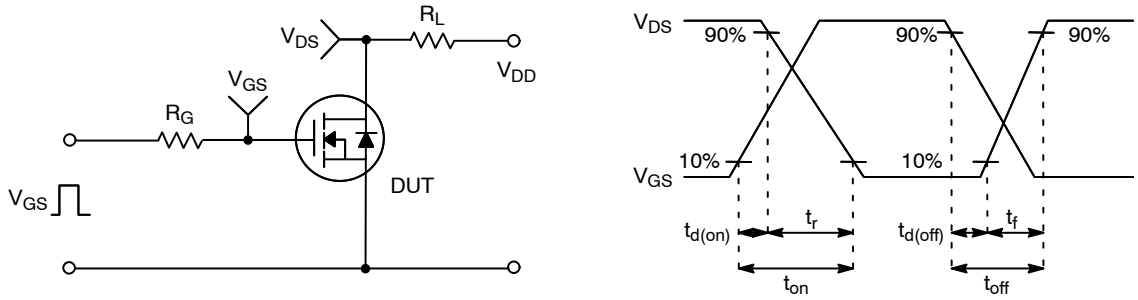


Figure 14. Resistive Switching Test Circuit & Waveforms

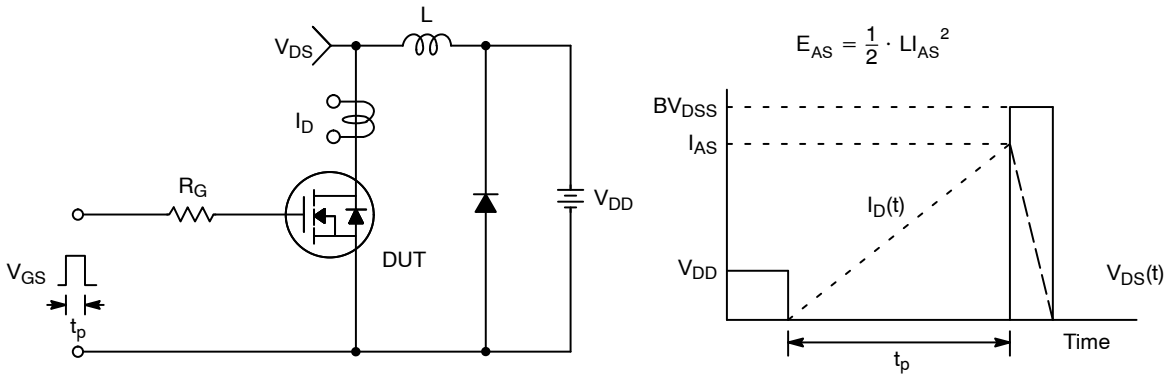


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

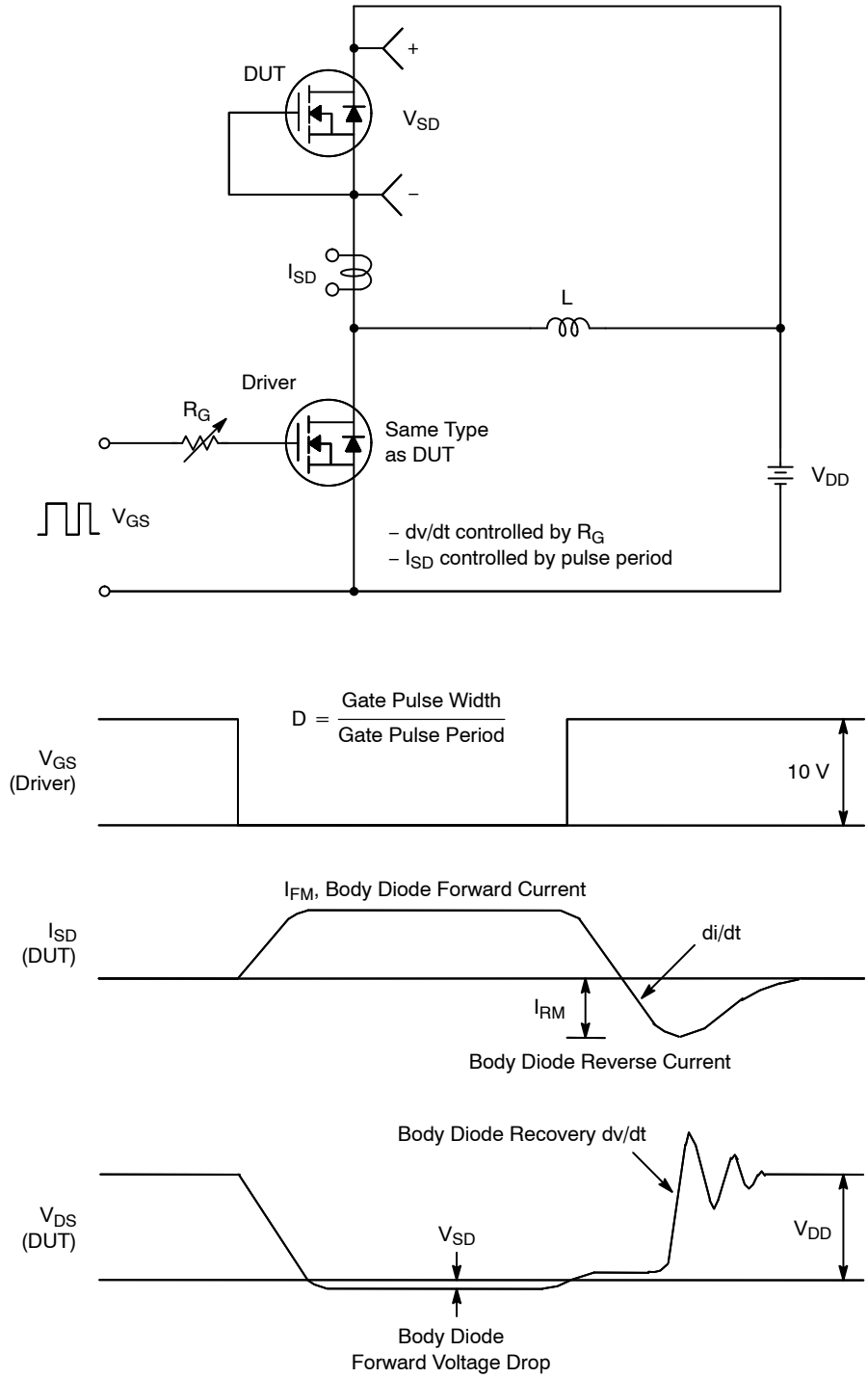


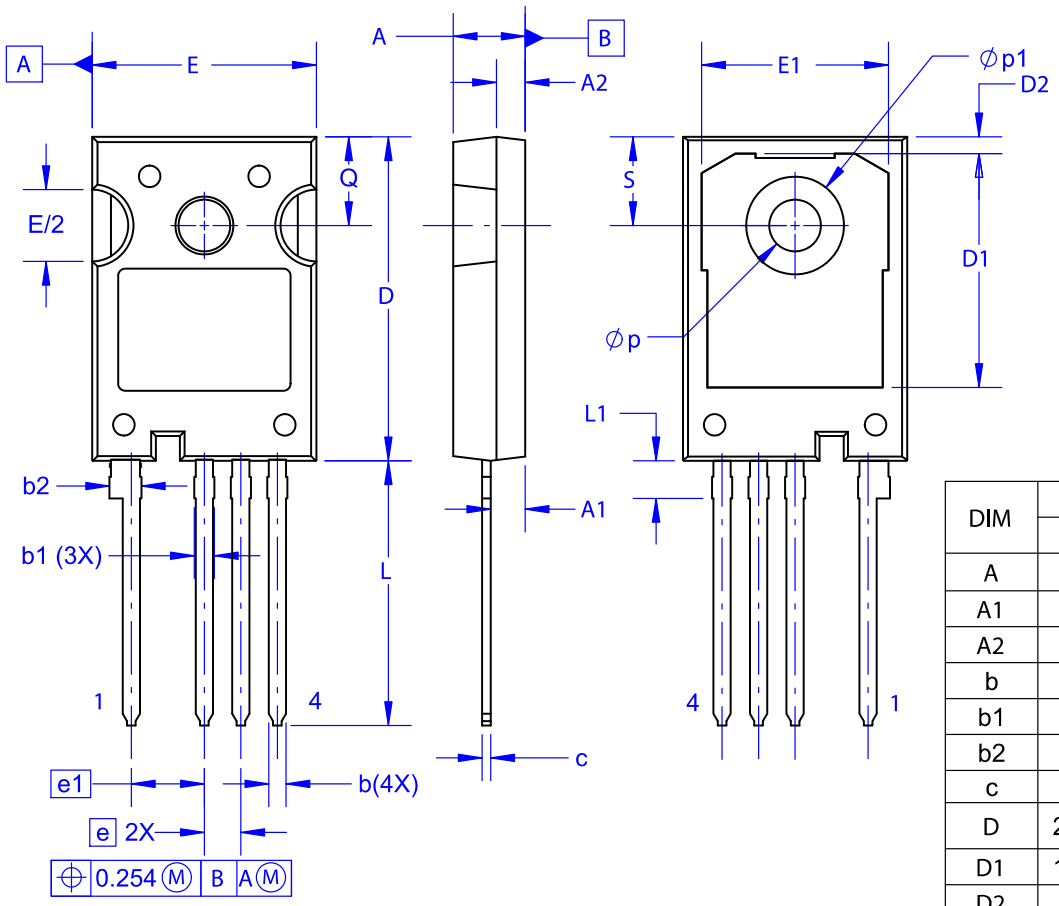
Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

TO−247−4LD
CASE 340CJ
ISSUE A

DATE 16 SEP 2019



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.80	5.00	5.20
A1	2.10	2.40	2.70
A2	1.80	2.00	2.20
b	1.07	1.20	1.33
b1	1.20	1.40	1.60
b2	2.02	2.22	2.42
c	0.50	0.60	0.70
D	22.34	22.54	22.74
D1	16.00	16.25	16.50
D2	0.97	1.17	1.37
e	2.54 BSC		
e1	5.08 BSC		
E	15.40	15.60	15.80
E1	12.80	13.00	13.20
E/2	4.80	5.00	5.20
L	18.22	18.42	18.62
L1	2.42	2.62	2.82
p	3.40	3.60	3.80
p1	6.60	6.80	7.00
Q	5.97	6.17	6.37
S	5.97	6.17	6.37

NOTES:

A. NO INDUSTRY STANDARD APPLIES TO THIS PACKAGE.
B. DIMENSIONS ARE EXCLUSIVE OF BURRS,MOLD FLASH,AND TIE BAR EXTRUSIONS.
C. ALL DIMENSIONS ARE IN MILLIMETERS.
D. DRAWING CONFORMS TO ASME Y14.5-2009.

DOCUMENT NUMBER:	**98AON13852G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**TO−247−4LD**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales