LEOPARD IMAGING INC

LI-M021C-MIPI Data Sheet

Key Features

- Aptina 1/3" CMOS Digital Image Sensor MT9M021
- Optical format: 1/3"
- Active pixels: 1280H x 960V
- Pixel size: 3.75 um x 3.75 um
- Global shutter
- Color filter array: RGB Bayer
- Responsivity: 5.3V/lux-sec
- Support M8 lens
- Module Size: 18.5mm x 15mm
- Weight: 2 g
- Part#: LI-M021C-MIPI

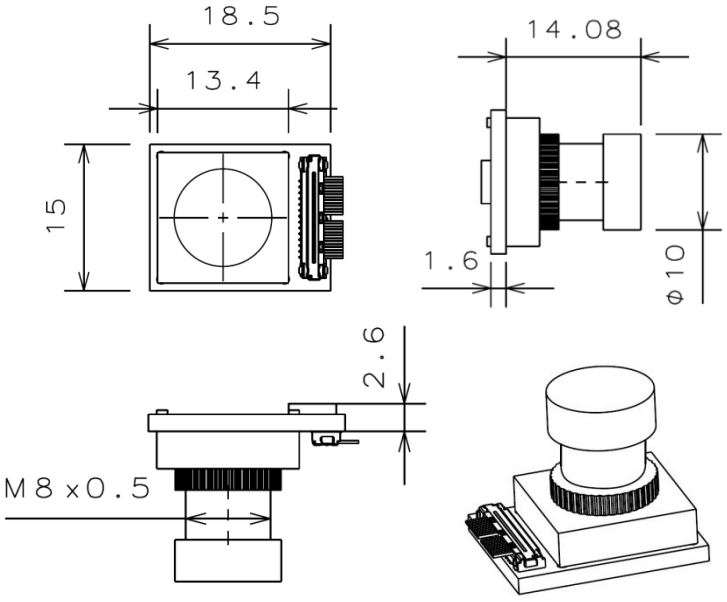
Interface

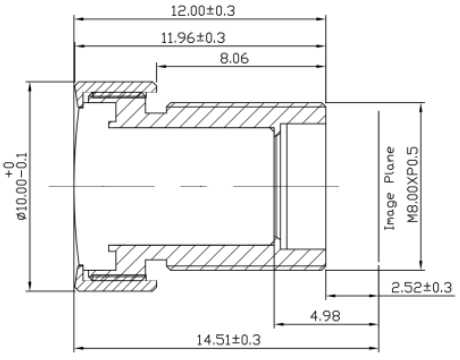
- Part#: 20498-026E-41
- Number of Positions: 26
- Shell Plating: Sn
- Vaccum Clip: With

Lens Spec

- Part#: HK-8110-131-1-M8
- Sensor size: 1/3"
- Focal Length: 3 mm
- Aperture, F/#: 2.8
- Built in 650 nm IR cut filter
- FOV (D/H/V): 117 °90 °67 °
- Mount: M8 x P0.5 – 6g

Dimensions





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1130 Cadillac Ct., Milpitas, CA 95035,USA
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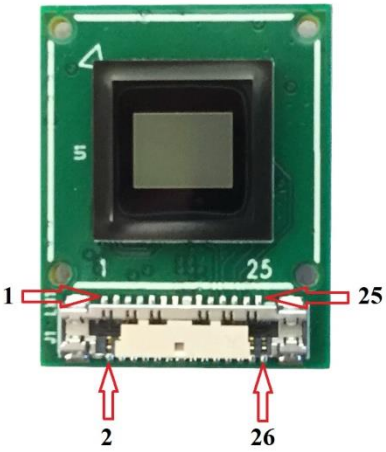
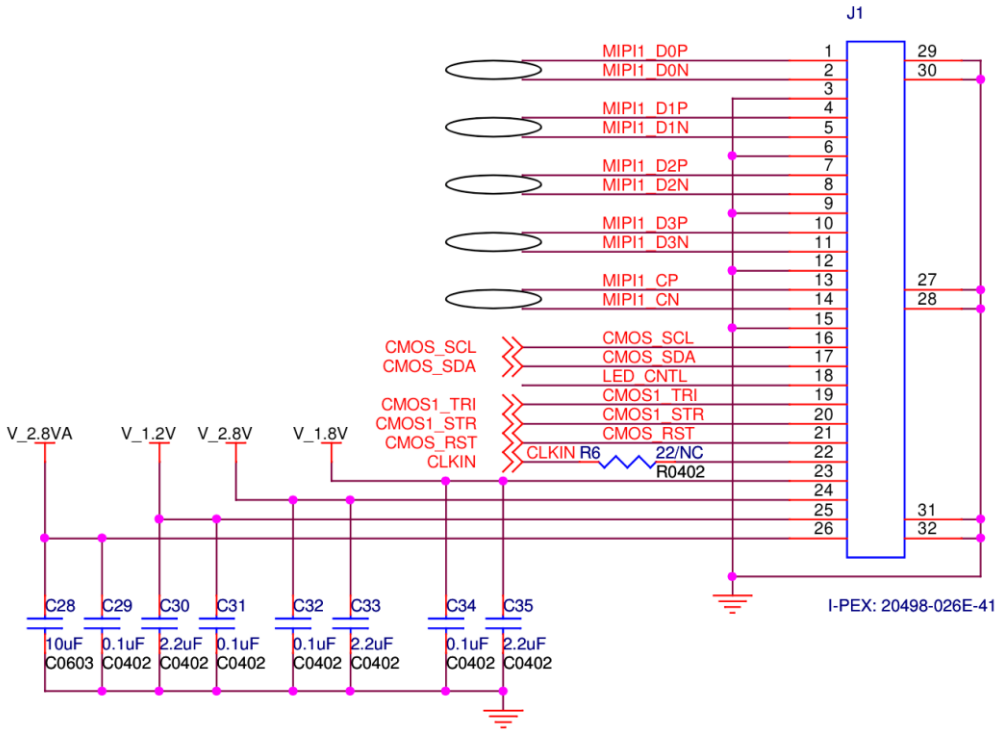
Pin Assignment





Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
V_{SUPPLY}	Power supply voltage (all supplies)	-0.3	4.5	V
I_{SUPPLY}	Total power supply current	-	200	mA
I_{GND}	Total ground current	-	200	mA
V_{IN}	DC input voltage	-0.3	V_{DD} IO + 0.3	V
V_{OUT}	DC output voltage	-0.3	V_{DD} IO + 0.3	V
T_{STG} [1]	Storage temperature	-40	+85	°C

Note: 1. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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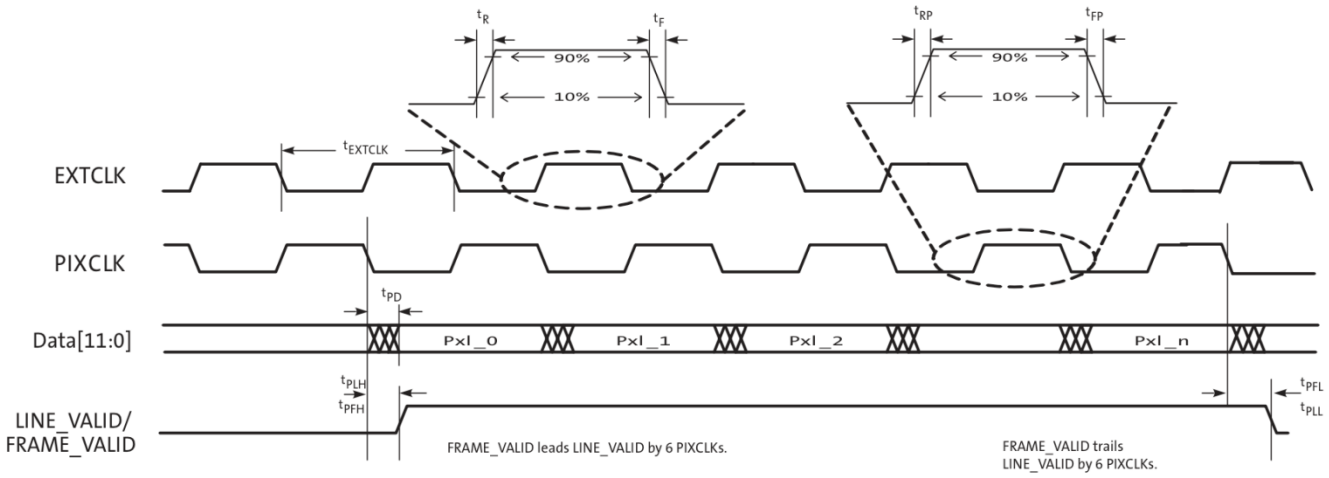
DC Electrical Characteristics

Symbol	Definition	Condition	Min	Typ	Max	Unit
V_{DD}	Core digital voltage		1.7	1.8	1.95	V
V_{DD}_IO	I/O digital voltage		1.7/2.5	1.8/2.8	1.9/3.1	V
V_{AA}	Analog voltage		2.5	2.8	3.1	V
V_{AA}_PIX	Pixel supply voltage		2.5	2.8	3.1	V
V_{DD}_PLL	PLL supply voltage		2.5	2.8	3.1	V
V_{DD}_SLVS	HiSPi supply voltage		0.3	0.4	0.6	V
V_{IH}	Input HIGH voltage		V_{DD}_IO * 0.7	-	-	V
V_{IL}	Input LOW voltage		-	-	V_{DD}_IO * 0.3	V
I_{IN}	Input leakage current	No pull-up resistor; V_{IN} = V_{DD}_IO or D_{GND}	20	-	-	uA
V_{OH}	Output HIGH voltage		V_{DD}_IO – 0.3	-	-	V
V_{OL}	Output LOW voltage	V_{DD}_IO = 2.8V	-	-	0.4	V
I_{OH}	Output HIGH current	At specified V_{OH}	-22	-	-	mA
I_{OL}	Output LOW current	At specified V_{OL}	-	-	22	mA

I/O Timing Diagram



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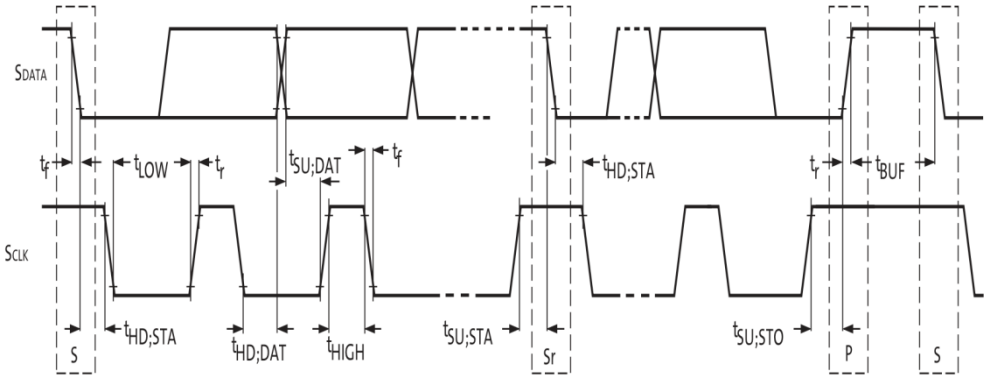
I/O Timing Characteristics

Parallel Output									
Symbol	Definition	Condition	VDD_IO=2.8V			VDD_IO=1.8V			Unit
			Min	Typ	Max	Min	Typ	Max	
f_{EXTCLK}	Input clock frequency		6		50	6		50	MHz
t_{EXTCLK}	Input clock period		20		166	20		166	ns
t_R	Input clock rise time	PLL enabled		3	4		3	4	ns
t_F	Input clock fall time	PLL enabled		3	4		3	4	ns
t_{RP}	PIXCLK rise time	Slew setting = 4 (default)	2.3		4.6	2.3		4.6	ns
t_{FP}	PIXCLK fall time	Slew setting = 4 (default)	3		4.4	3		4.4	ns
	PIXCLK duty cycle		40	50	60	40	50	60	%
f_{PIXCLK}	PIXCLK frequency	Nominal voltages, PLL Enabled	6		74.25	6		74.25	MHz
t_{PD}	PIXCLK to data valid	Nominal voltages, PLL Enabled	-3	2.3	4	-3	2.3	4.5	ns
t_{PFH}	PIXCLK to FV HIGH	Nominal voltages, PLL Enabled	-3	1.5	4	-3	1.5	4.5	ns
t_{PLH}	PIXCLK to LV HIGH	Nominal voltages, PLL Enabled	-3	2.3	4	-3	2.3	4.5	ns
t_{PFL}	PIXCLK to FV LOW	Nominal voltages, PLL Enabled	-3	1.5	4	-3	1.5	4.5	ns
t_{PLL}	PIXCLK to LV LOW	Nominal voltages, PLL Enabled	-3	2	4	-3	2	4.5	ns

Two-Wire Serial Bus Timing Parameters



Note: Read sequence: For an 8-bit READ, read waveforms start after WRITE command and register address are issued.

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Two-Wire Serial Bus Characteristics

[f]EXTCLK = 27 MHz; VDD = 1.8V; VDD_IO = 2.8V; VAA = 2.8V; VAA_PIX = 2.8V; VDD_PLL = 2.8V; TA = 25℃

Parameter	Symbol	Standard-Mode		Fast-Mode		Unit
		Min	Max	Min	Max	
S_{CLK} Clock Frequency	[f]SCL	0	100	0	400	KHz
Hold time (repeated) START condition						
After this period, the first clock pulse is generated	[t]HD;STA	4.0	-	0.6	-	us
LOW period of the SCLK clock	[t]LOW	4.7	-	1.3	-	us
HIGH period of the SCLK clock	[t]HIGH	4.0	-	0.6	-	us
Set-up time for a repeated START condition	[t]SU;STA	4.7	-	0.6	-	us
Data hold time	[t]HD;DAT	0[4]	3.45[5]	0[6]	0.9[5]	us
Data set-up time	[t]SU;DAT	250	-	100[6]	-	ns
Rise time of both S_{DATA} and S_{CLK} signals	[t]r	-	1000	20 + 0.1Cb7	300	ns
Fall time of both S_{DATA} and S_{CLK} signals	[t]f	-	300	20 + 0.1Cb7	300	ns
Set-up time for STOP condition	[t]SU;STO	4.0	-	0.6	-	us
Bus free time between a STOP and START condition	[t]BUF	4.7	-	1.3	-	us
Capacitive load for each bus line	Cb	-	400	-	400	pF
Serial interface input pin capacitance	CIN_SI	-	3.3	-	3.3	pF
S_{DATA} max load capacitance	CLOAD_SD	-	30	-	30	pF
S_{DATA} pull-up resistor	RSD	1.5	4.7	1.5	4.7	KΩ

Note: 1. This table is based on I^2C standard (v2.1 January 2000). Philips Semiconductor.

2. Two-wire control is I^2C-compatible.
3. All values referred to V_{IHmin} = 0.9 VDD and V_{ILmax} = 0.1 VDD levels. Sensor EXCLK = 27MHz.
4. A device must internally provide a hold time of at least 300 ns for the SDATA signal to bridge the unde-fined region of the falling edge of SCLK.
5. The maximum [t]HD;DAT has only to be met if the device does not stretch the LOW period ([t]LOW) of the SCLK signal.
6. A Fast-mode I^2C-bus device can be used in a Standard-modeI^2C-bus system, but the requirement [t]SU;DAT 250ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCLK signal. If such a device does stretch the LOW period of the SCLK signal, it must out- put the next data bit to the SDATA line [t]r max + [t]SU;DAT = 1000 + 250 = 1250 ns (according to the Stan- dard-mode I^2C-bus specification) before the SCLK line is released.
7. Cb = total capacitance of one bus line in pF.

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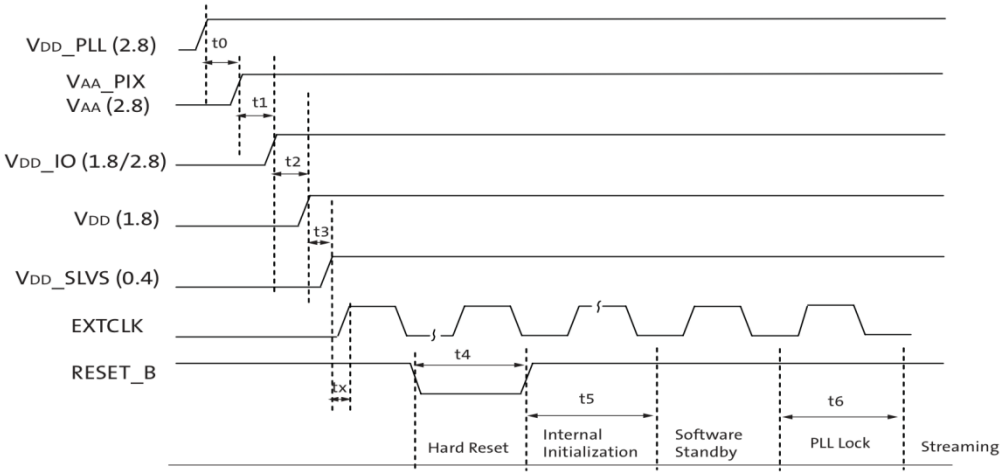
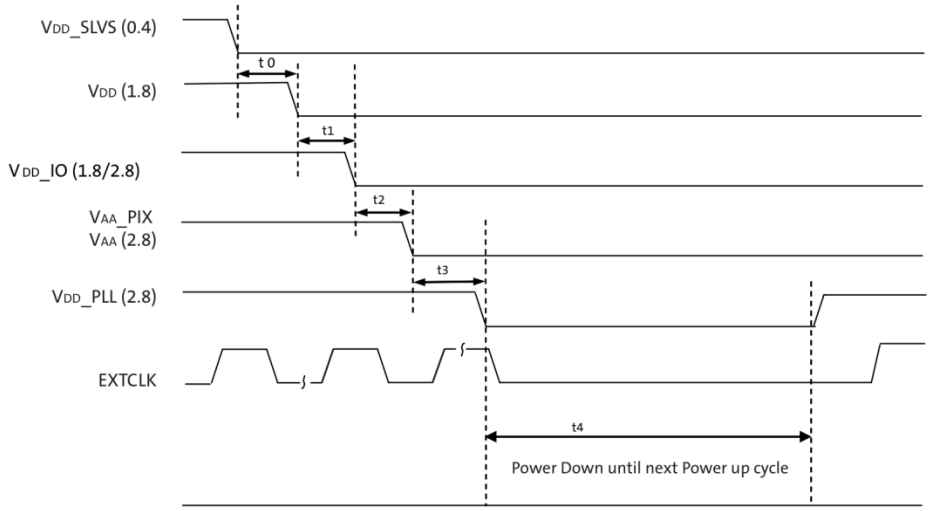
Power-Up Sequence



Definition	Symbol	Minimum	Typical	Maximum	Unit
V_{DD}_PLL to V_{AA}/V_{AA}_PIX	t0	0	10	-	us
V_{AA}/V_{AA}_PIX to V_{DD}_IO	t1	0	10	-	us
V_{DD}_IO to V_{DD}	t2	0	10	-	us
V_{DD} to V_{DD}_SLVS	t3	0	10	-	us
Xtal settle time	tx	-	30[1]	-	ms
Hard Reset	t4	1[2]	-	-	ms
Internal Initialization	t5	150000	-	-	EXTCLKs
PLL Lock Time	t6	1	-	-	ms

Note: 1. Xtal settling time is component-dependent, usually taking about 10 – 100 ms.
2. Hard reset time is the minimum time required after power rails are settled. In a circuit where Hard reset is held down by RC circuit, then the RC time must include the all power rail settle time and Xtal settle time.

Power-Down Sequence



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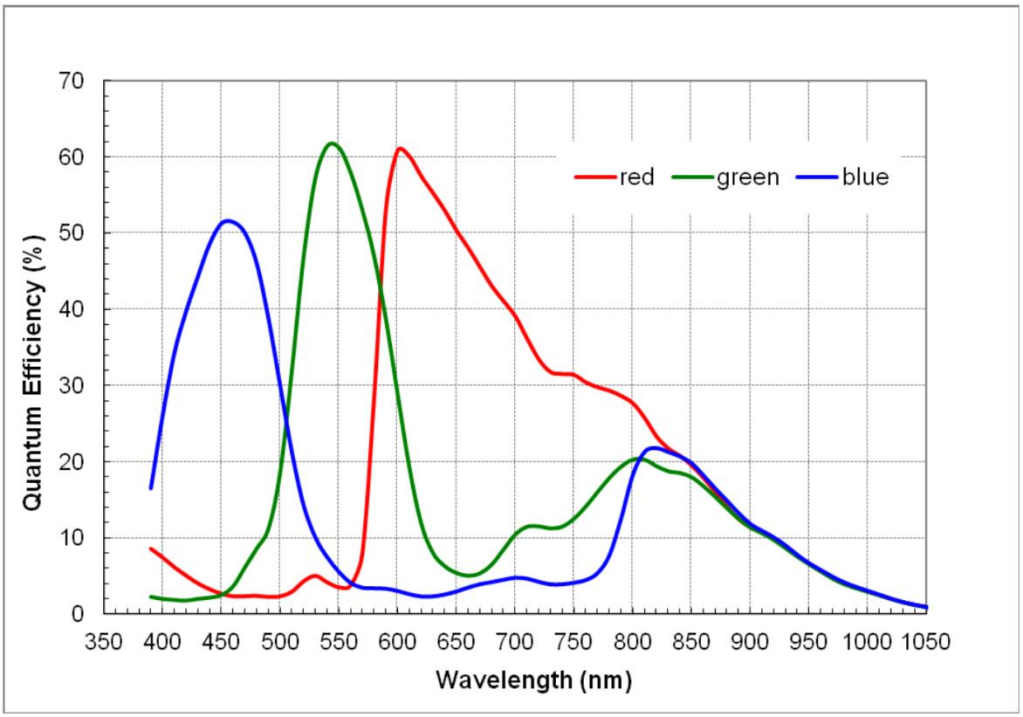
Definition	Symbol	Minimum	Typical	Maximum	Unit
V_{DD}_SLVS to V_{DD}	t0	0	-	-	us
V_{DD} to V_{DD}_IO	t1	0	-	-	us
V_{DD}_IO to V_{AA}/V_{AA}_PIX	t2	0	-	-	us
V_{AA}/V_{AA}_PIX to V_{DD}_PLL	t3	0	-	-	us
PwrDn until Next PwrUp Time	t4	100	-	-	ms

Note: t4 is required between power down and next power up time; all decoupling caps from regulators must be completely discharged.

Quantum Efficiency – Color Sensor



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