

20V Dual N-Channel Enhancement Mode MOSFET

Description

The NP9926A uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

- ◆ $V_{DS} = 20V$, $I_D = 6.5A$
 $R_{DS(ON)}(Typ.) = 19m\Omega$ @ $V_{GS} = 2.5V$
 $R_{DS(ON)}(Typ.) = 14m\Omega$ @ $V_{GS} = 4.5V$
- ◆ High density cell design for ultra low R_{dson}
- ◆ Fully characterized avalanche voltage and current

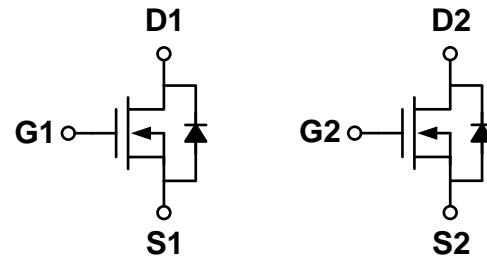
Application

- ◆ Power switching application
- ◆ Hard switched and high frequency circuits
- ◆ Uninterruptible power supply

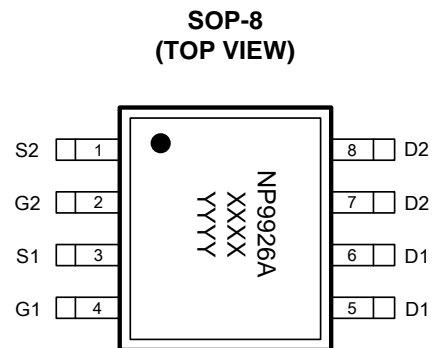
Package

- ◆ SOP-8

Schematic diagram



Marking and pin assignment



Note: XXXX is the date code, YYYY is the wafer lot number.

Ordering Information

Part Number	Storage Temperature	Package	Devices Per Reel
NP9926ASR	-55°C to +150°C	SOP-8	3000

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

parameter	symbol	limit	unit	
Drain-source voltage	V_{DS}	20	V	
Gate-source voltage	V_{GS}	±12	V	
Drain Current-Continuous (Silicon Limited)	I_D	$T_A = 25^\circ C$	6.5	A
		$T_A = 75^\circ C$	4	
Pulsed Drain Current (Package Limited)	I_{DM}	26	A	
Maximum power dissipation	P_D	$T_A = 25^\circ C$	1.25	W
		$T_A = 75^\circ C$	0.8	
Operating junction Temperature range	T_j	-55—150	°C	

Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF Characteristics						
Drain-source breakdown voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	20	-	-	V
Zero gate voltage drain current	I_{DSS}	$V_{DS}=20V, V_{GS}=0V$	-	-	1	μA
Gate-body leakage	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 12V$	-	-	± 100	nA
ON Characteristics						
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	-0.5	0.7	1.2	V
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=6.5A$	-	14	22	m Ω
		$V_{GS}=2.5V, I_D=5.5A$	-	19	27	
Forward transconductance	g_{fs}	$V_{GS}=5V, I_D=6A$	-	10	-	S
Dynamic Characteristics						
Input capacitance	C_{ISS}	$V_{DS}=10V, V_{GS}=0V$ $f=1.0MHz$	-	900	-	pF
Output capacitance	C_{OSS}		-	220	-	
Reverse transfer capacitance	C_{RSS}		-	100	-	
Switching Characteristics						
Turn-on delay time	$t_{D(ON)}$	$V_{DD}=10V$ $I_D=6A$ $V_{GEN}=4.5V$ $R_{GEN}=6\Omega$	-	10	-	ns
Rise time	t_r		-	11	-	
Turn-off delay time	$t_{D(OFF)}$		-	35	-	
Fall time	t_f		-	30	-	
Total gate charge	Q_g	$V_{DS}=10V, I_D=6A$ $V_{GS}=4.5V$	-	12	-	nC
Gate-source charge	Q_{gs}		-	2.3	-	
Gate-drain charge	Q_{gd}		-	1	-	

Thermal Characteristics

Thermal Resistance junction-to ambient	$R_{th JA}$	100	$^{\circ}C/W$
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Typical Performance Characteristics

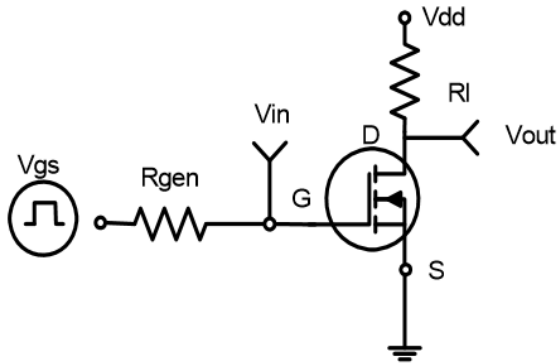


Figure 1: Switching Test Circuit

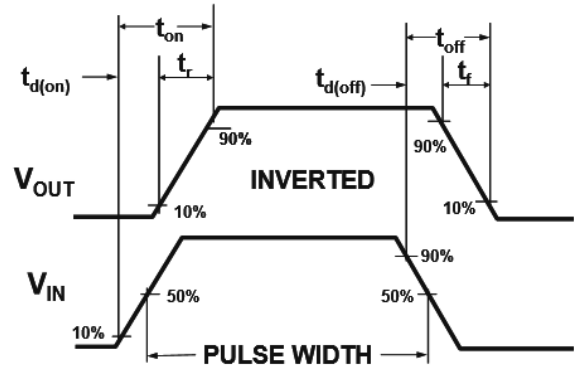


Figure 2: Switching Waveforms

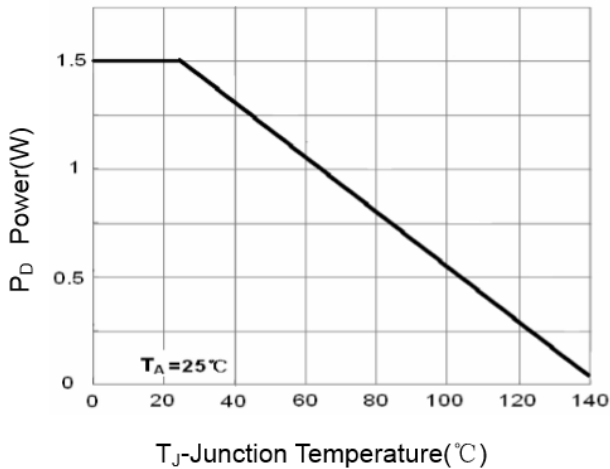


Figure 3 Power Dissipation

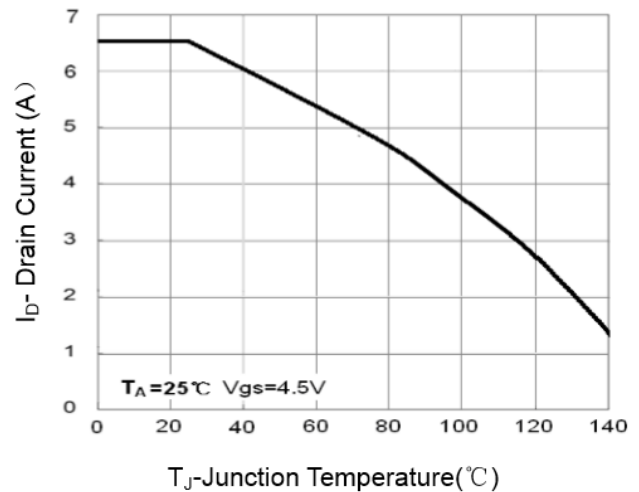


Figure 4 Drain Current

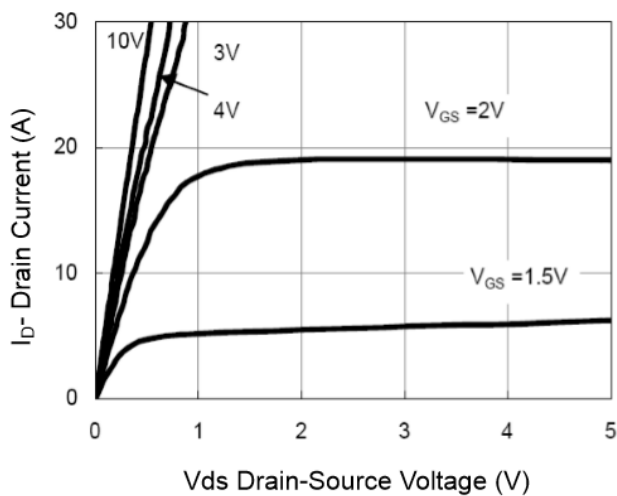


Figure 5 Output Characteristics

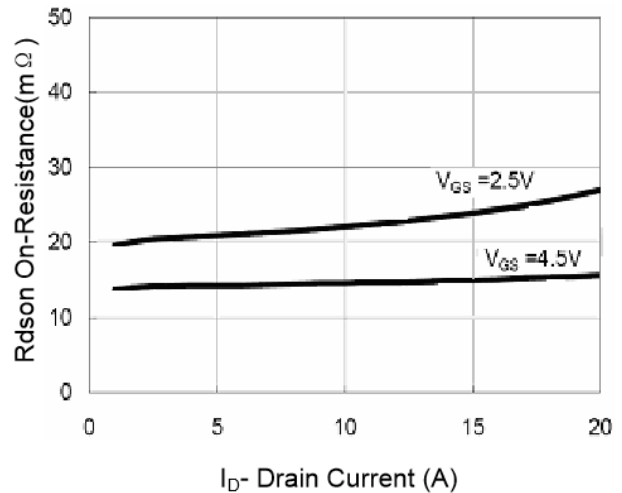


Figure 6 Drain-Source On-Resistance

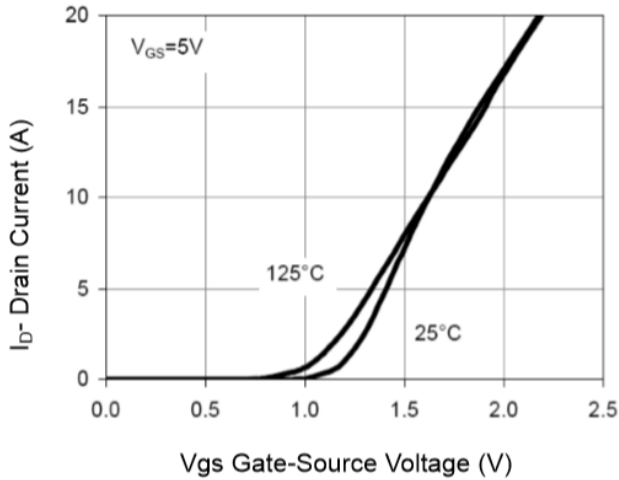


Figure 7 Transfer Characteristics

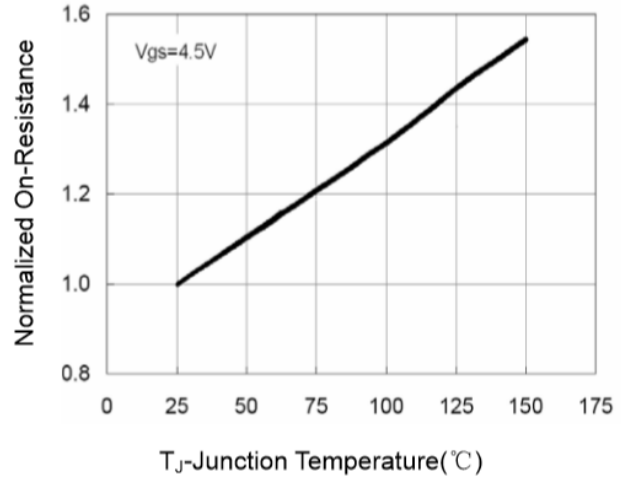


Figure 8 Drain-Source On-Resistance

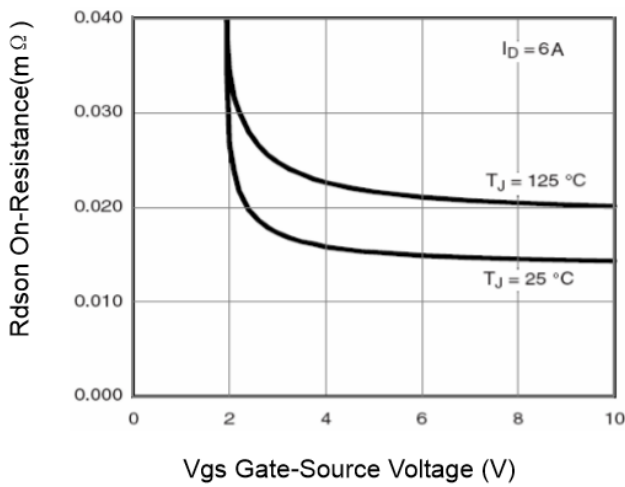


Figure 9 Rdson vs Vgs

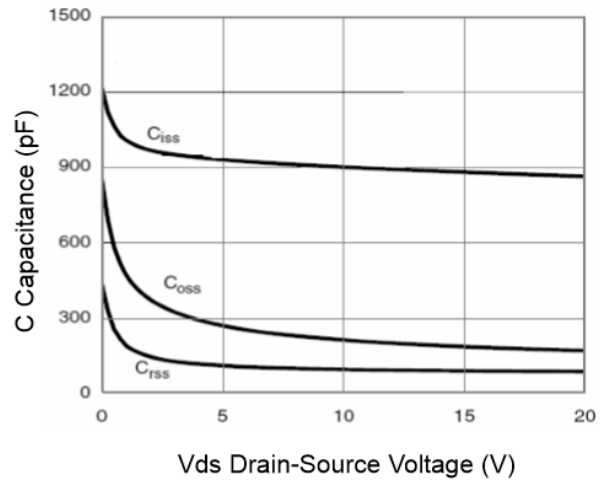


Figure 10 Capacitance vs Vds

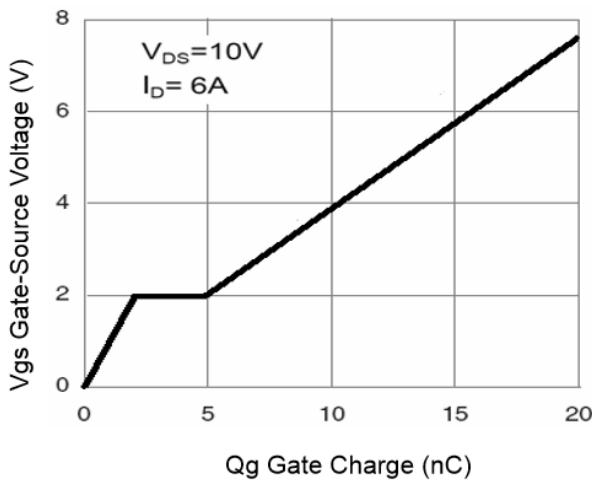


Figure 11 Gate Charge

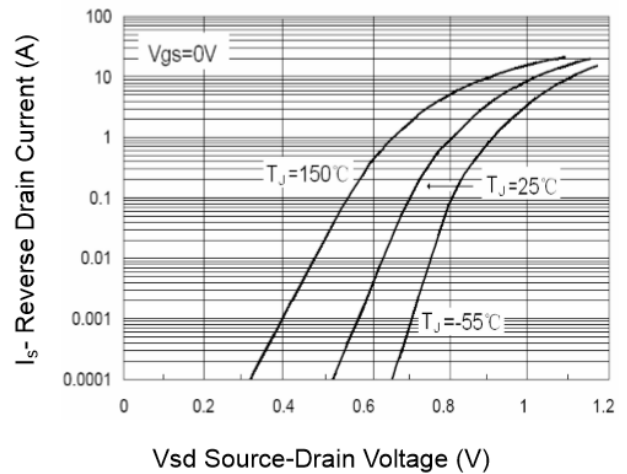


Figure 12 Source- Drain Diode Forward

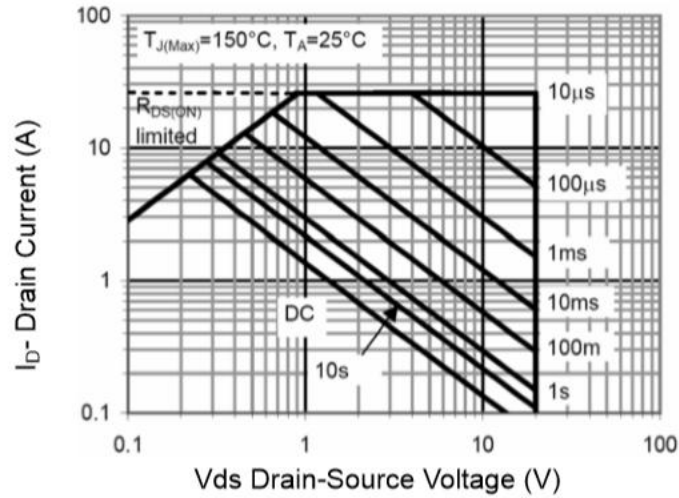


Figure 13 Safe Operation Area

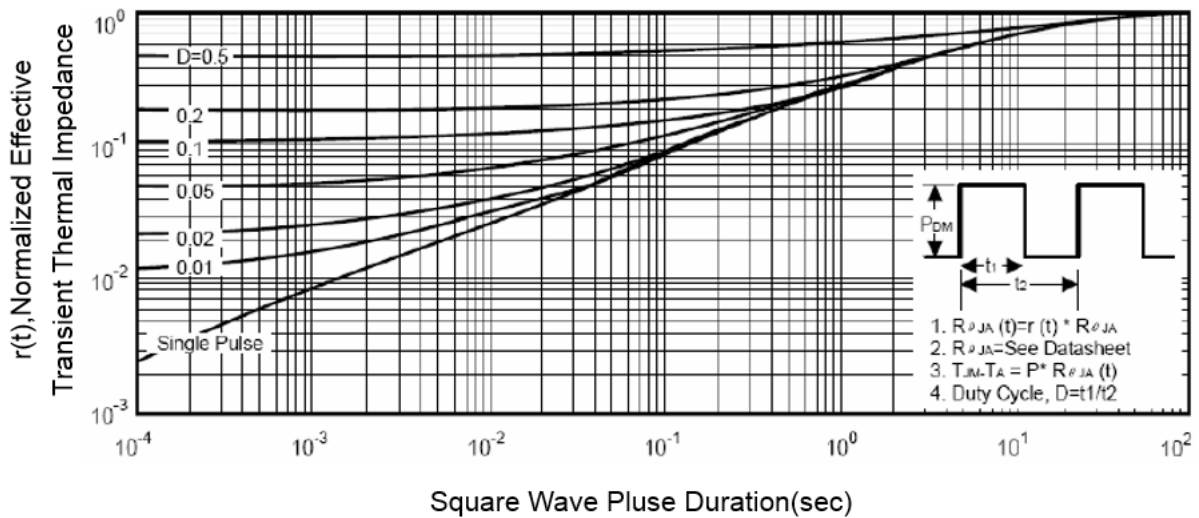
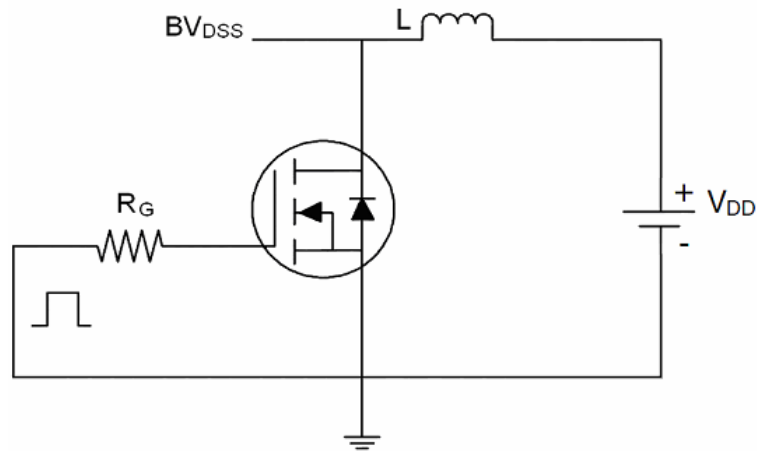


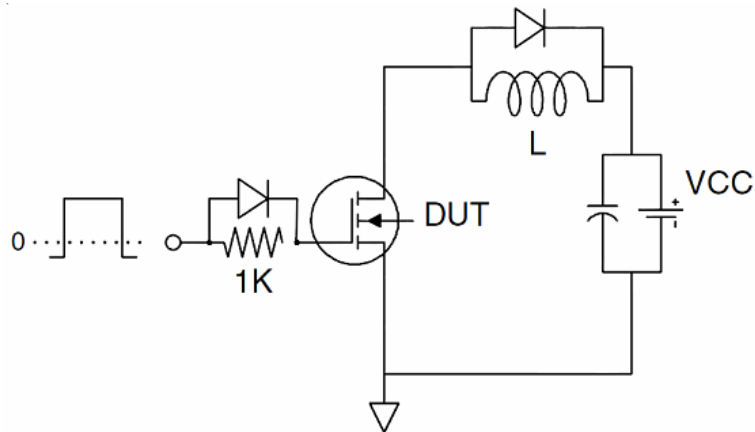
Figure 14 Normalized Maximum Transient Thermal Impedance

Test Circuit:

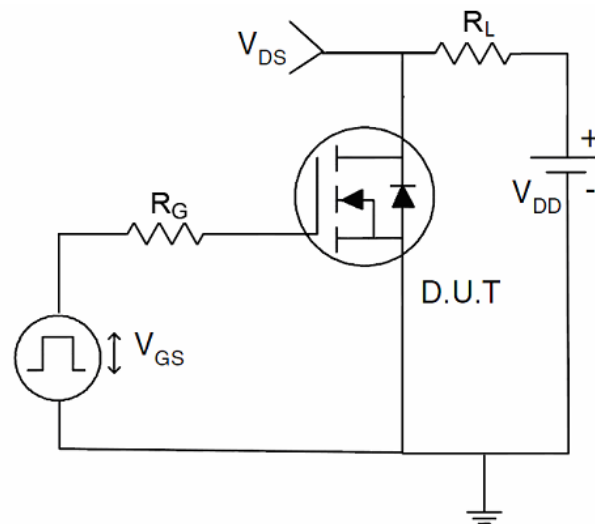
(1)、EAS Test Circuit



(2)、Gate Charge Test Circuit

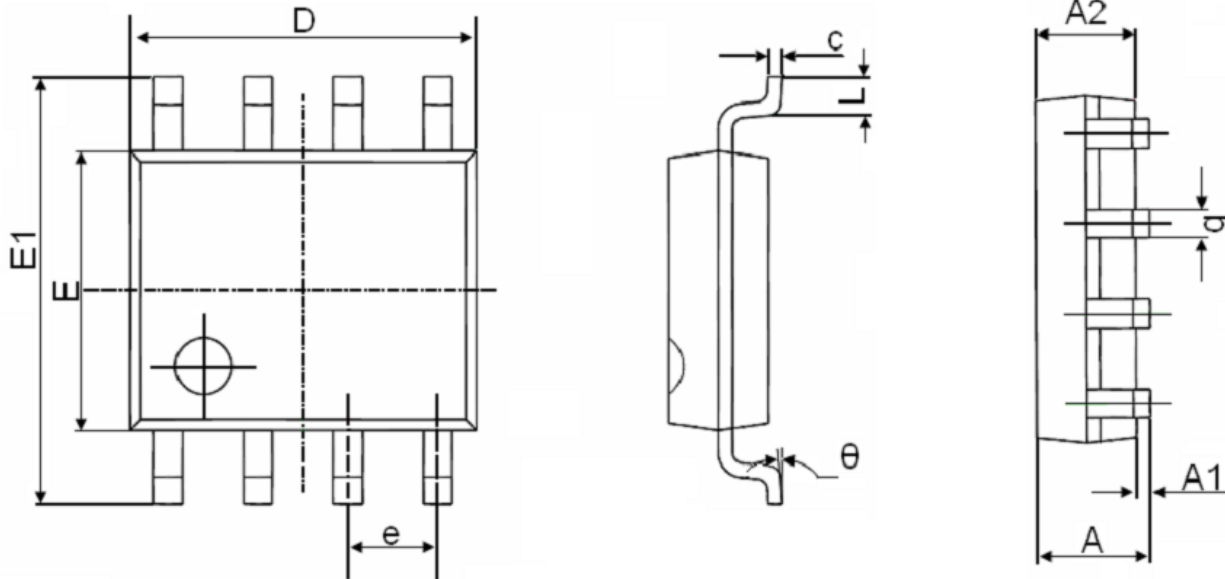


(3)、Switch Time Test Circuit



Package Information

- SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°