Features

- Supply Voltage: 4.5V to 36V
- Rail to Rail Output
- Bandwidth: 6 MHz
- Slew Rate: 20V/μs
- Excellent EMI Suppress Performance
- Offset Voltage: ±100μV Maximum
- Offset Voltage Temperature Drift: 2 μV/°C
- Low Noise: 25 nV/√Hz at 1kHz
- –40°C to 125°C Operation Temperature Range

Applications

- Instrumentation
- Active Filters, ASIC Input or Output Amplifier
- Sensor Interface
- Motor Control
- Industrial Control

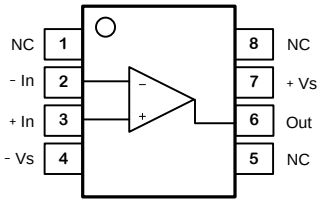
Description

The TP17 is newest high supply voltage amplifiers with low offset, low power and stable high frequency response. It incorporates 3PEAK's proprietary and patented design techniques to achieve very good AC performance with 6MHz bandwidth, 20V/μs slew rate and low distortion while drawing only 1500μA of quiescent current per amplifier. The input common-mode voltage range extends to V–, and the outputs swing rail-to-rail. The TP17 family can be used as plug-in replacements for many commercially available op-amps to reduce power and improve input/output range and performance.

The combination of features makes the TP17 ideal choices for industrial control, instrumentation.

Pin Configuration

TP17
8-Pin SOIC
(-S Suffix)



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Revision History

Date	Revision	Notes
2018/4/21	Rev.Pre	Pre-Release Version
2018/10/5	Rev.0	Initial Vesion

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity
TP17-SR	-40 to 125°C	8-Pin SOIC	TP17 XXXX Note 1	3	Tape and Reel, 4000

Note 1: XXXX identify the manufacture information.

Absolute Maximum Ratings Note 1

Parameters	Rating
Supply Voltage, $(+V_S)$– $(-V_S)$	40 V
Input Voltage	$(-V_S)$ – 0.3 to $(+V_S)$ + 0.3
Differential Input Voltage	$(+V_S)$ - $(-V_S)$
Input Current: +IN, –IN Note 2	±10mA
Output Short-Circuit Duration Note 3	Infinite
Maximum Junction Temperature	150°C
Operating Temperature Range	–40 to 125°C
Storage Temperature Range	–65 to 150°C
Lead Temperature (Soldering, 10 sec)	260°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 300mV beyond the power supply, the input current should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD Rating

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	1	kV

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
8-Pin SOIC	158	43	°C/W

Electrical Characteristics

All test condition is V_S = 30V, T_A = 25°C, R_L = 10kΩ, unless otherwise noted.

Symbol	Parameter	Conditions	T_A	Min	Typ	Max	Unit
Power Supply							
V_S	Supply Voltage Range			4.5		36	V
I_Q	Quiescent Current per Amplifier	V_S = 30V			1.5	2	mA
			-40°C to 125°C			3	mA
PSRR	Power Supply Rejection Ratio	V_S = 4.5V to 36V		105	130		dB
			-40°C to 125°C	100			dB
Input Characteristics							
V_{OS}	Input Offset Voltage	V_S = 30V, V_{CM} = 15V		-100	50	100	μV
			-40°C to 85°C	-400		400	μV
			-40°C to 125°C	-600		600	μV
		V_S = 25V, V_{CM} = 12.5V		-100	50	100	μV
			-40°C to 85°C	-400		400	μV
			-40°C to 125°C	-600		600	μV
		V_S = 5V, V_{CM} = 2.5V		-150	50	150	μV
			-40°C to 85°C	-500		500	μV
			-40°C to 125°C	-600		600	μV
V_{OS} TC	Input Offset Voltage Drift		-40°C to 125°C		1		μV/°C
I_B	Input Bias Current				25		pA
			-40°C to 85°C		80		pA
			-40°C to 125°C		1000		pA
I_{OS}	Input Offset Current				25		pA
I_{IN}	Different Input Current	V_S = 36V, V_{ID} = 36V			10	100	nA
			-40°C to 125°C		100	300	nA
C_{IN}	Input Capacitance	Differential Mode			5		pF
		Common Mode			2.5		pF
Av	Open-loop Voltage Gain	V_S = 30V, V_{OUT} = 0.5V to 29.5V		120	130		dB
			-40°C to 125°C	105			dB
V_{CMR}	Common-mode Input Voltage Range			(V-)		(V+) – 1.5	V
CMRR	Common Mode Rejection Ratio	V_{CM} = 0.5V to 28.5V		100	125		dB
			-40°C to 125°C	95			dB

Output Characteristics							
V_{OH}	Output Swing from Positive Rail	R_{LOAD} = 100kΩ to V_S/2			5	15	mV
			-40°C to 85°C			30	mV
			-40°C to 125°C			40	mV
		R_{LOAD} = 10kΩ to V_S/2			50	80	mV
			-40°C to 85°C			120	mV
			-40°C to 125°C			130	mV
V_{OL}	Output Swing from Negative Rail	R_{LOAD} = 100kΩ to V_S/2			5	10	mV
			-40°C to 85°C			20	mV
			-40°C to 125°C			25	mV
		R_{LOAD} = 10kΩ to V_S/2			40	50	mV
			-40°C to 85°C			80	mV
			-40°C to 125°C			100	mV
I_{SC}	Output Short-Circuit Current	Source Current		20	32		mA
		Sink Current		15	25		mA
AC Specifications							
GBW	Gain-Bandwidth Product				6		MHz
SR	Slew Rate	G = 1, 10V step		13	20		V/μs
			-40°C to 125°C	10			V/μs
t_{OR}	Overload Recovery				100		ns
t_S	Settling Time, 0.1%	G = -1, 10V step			0.5		μs
	Settling Time, 0.01%				0.8		μs
PM	Phase Margin	V_S = 36V, R_L=10K, C_L=100pF			60		°
GM	Gain Margin	V_S = 36V, R_L=10K, C_L=100pF			10		dB
Noise Performance							
E_N	Input Voltage Noise	f = 0.1Hz to 10Hz			2		μV_{RMS}
e_N	Input Voltage Noise Density	f = 1kHz			25		nV/√Hz
i_N	Input Current Noise	f = 1kHz			2		fA/√Hz
THD+N	Total Harmonic Distortion and Noise	f = 1kHz, G =1, R_L = 10kΩ, V_{OUT} = 6V_{RMS}			0.0005		%
Thermal Shutdown							
	Thermal Shutdown temperature				170		°C
	Recover Temperature				150		°C

Typical Performance Characteristics

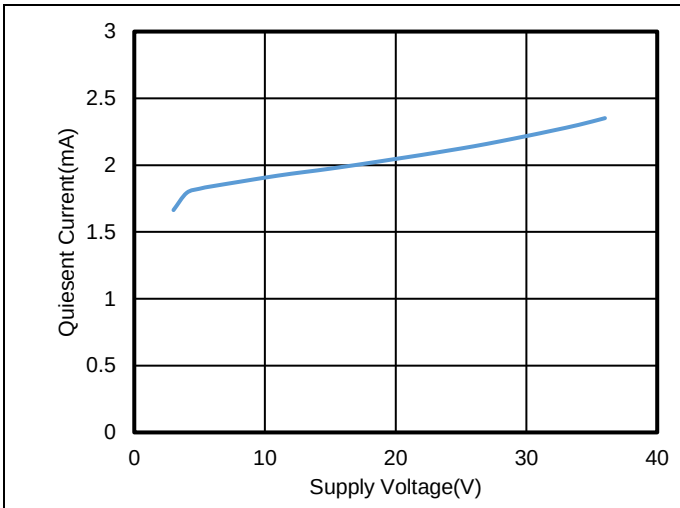


Figure 1. Quiescent Current vs. Supply Voltage, TP1282L1

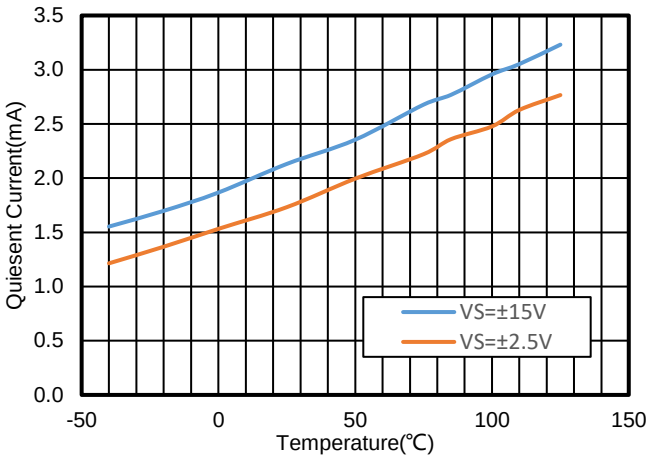


Figure 2. Quiescent Current vs. Temperature, TP1282L1

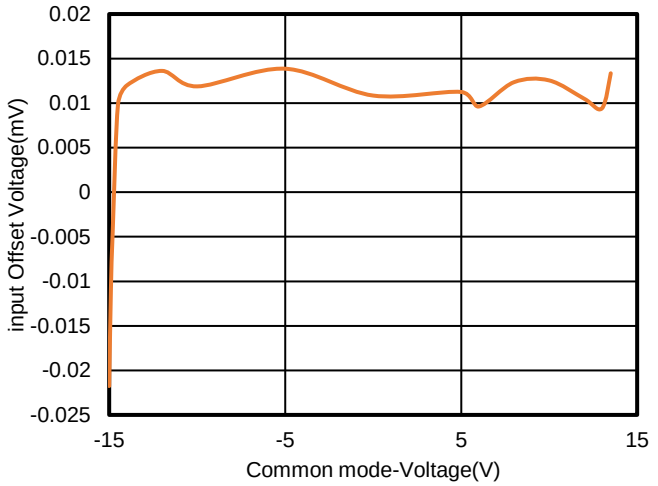


Figure 3. Offset Voltage vs. Common Mode Voltage

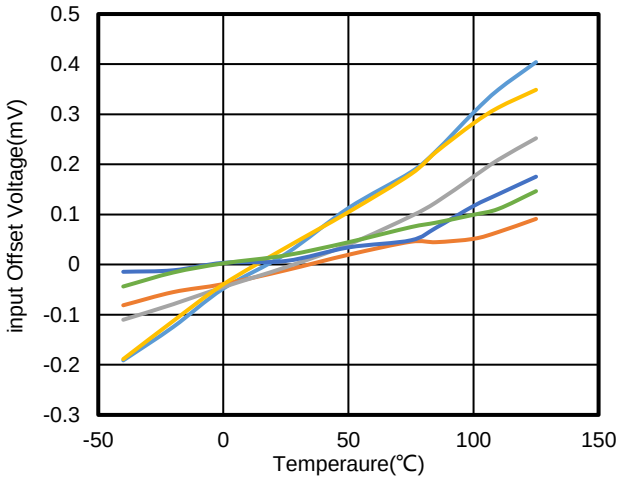


Figure 4. V_{OS} vs. Temperature

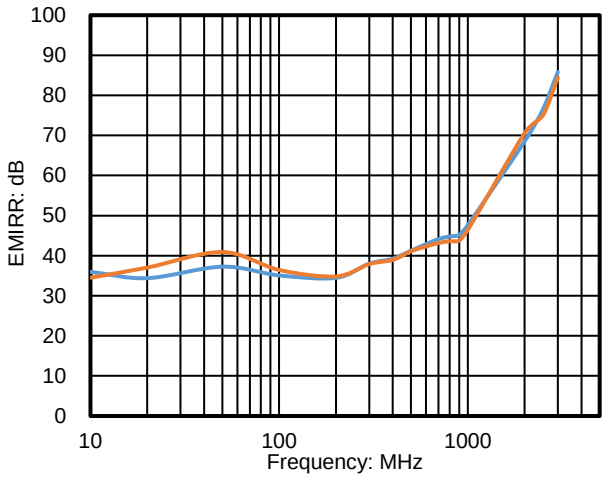


Figure 5. EMIRR vs. Frequency

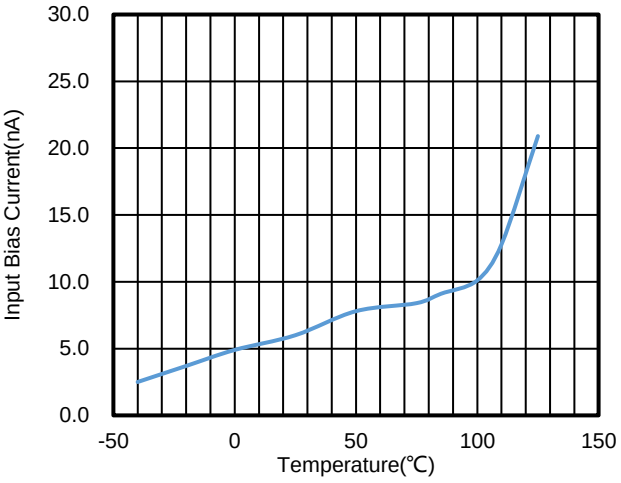


Figure 6. Input Current in Large Vdm vs. Temperature

V_S = ±15V, V_{CM} = 0V, R_L = 10kΩ, unless otherwise specified.

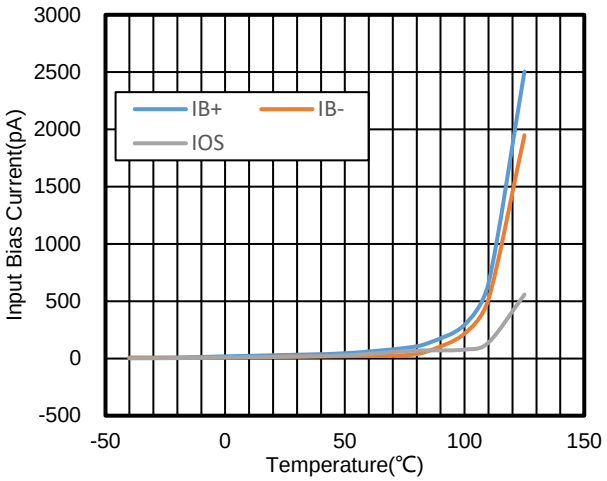


Figure 7. I_B vs. Temperature, -40 to 125°C

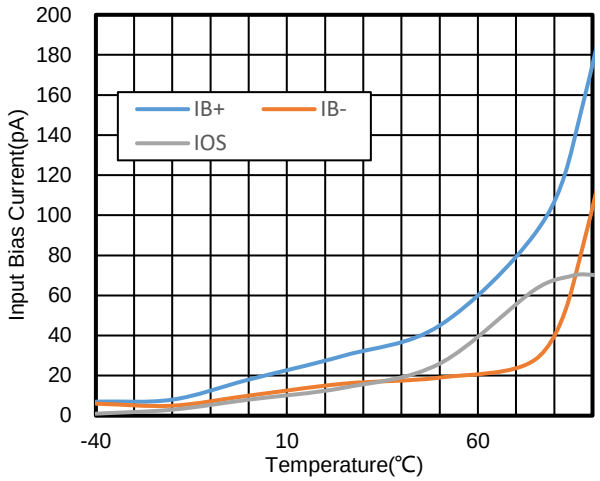


Figure 8. I_B vs. Temperature, -40 to 90°C

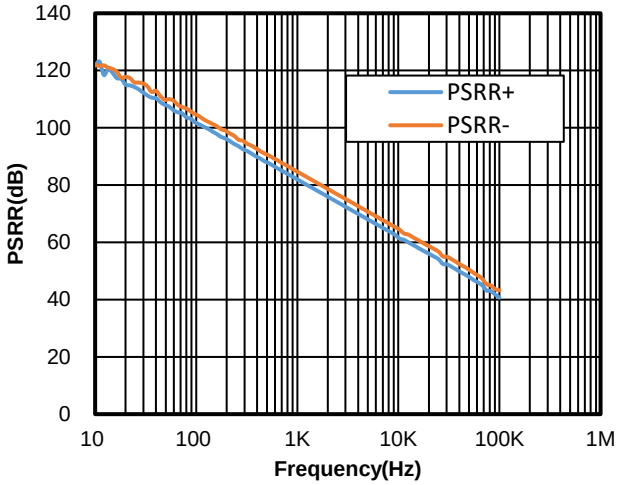


Figure 9. PSRR vs. Frequency

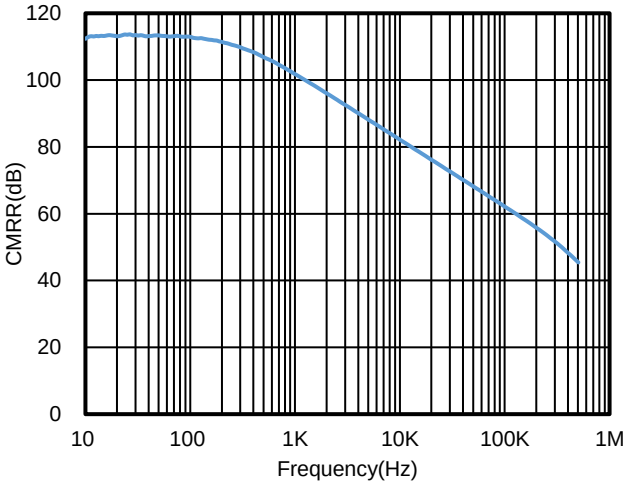


Figure 10. CMRR vs. Frequency

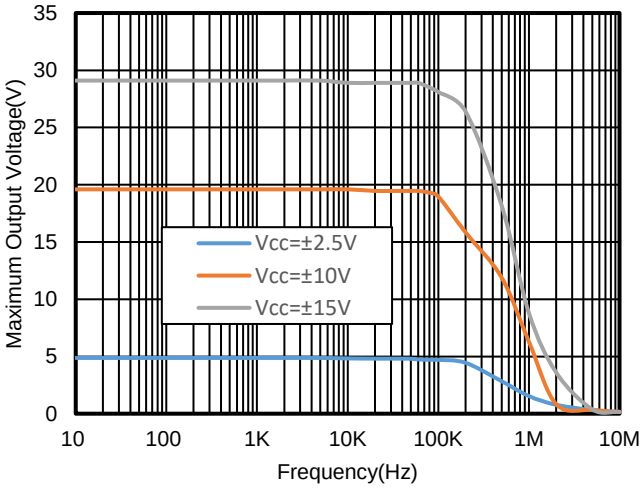


Figure 11. Maximum Output Voltage vs. Frequency

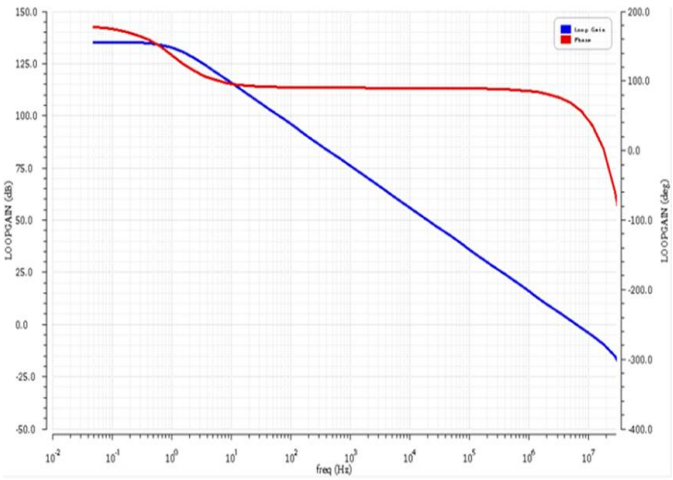


Figure 12. Open Loop Gain and Phase vs. Frequency

R_{LOAD} = 10K, C_{LOAD} = 100pF

V_S = ±15V, V_{CM} = 0V, R_L = 10kΩ, unless otherwise specified.

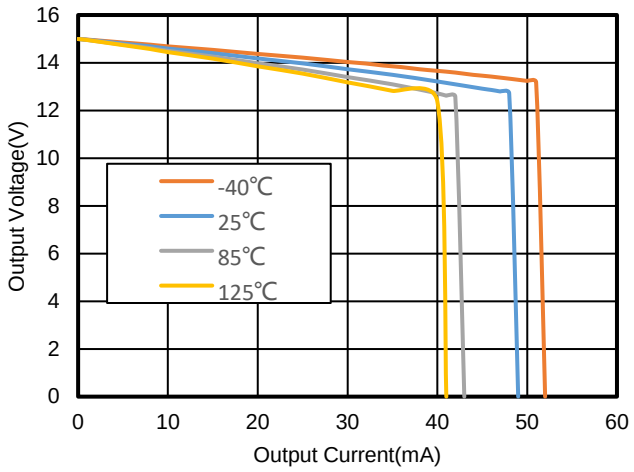


Figure 13. Positive Output Voltage vs. Output Current

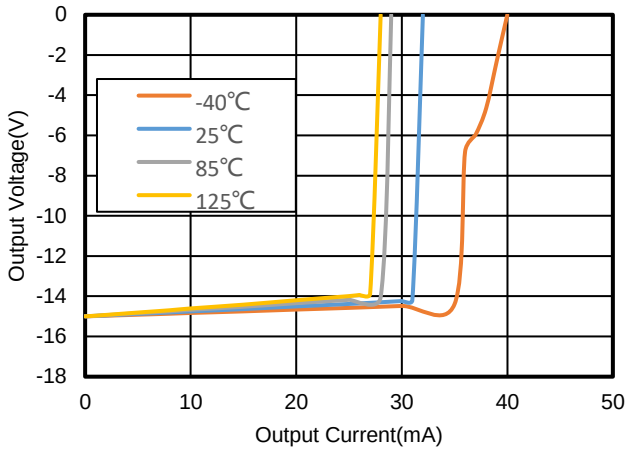
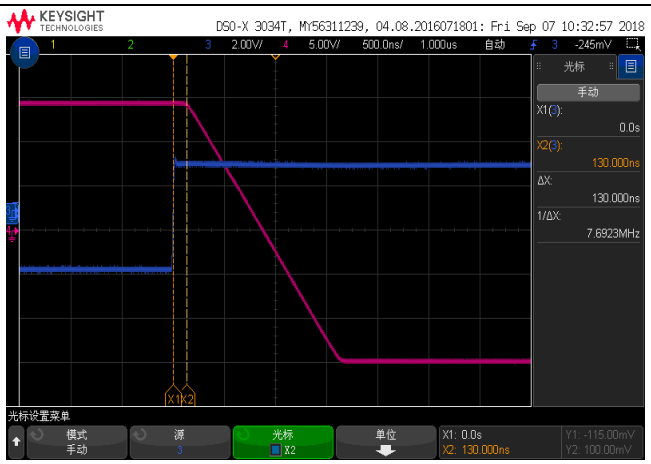


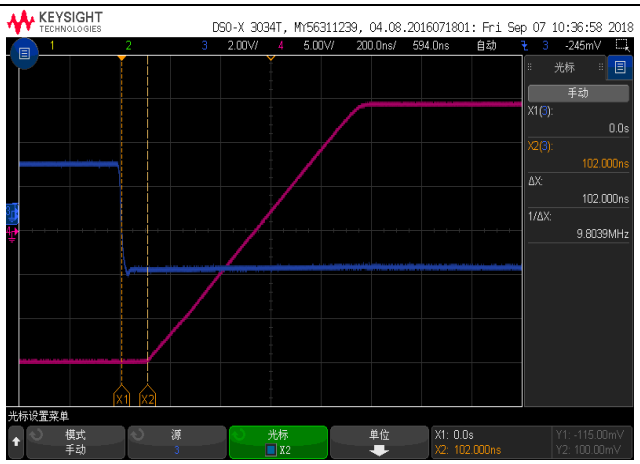
Figure 14. Negative Output Voltage vs. Output Current



Voltage: 5V/div for Output, Time: 500ns/div

G=-10, VREF = GND; VIN=5VPP, Load R=2K C=100pF

Figure 15. Positive Overload Recovery



Voltage: 5V/div for Output, Time: 500ns/div

G=-10, VREF = GND; VIN=5VPP, Load R=2K C=100pF

Figure 16. Negative Overload Recovery

Voltage: 50mV/div, Time: 1μs/div

R_L=2K, C_L=100pF, G=1

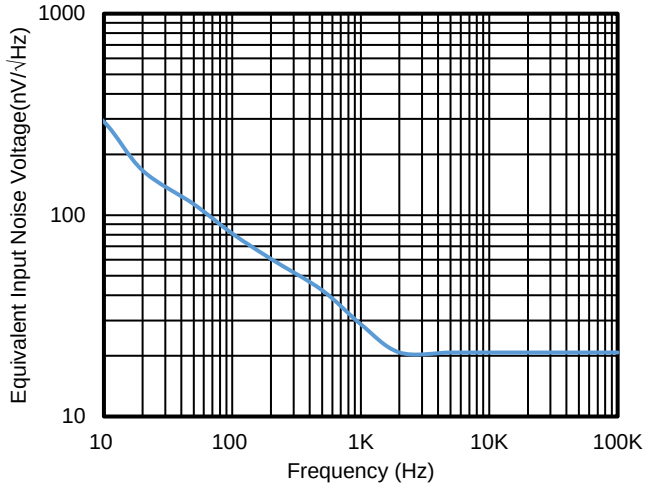
Figure 17. 100mV Signal Step Response

Voltage: 5V/div, Time: 1μs/div

R_L=2K, C_L=100pF, G=1

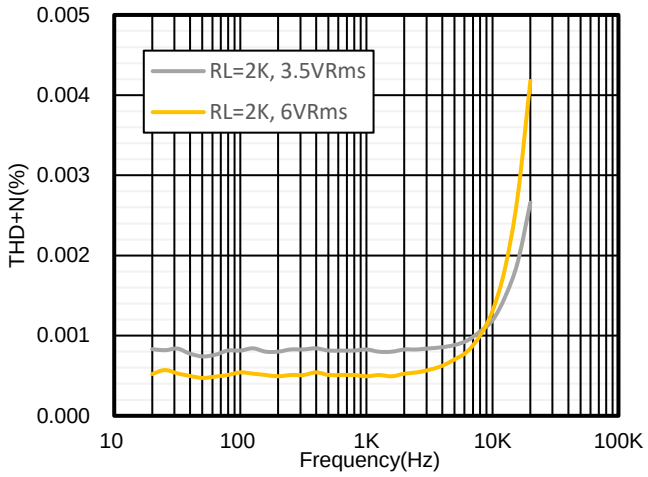
Figure 18. 10V Signal Step Response

V_S = ±15V, V_{CM} = 0V, R_L = 10kΩ, unless otherwise specified.



V_S =±15V, V_{CM}=0V

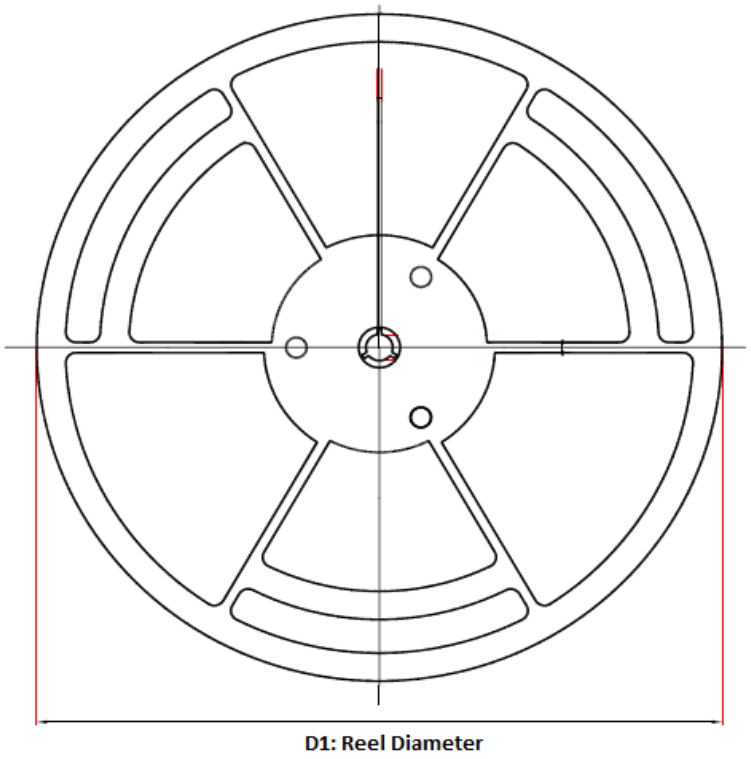
Figure 19. Voltage Noise Spectral Density vs. Frequency

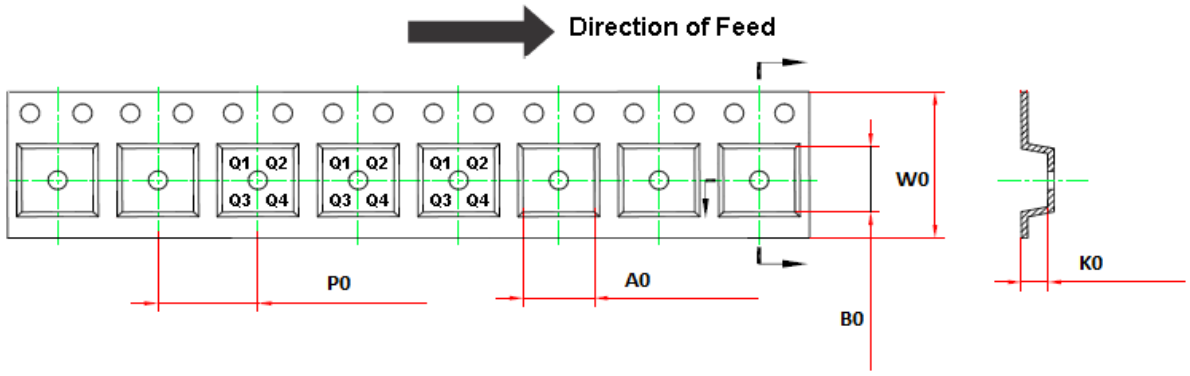


V_S =±15V, V_{CM}=0V, G=1

Figure 20. THD+N vs. Frequency

Tape and Reel Information

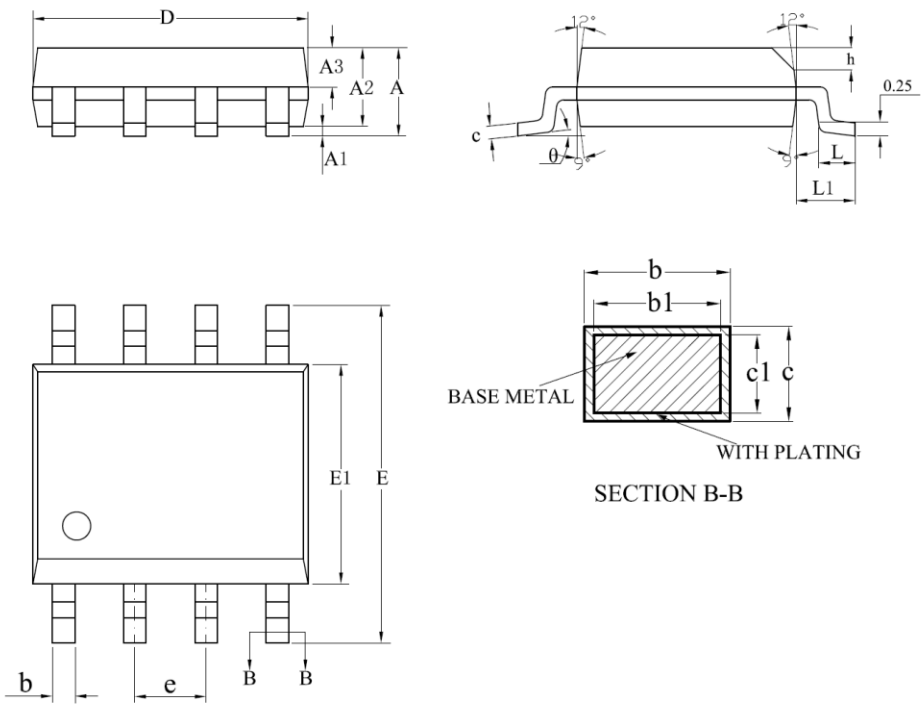




Order Number	Package	D1	W1	A0	B0	K0	P0	W0	Pin1 Quadrant
TP17-SR	8-Pin SOIC	330.0	17.6	6.4	5.4	2.1	8.0	12.0	Q1

Package Outline Dimensions

SOIC-8



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

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