HIP6020A

Advanced Dual PWM and Dual Linear Power Controller

FN4735
Rev 2.00
September 2001

The HIP6020A provides the power control and protection for four output voltages in high-performance, graphics intensive microprocessor and computer applications. The IC integrates two PWM controllers and two linear controllers, as well as the monitoring and protection functions into a 28-pin SOIC package. One PWM controller regulates the microprocessor core voltage with a synchronous-rectified buck converter. The second PWM controller supplies the computer system's AGP 1.5V or 3.3V bus power with a standard buck converter. The linear controllers regulate power for the 1.5V GTL bus and the 1.8V power for the North/South Bridge core voltage and/or cache memory circuits.

The HIP6020A includes an Intel-compatible, TTL 5-input digital-to-analog converter (DAC) that adjusts the core PWM output voltage from $1.3V_{DC}$ to $2.05V_{DC}$ in 0.05V steps and from $2.1V_{DC}$ to $3.5V_{DC}$ in 0.1V increments. The precision reference and voltage-mode control provide ±1% static regulation. The second PWM controller's output is user-selectable, through a TTL-compatible signal applied at the SELECT pin, for levels of 1.5V (±3%) or fully ON switch. The linear regulators use external N-Channel MOSFETs or bipolar NPN pass transistors to provide output voltages of 1.5V ±3% (V_{OUT3}) and 1.8V ±3% (V_{OUT4}).

The HIP6020A monitors all the output voltages. A single Power Good signal is issued when the core is within ±10% of the DAC setting and all other outputs are above their under-voltage levels. Additional built-in over-voltage protection for the core output uses the lower MOSFET to prevent output voltages above 115% of the DAC setting. The PWM controllers' over-current function monitors the output current by using the voltage drop across the upper MOSFET's $r_{DS(ON)}$, eliminating the need for a current sensing resistor.

Related Literature

- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HIP6020ACB	0 to 70	28 Ld SOIC	M28.3

Features

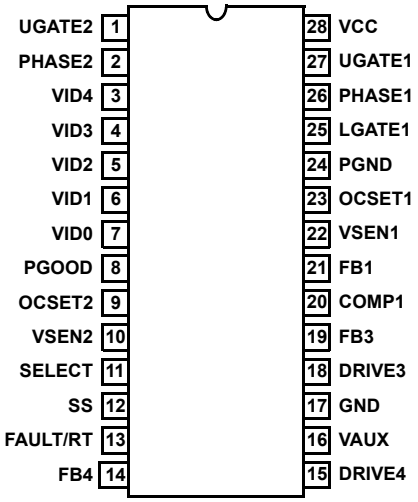
- Provides 4 Regulated Voltages
  - Microprocessor Core, AGP Bus, North/South Bridge and/or Cache Memory, and GTL Bus Power
- Drives N-Channel MOSFETs
- Linear Regulator Drives Compatible with both MOSFET and Bipolar Series Pass Transistors
- Simple Single-Loop Control Designs
  - Voltage-Mode PWM Control
- Fast PWM Converter Transient Response
  - High-Bandwidth Error Amplifiers
  - Full 0% to 100% Duty Ratios
- Excellent Output Voltage Regulation
  - Core PWM Output: ±1% Over Temperature
  - AGP Bus PWM Output: ±3% Over Temperature (1.5V Setting Only)
  - Other Outputs: ±3% Over Temperature
- TTL-Compatible 5 Bit DAC Microprocessor Core Output Voltage Selection
  - Wide Range - $1.3V_{DC}$ to $3.5V_{DC}$
- Power-Good Output Voltage Monitor
- Over-Voltage and Over-Current Fault Monitors
  - Switching Regulators Use MOSFET's $r_{DS(ON)}$ Sensing
- Small Converter Size
  - Constant Frequency Operation
  - 200kHz Free-Running Oscillator; Programmable From 50kHz to Over 1MHz
  - Small External Component Count

Applications

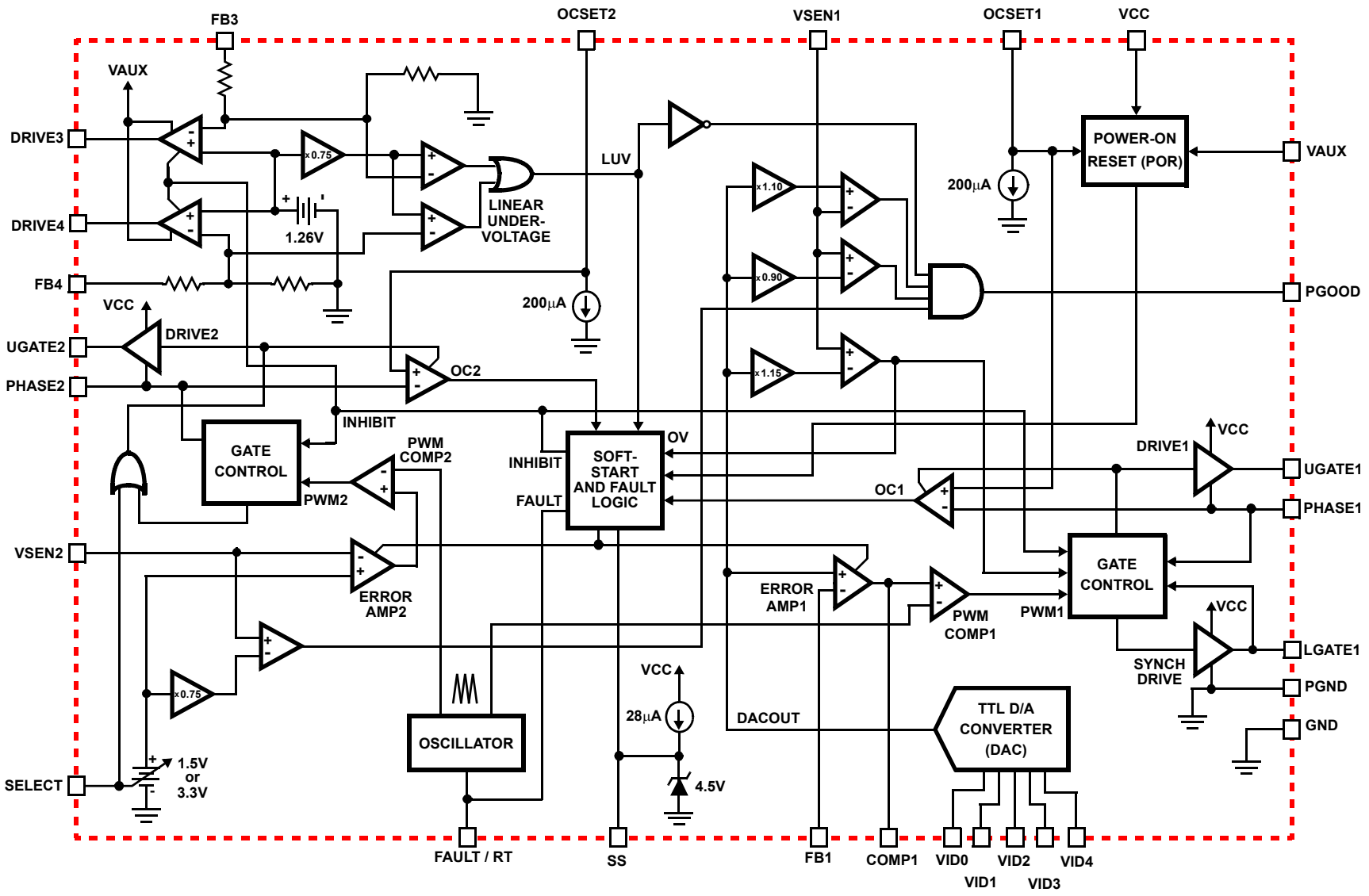
- Motherboard Power Regulation for Computers

Pinout

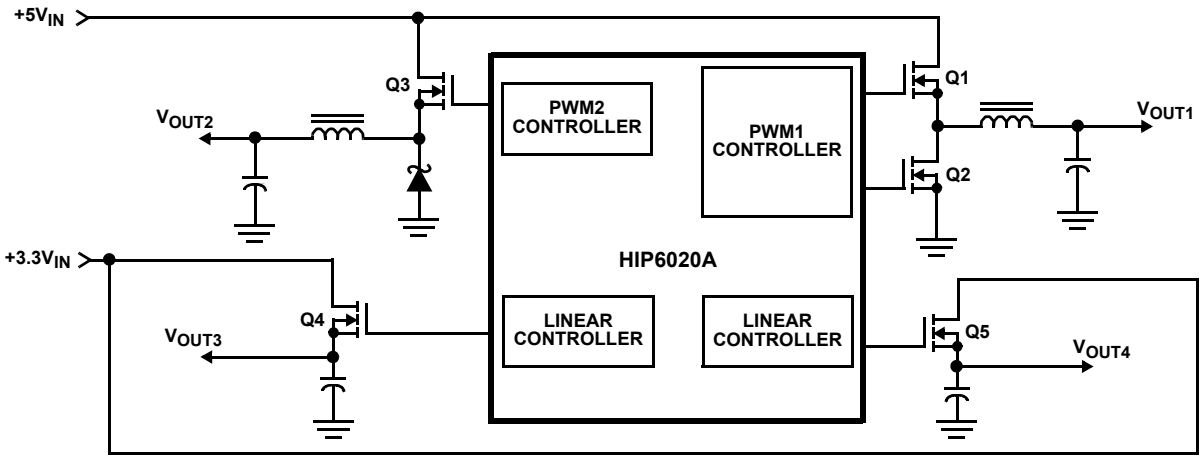
HIP6020A (SOIC)
TOP VIEW



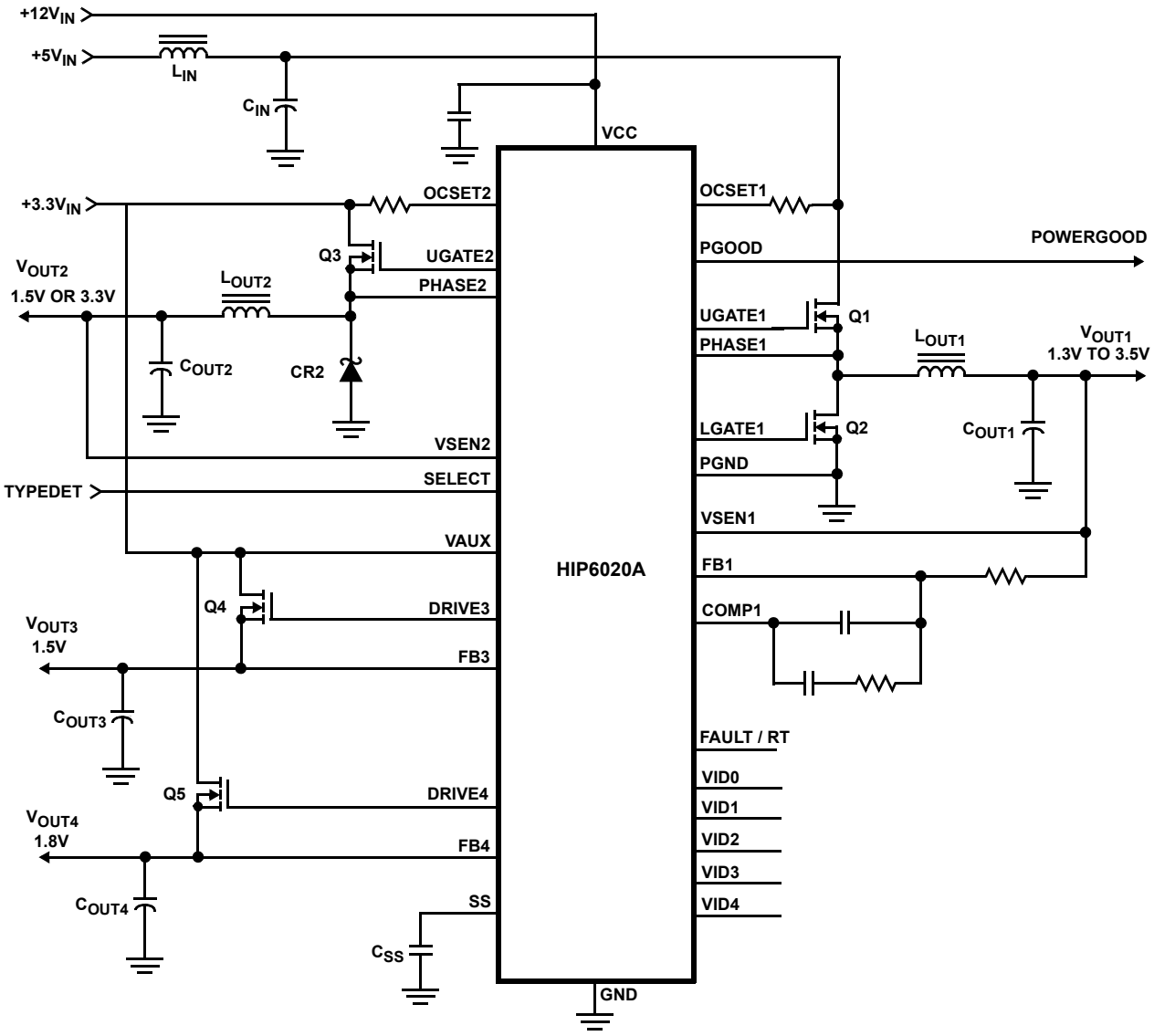
Block Diagram



Simplified Power System Diagram



Typical Application



Absolute Maximum Ratings

Supply Voltage, V_{CC} . . . . . +15V
PGOOD, RT/FAULT, DRIVE, PHASE, and
GATE Voltage . . . . . GND - 0.3V to V_{CC} + 0.3V
Input, Output or I/O Voltage . . . . . GND -0.3V to 7V
ESD Classification . . . . . Class 1

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . +12V ±10%
Ambient Temperature Range. . . . . 0^oC to 70^oC
Junction Temperature Range . . . . . 0^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^oC/W$)
SOIC Package 70
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θJA is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted. Refer to Figures 1, 2 and 3

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT						
Nominal Supply Current	I_{CC}	UGATE1, LGATE1, UGATE2, DRIVE3, and DRIVE4 Open	-	9	-	mA
POWER-ON RESET						
Rising VCC Threshold		V_{OCSET} = 4.5V	-	-	10.4	V
Falling VCC Threshold		V_{OCSET} = 4.5V	8.2	-	-	V
Rising VAUX Threshold		V_{OCSET} = 4.5V	-	2.5	-	V
VAUX Threshold Hysteresis		V_{OCSET} = 4.5V	-	0.5	-	V
Rising V_{OCSET1} Threshold			-	1.26	-	V
OSCILLATOR						
Free Running Frequency	F_{OSC}	RT = OPEN	185	200	215	kHz
Total Variation		6kΩ < RT to GND < 200kΩ	-15	-	+15	%
Ramp Amplitude	ΔV_{OSC}	RT = Open	-	1.9	-	V_{P-P}
DAC AND STANDARD BUCK REGULATOR REFERENCE						
DAC(VID0-VID4) Input Low Voltage					0.8	V
DAC(VID0-VID4) Input High Voltage			2.0			V
DACOUT Voltage Accuracy			-1.0	-	+1.0	%
PWM2 Reference Voltage		SELECT < 0.8V	-	1.5	-	V
PWM2 Reference Voltage Tolerance			-	3	-	%
LINEAR REGULATORS (V_{OUT3} AND V_{OUT4})						
Regulation			-	3	-	%
FB3 Regulation Voltage	$VREG_3$		-	1.5	-	V
FB4 Regulation Voltage	$VREG_4$		-	1.8	-	V
FB3,4 Under-Voltage Level	FB_{UV}	FB Rising	-	75	-	%
FB3,4 Under-Voltage Hysteresis				7		%
Output Drive Current		VAUX-V_{DRIVE} > 0.6V	20	40	-	mA

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted. Refer to Figures 1, 2 and 3 **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SYNCHRONOUS PWM CONTROLLER ERROR AMPLIFIER						
DC Gain			-	88	-	dB
Gain-Bandwidth Product	GBWP		-	15	-	MHz
Slew Rate	SR	COMP1 = 10pF	-	6	-	V/µs
PWM CONTROLLERS GATE DRIVERS						
UGATE1,2 Source	I_{UGATE}	VCC = 12V, V_{UGATE1} (or V_{UGATE2}) = 6V	-	1	-	A
UGATE1,2 Sink	R_{UGATE}	$V_{GATE-PHASE}$ = 1V	-	1.7	3.5	Ω
LGATE Source	I_{LGATE}	VCC = 12V, V_{LGATE1} = 1V	-	1	-	A
LGATE Sink	R_{LGATE}	V_{LGATE} = 1V	-	1.4	3.0	Ω
PROTECTION						
VSEN1 Over-Voltage (VSEN1/DACOUT)		VSEN1 Rising	-	115	120	%
FAULT Sourcing Current	I_{OVP}	$V_{FAULT/RT}$ = 2.0V	-	8.5	-	mA
OCSET1,2 Current Source	I_{OCSET}	V_{OCSET} = 4.5V_{DC}	170	200	230	µA
Soft-Start Current	I_{SS}		-	28	-	µA
VSEN2 Under-Voltage Threshold		SELECT < 0.8V	-	75	-	%
		SELECT > 2.0V	-	2.475	-	V
VSEN2 Under-Voltage Hysteresis		SELECT < 0.8V	-	7	-	%
		SELECT > 2.0V	-	0.231	-	V
POWER GOOD						
VSEN1 Upper Threshold (VSEN1/DACOUT)		VSEN1 Rising	108	-	110	%
VSEN1 Under-Voltage (VSEN1/DACOUT)		VSEN1 Rising	92	-	94	%
VSEN1 Hysteresis (VSEN1/DACOUT)		Upper/Lower Threshold	-	2	-	%
PGOOD Voltage Low	V_{PGOOD}	I_{PGOOD} = -4mA	-	-	0.8	V

Typical Performance Curves

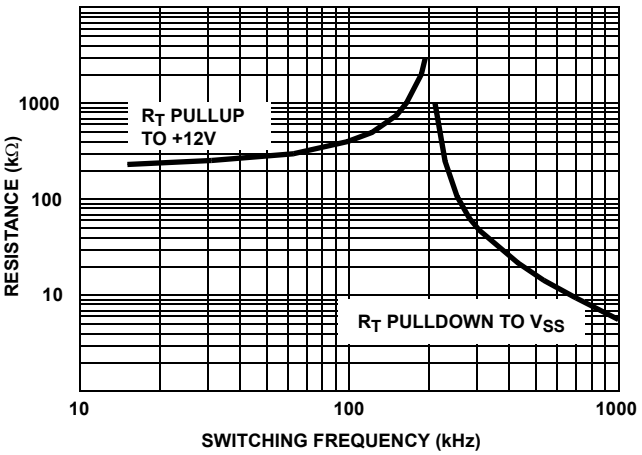


FIGURE 1. R_T RESISTANCE vs FREQUENCY

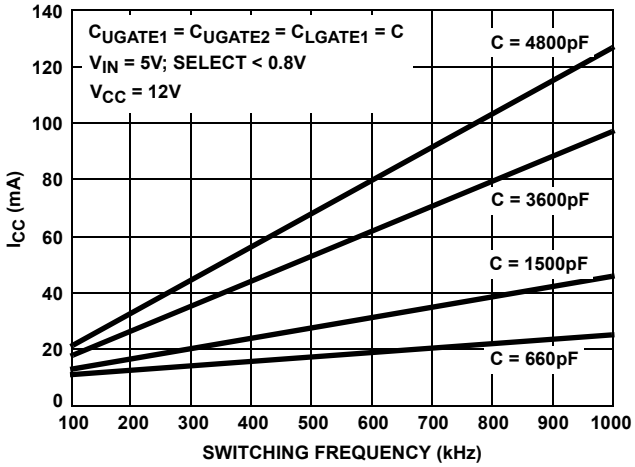


FIGURE 2. BIAS SUPPLY CURRENT vs FREQUENCY

Functional Pin Descriptions

VCC (Pin 28)

Provide a 12V bias supply for the IC to this pin. This pin also provides the gate bias charge for all the MOSFETs controlled by the IC. The voltage at this pin is monitored for Power-On Reset (POR) purposes.

GND (Pin 17)

Signal ground for the IC. All voltage levels are measured with respect to this pin.

PGND (Pin 24)

This is the power ground connection. Tie the synchronous PWM converter's lower MOSFET source to this pin.

VAUX (Pin 16)

The +3.3V input voltage at this pin is monitored for power-on reset (POR) purposes. Connected to +5V input, this pin provides boost current for the two linear regulator output drives in the event bipolar NPN transistors (instead of N-Channel MOSFETs) are employed as pass elements.

SS (Pin 12)

Connect a capacitor from this pin to ground. This capacitor, along with an internal 28µA current source, sets the soft-start interval of the converter.

FAULT / RT (Pin 13)

This pin provides oscillator switching frequency adjustment. By placing a resistor (R_T) from this pin to GND, the nominal 200kHz switching frequency is increased according to the following equation:

$$Fs \approx 200KHz + \frac{5 \times 10^6}{R_{T(k\Omega)}} \quad (R_T \text{ to GND})$$

Conversely, connecting a pull-up resistor (R_T) from this pin to VCC reduces the switching frequency according to the following equation:

$$Fs \approx 200KHz - \frac{4 \times 10^7}{R_{T(k\Omega)}} \quad (R_T \text{ to 12V})$$

Nominally, the voltage at this pin is 1.26V. In the event of an over-voltage or over-current condition, this pin is internally pulled to VCC.

PGOOD (Pin 8)

PGOOD is an open collector output used to indicate the status of the output voltages. This pin is pulled low when the synchronous regulator output is not within ±10% of the DACOUT reference voltage or when any of the other outputs are below their under-voltage thresholds.

The PGOOD output is open for '11111' VID code.

VID0, VID1, VID2, VID3, VID4 (Pins 7, 6, 5, 4 and 3)

VID0-4 are the TTL-compatible input pins to the 5-bit DAC. The logic states of these five pins program the internal voltage reference (DACOUT). The level of DACOUT sets the microprocessor core converter output voltage, as well as the corresponding PGOOD and OVP thresholds.

OCSET1, OCSET2 (Pins 23 and 9)

Connect a resistor (R_{OCSET}) from this pin to the drain of the respective upper MOSFET. R_{OCSET}, an internal 200µA current source (I_{OCSET}), and the upper MOSFET's on-resistance ($r_{DS(ON)}$) set the converter over-current (OC) trip point according to the following equation:

$$I_{PEAK} = \frac{I_{OCSET} \times R_{OCSET}}{r_{DS(ON)}}$$

An over-current trip cycles the soft-start function.

The voltage at OCSET1 pin is monitored for power-on reset (POR) purposes.

PHASE1, PHASE2 (Pins 26 and 2)

Connect the PHASE pins to the respective PWM converter's upper MOSFET source. These pins represent the gate drive return current path and are used to monitor the voltage drop across the upper MOSFETs for over-current protection.

UGATE1, UGATE2 (Pins 27 and 1)

Connect UGATE pins to the respective PWM converter's upper MOSFET gate. These pins provide the gate drive for the upper MOSFETs. For SELECT high, UGATE2 is turned on continuously to provide a DC current flow path to V_{OUT2}.

LGATE1 (Pin 25)

Connect LGATE1 to the synchronous PWM converter's lower MOSFET gate. This pin provides the gate drive for the lower MOSFET.

COMP1 and FB1 (Pins 20, and 21)

COMP1 and FB1 are the available external pins of the synchronous PWM regulator error amplifier. The FB1 pin is the inverting input of the error amplifier. Similarly, the COMP1 pin is the error amplifier output. These pins are used to compensate the voltage-mode control feedback loop of the synchronous PWM converter.

VSEN1 (Pin 22)

This pin is connected to the synchronous PWM converters' output voltage. The PGOOD and OVP comparator circuits use this signal to report output voltage status and for over- voltage protection.

VSEN2 (Pin 10)

Connect this pin to the output of the standard buck PWM regulator. The voltage at this pin is regulated to 1.5V if the SELECT pin is low. This pin is also monitored by the PGOOD comparator circuit.

SELECT (Pin 11)

This pin determines the output voltage of the AGP bus switching regulator. A low TTL input sets the output voltage to

1.5V, while a high input turns Q3 on continuously, providing a DC current path from the input (+3.3V) to the output (V_{OUT2}) of the AGP controller.

DRIVE3 (Pin 18)

Connect this pin to the gate of an external MOSFET. This pin provides the drive for the 1.5V regulator's pass transistor.

FB3 (Pin 19)

Connect this pin to the output of the 1.5V linear regulator. This pin is monitored for undervoltage events.

DRIVE4 (Pin 15)

Connect this pin to the gate of an external MOSFET. This pin provides the drive for the 1.8V regulator's pass transistor.

FB4 (Pin 14)

Connect this pin to the output of the linear 1.8V regulator. This pin is monitored for undervoltage events.

Description

Operation

The HIP6020A monitors and precisely controls 4 output voltage levels (Refer to Block, Power System, and Typical Application Diagrams). It is designed for microprocessor computer applications with 3.3V, 5V, and 12V bias input from an ATX power supply. The IC has 2 PWM and two linear controllers. The first PWM controller (PWM1) is designed to regulate the microprocessor core voltage (V_{OUT1}). PWM1 controller drives 2 MOSFETs (Q1 and Q2) in a synchronous-rectified buck converter and regulates the core voltage to a level programmed by the 5-bit digital-to-analog converter (DAC). The second PWM controller (PWM2) is designed to regulate the advanced graphics port (AGP) bus voltage (V_{OUT2}). PWM2 controller drives a MOSFET (Q3) in a standard buck converter and regulates the output voltage to a level of 1.5V or fully on to output 3.3V. Selection of either output voltage is achieved by applying the proper logic level at the SELECT pin. The two linear controllers supply the 1.5V GTL bus power (V_{OUT3}) and the 1.8V memory power (V_{OUT4}).

Initialization

The HIP6020A automatically initializes upon receipt of input power. Special sequencing of the input supplies is not necessary. The Power-On Reset (POR) function continually monitors the input supply voltages. The POR monitors the bias voltage ($+12V_{IN}$) at the VCC pin, the 5V input voltage ($+5V_{IN}$) on the OCSET1 pin, and the 3.3V input voltage ($+3.3V_{IN}$) at the VAUX pin. The normal level on OCSET1 is equal to $+5V_{IN}$ less a fixed voltage drop (see over-current protection). The POR function initiates soft-start operation after all supply voltages exceed their POR thresholds.

Soft-Start

The POR function initiates the soft-start sequence. Initially, the voltage on the SS pin rapidly increases to approximately 1V (this minimizes the soft-start interval). Then an internal 28µA current source charges an external capacitor (C_{SS}) on the SS pin to 4.5V.

The PWM error amplifiers reference inputs (+ terminal) and outputs (COMP1 pin) are clamped to a level proportional to the SS pin voltage. As the SS pin voltage slews from 1V to 4V, the output clamp allows generation of PHASE pulses of increasing width that charge the output capacitor(s). After the output voltage increases to approximately 70% of the set value, the reference input clamp slows the output voltage rate-of-rise and provides a smooth transition to the final set voltage. Additionally both linear regulators' reference inputs are clamped to a voltage proportional to the SS pin voltage. This method provides a rapid and controlled output voltage rise.

Figure 3 shows the soft-start sequence for the typical application. At T0 the SS voltage rapidly increases to approximately 1V. At T1, the SS pin and error amplifier output voltage reach the valley of the oscillator's triangle wave. The oscillator's triangular wave form is compared to the clamped error amplifier output voltage. As the SS pin voltage increases, the pulse-width on the PHASE pin increases. The interval of increasing pulse-width continues until each PWM output reaches sufficient voltage to transfer control to the error amplifier input reference clamp. If we consider the core output (V_{OUT1}) in Figure 3, this time occurs at T2. During the interval between T2 and T3, the error amplifier reference ramps to the final value and the converter regulates the output a voltage proportional to the SS pin voltage. At T3 the input clamp voltage exceeds the reference voltage and the output voltage is in regulation.

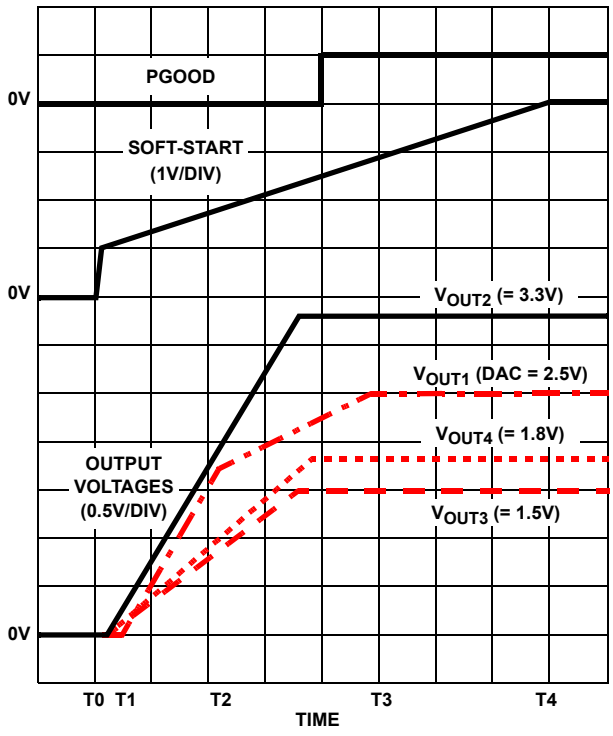


FIGURE 3. SOFT-START INTERVAL

The remaining outputs are also programmed to follow the SS pin voltage. The PGOOD signal toggles 'high' when all output voltage levels have exceeded their under-voltage levels. See the Soft-Start Interval section under Applications Guidelines for a procedure to determine the soft-start interval.

Fault Protection

All four outputs are monitored and protected against extreme overload. A sustained overload on any output or an over-voltage on V_{OUT1} output (VSEN1) disables all outputs and drives the FAULT/RT pin to VCC.

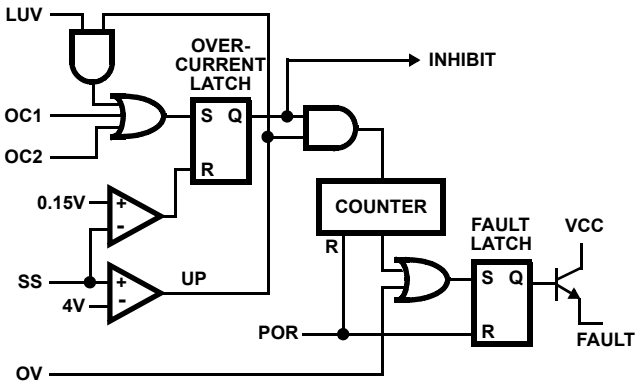


FIGURE 4. FAULT LOGIC - SIMPLIFIED SCHEMATIC

Figure 4 shows a simplified schematic of the fault logic. An over-voltage detected on VSEN1 immediately sets the fault latch. A sequence of three over-current fault signals also sets the fault latch. The over-current latch is set dependent upon the states of the over-current (OC1 and OC2), linear under-voltage (LUV) and the soft-start signals. A window comparator monitors the SS pin and indicates when C_{SS} is fully charged to 4.5V (UP signal). An under-voltage on either linear output (sensed at FB3 and FB4) is ignored until after the soft-start interval (T4 in Figure 3). This allows V_{OUT3} and V_{OUT4} to increase without fault at start-up. Cycling the bias input voltage ($+12V_{IN}$ on the VCC pin off then on) resets the counter and the fault latch.

Over-Voltage Protection

During operation, a short across the synchronous PWM upper MOSFET (Q1) causes V_{OUT1} to increase. When the output exceeds the over-voltage threshold of 115% of DACOUT, the over-voltage comparator trips to set the fault latch and turns the lower MOSFET (Q2) on. This blows the input fuse and reduces V_{OUT1}. The fault latch raises the FAULT/RT pin to VCC.

A separate over-voltage circuit provides protection during the initial application of power. For voltages on the VCC pin below the power-on reset (and above ~4V), the output level is monitored for voltages above 1.3V. Should VSEN1 exceed this level, the lower MOSFET, Q2 is driven on.

Over-Current Protection

All outputs are protected against excessive over-currents. Both PWM controllers use the upper MOSFET's on-resistance, $r_{DS(ON)}$ to monitor the current for protection against shorted outputs. Both linear regulators monitor their respective FB pins for under-voltage to protect against excessive currents.

Figure 5 illustrates the over-current protection with an overload on OUT2. The overload is applied at T0 and the current increases through the inductor (L_{OUT2}). At time T1, the OVER-CURRENT2 comparator trips when the voltage across Q3 ($i_D \cdot r_{DS(ON)}$) exceeds the level programmed by R_{OCSET}. This inhibits all outputs, discharges the soft-start capacitor (C_{SS}) with a 28µA current sink, and increments the counter. C_{SS} recharges at T2 and initiates a soft-start cycle with the error amplifiers clamped by soft-start. With OUT2 still overloaded, the inductor current increases to trip the over-current comparator. Again, this inhibits all outputs, but the soft-start voltage continues increasing to 4.5V before discharging. The counter increments to 2. The soft-start cycle repeats at T3 and trips the over-current comparator. The SS pin voltage increases to 4.5V at T4 and the counter increments to 3. This sets the fault latch to disable the converter. The fault is reported on the FAULT/RT pin.

The PWM1 controller operates in the same way as PWM2 to over-current faults. Additionally, the two linear controllers monitor the FB pins for an under-voltage. Should excessive currents cause FB3 or FB4 to fall below the linear under-voltage threshold, the LUV signal sets the over-current latch, providing C_{SS} is fully charged. Blanking the LUV signal during the C_{SS} charge interval allows the linear outputs to build above the under-voltage threshold during normal operation. Cycling the bias input power off then on resets the counter and the fault latch.

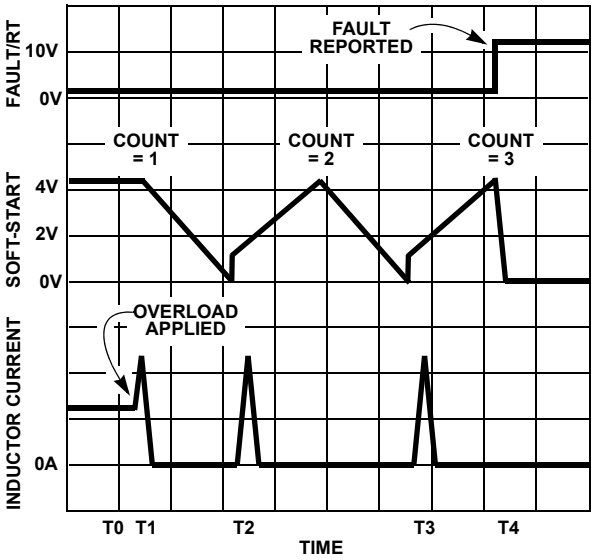


FIGURE 5. OVER-CURRENT OPERATION

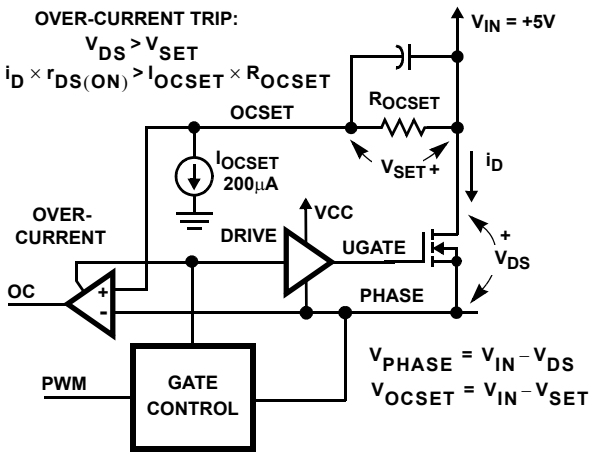


FIGURE 6. OVER-CURRENT DETECTION

Resistors (R_{OCSET1} and R_{OCSET2}) program the over-current trip levels for each PWM converter. As shown in Figure 6, the internal 200µA current sink (I_{OCSET}) develops a voltage across R_{OCSET} (V_{SET}) that is referenced to V_{IN}. The DRIVE signal enables the over-current comparator (OVER-CURRENT1 or OVER-CURRENT2). When the voltage across the upper MOSFET ($V_{DS(ON)}$) exceeds V_{SET}, the over-current comparator trips to set the over-current latch. Both V_{SET} and V_{DS} are referenced to V_{IN} and a small capacitor across R_{OCSET} helps V_{OCSET} track the variations of V_{IN} due to MOSFET switching. The over-current function will trip at a peak inductor current (I_{PEAK}) determined by:

$$I_{PEAK} = \frac{I_{OCSET} \times R_{OCSET}}{r_{DS(ON)}}$$

The OC trip point varies with MOSFET's $r_{DS(ON)}$ temperature variations. To avoid over-current tripping in the normal operating load range, determine the ROCSET resistor value from the equation above with:

1. The maximum $r_{DS(ON)}$ at the highest junction temperature
2. The minimum I_{OCSET} from the specification table
3. Determine I_{PEAK} for $I_{PEAK} > I_{OUT(MAX)} + (\Delta I)/2$, where ΔI is the output inductor ripple current.

For an equation for the ripple current see the section under component guidelines titled 'Output Inductor Selection'.

OUT1 Voltage Program

The output voltage of the PWM1 converter is programmed to discrete levels between $1.3V_{DC}$ and $3.5V_{DC}$. This output (OUT1) is designed to supply the core voltage of Intel's advanced microprocessors. The voltage identification (VID) pins program an internal voltage reference (DACOUT) with a TTL-compatible 5-bit digital-to-analog converter (DAC). The level of DACOUT also sets the PGOOD and OVP thresholds. Table 1 specifies the DACOUT voltage for the different combinations of connections on the VID pins. The VID pins can be left open for a logic 1 input, because they are internally pulled up to an internal voltage of about 5V by a 10µA current source. Changing the VID inputs during operation is not recommended and could toggle the PGOOD signal and exercise the over-voltage protection.

TABLE 1. OUT1 VOLTAGE PROGRAM

PIN NAME					NOMINAL DACOUT VOLTAGE
VID4	VID3	VID2	VID1	VID0	
0	1	1	1	1	1.30
0	1	1	1	0	1.35
0	1	1	0	1	1.40
0	1	1	0	0	1.45
0	1	0	1	1	1.50
0	1	0	1	0	1.55
0	1	0	0	1	1.60
0	1	0	0	0	1.65
0	0	1	1	1	1.70
0	0	1	1	0	1.75
0	0	1	0	1	1.80
0	0	1	0	0	1.85
0	0	0	1	1	1.90
0	0	0	1	0	1.95
0	0	0	0	1	2.00
0	0	0	0	0	2.05
1	1	1	1	1	2.00
1	1	1	1	0	2.1
1	1	1	0	1	2.2
1	1	1	0	0	2.3
1	1	0	1	1	2.4
1	1	0	1	0	2.5
1	1	0	0	1	2.6
1	1	0	0	0	2.7
1	0	1	1	1	2.8
1	0	1	1	0	2.9
1	0	1	0	1	3.0
1	0	1	0	0	3.1
1	0	0	1	1	3.2
1	0	0	1	0	3.3
1	0	0	0	1	3.4
1	0	0	0	0	3.5

NOTE: 0 = connected to GND, 1 = open or connected to 5V through pull-up resistors

OUT2 Voltage Selection

The AGP regulator output voltage is internally set to 1.5V or continuously on, based on the status of the SELECT pin. SELECT pin is internally pulled 'high', such that left open, the standard buck MOSFET will be continuously on, V_{OUT2} being equal to the input voltage (3.3V) less any voltage drop across the MOSFET's $r_{DS(ON)}$ and output inductor's DCR. The other setting available is 1.5V, which can be obtained by grounding the SELECT pin using a jumper or another suitable method capable of sinking a few tens of microamperes. The status of the SELECT pin cannot be changed during operation of the IC without possibly causing a fault condition.

Application Guidelines

Soft-Start Interval

Initially, the soft-start function clamps the error amplifier's output of the PWM converters. This generates PHASE pulses of increasing width that charge the output capacitor(s). After the output voltage increases to approximately 70% of the set value, the reference input of the error amplifier is clamped to a voltage proportional to the SS pin voltage. The resulting output voltages start-up as shown in Figure 3.

The soft-start function controls the output voltage rate of rise to limit the current surge at start-up. The soft-start interval and the surge current are programmed by the soft-start capacitor, C_{SS}. Programming a faster soft-start interval increases the peak surge current. The peak surge current occurs during the initial output voltage rise to 70% of the set value. Using the recommended 0.1µF soft start capacitor insures all output voltages ramp up to their set values within 10ms of the input voltages reaching POR levels.

Shutdown

Neither PWM output switches until the soft-start voltage (V_{SS}) exceeds the oscillator's valley voltage. Additionally, the reference on each linear's amplifier is clamped to the soft-start voltage. Holding the SS pin low (with an open drain or open collector signal) turns off all four regulators.

Layout Considerations

MOSFETs switch very fast and efficiently. The speed with which the current transitions from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. The voltage spikes can degrade efficiency, radiate noise into the circuit, and lead to device over-voltage stress. Careful component layout and printed circuit design minimizes the voltage spikes in the converter. Consider, as an example, the turn-off transition of the upper MOSFET. Prior to turn-off, the upper MOSFET was carrying the full load current. During the turn-off, current stops flowing in the upper MOSFET and is picked up by the lower MOSFET or Schottky diode. Any inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selection, tight layout of the critical components, and short, wide circuit traces minimize the magnitude of voltage spikes.

There are two sets of critical components in a DC-DC converter using a HIP6020A controller. The switching power components are the most critical because they switch large amounts of energy, and as such, they tend to generate equally large amounts of noise. The critical small signal components are those connected to sensitive nodes or those supplying critical bypass current.

The power components and the controller IC should be placed first. Locate the input capacitors, especially the high-frequency ceramic de-coupling capacitors, close to the power switches. Locate the output inductor and output capacitors between the MOSFETs and the load. Locate the PWM controller close to the MOSFETs.

The critical small signal components include the bypass capacitor for VCC and the soft-start capacitor, C_{SS}. Locate these components close to their connecting pins on the control IC. Minimize any leakage current paths from SS node, since the internal current source is only 28µA.

A multi-layer printed circuit board is recommended. Figure 7 shows the connections of the critical components in the converter. Note that the capacitors C_{IN} and C_{OUT} each could represent numerous physical capacitors. Dedicate one solid layer for a ground plane and make all critical component ground connections with vias to this layer. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the PHASE nodes, but do not unnecessarily oversize these particular islands. Since the PHASE nodes are subjected to very high dV/dt voltages, the stray capacitor formed between these islands and the surrounding circuitry will tend to couple switching noise. Use the remaining printed circuit layers for small signal wiring. The wiring traces from the control IC to the MOSFET gate and source should be sized to carry 2A peak currents.

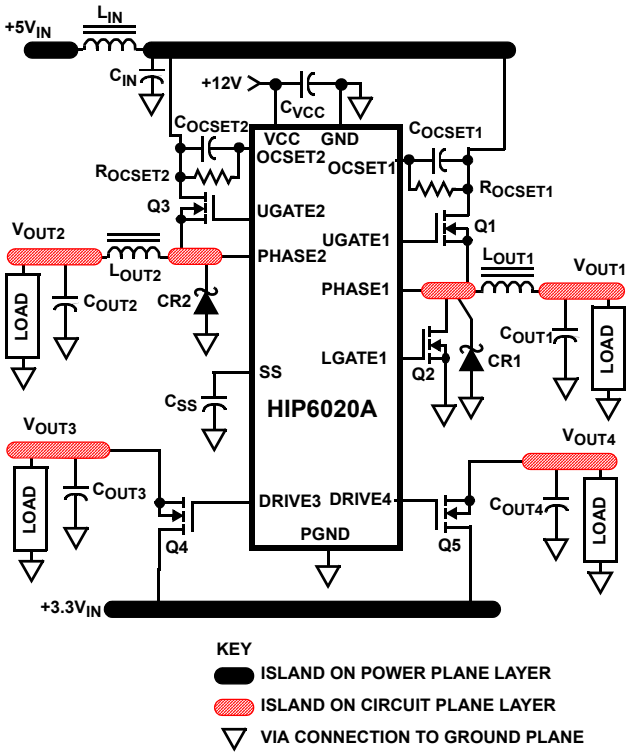


FIGURE 7. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

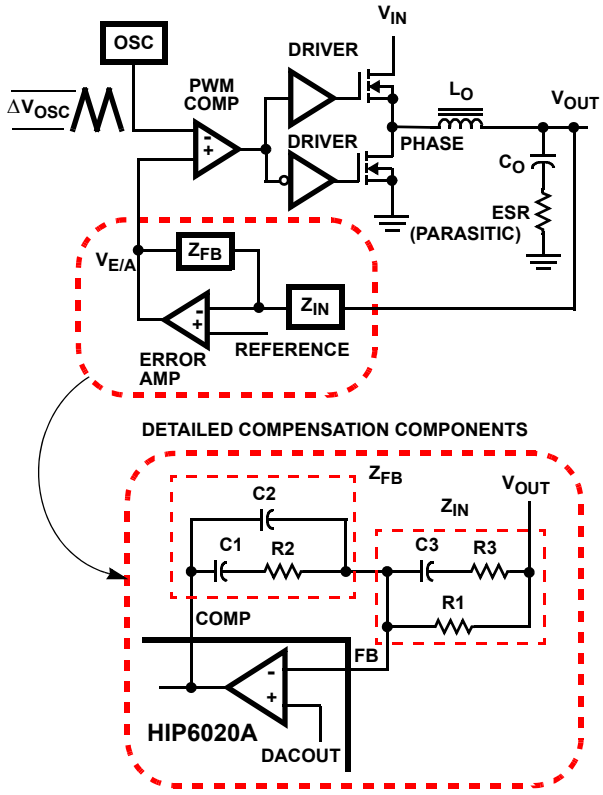


FIGURE 8. VOLTAGE-MODE BUCK CONVERTER COMPENSATION DESIGN

PWM1 Controller Feedback Compensation

Both PWM controllers use voltage-mode control for output regulation. This section highlights the design consideration for a voltage-mode controller requiring external compensation. Apply these methods and considerations only to the synchronous PWM controller. The considerations for the standard PWM controller are presented separately.

Figure 11 highlights the voltage-mode control loop for a synchronous-rectified buck converter. The output voltage (V_{OUT}) is regulated to the Reference voltage level. The reference voltage level is the DAC output voltage (DACOUT) for PWM1. The error amplifier output ($V_{E/A}$) is compared with the oscillator (OSC) triangular wave to provide a pulse-width modulated wave with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter (L_O and C_O).

The modulator transfer function is the small-signal transfer function of $V_{OUT}/V_{E/A}$. This function is dominated by a DC Gain, given by V_{IN}/V_{OSC}, and shaped by the output filter, with a double pole break frequency at F_{LC} and a zero at F_{ESR}.

Modulator Break Frequency Equations

$$F_{LC} = \frac{1}{2\pi \times \sqrt{L_O \times C_O}} \qquad F_{ESR} = \frac{1}{2\pi \times ESR \times C_O}$$

The compensation network consists of the error amplifier (internal to the HIP6020A) and the impedance networks Z_{IN} and Z_{FB}. The goal of the compensation network is to provide a closed loop transfer function with high 0dB crossing frequency (f_{0dB}) and adequate phase margin. Phase margin is the difference between the closed loop phase at f_{0dB} and 180 degrees. The equations below relate the compensation network's poles, zeros and gain to the components (R1, R2, R3, C1, C2, and C3) in Figure 8. Use these guidelines for locating the poles and zeros of the compensation network:

1. Pick Gain (R2/R1) for desired converter bandwidth
2. Place 1ST Zero Below Filter's Double Pole (~75% F_{LC})
3. Place 2ND Zero at Filter's Double Pole
4. Place 1ST Pole at the ESR Zero
5. Place 2ND Pole at Half the Switching Frequency
6. Check Gain against Error Amplifier's Open-Loop Gain
7. Estimate Phase Margin - Repeat if Necessary

Compensation Break Frequency Equations

$$F_{Z1} = \frac{1}{2\pi \times R2 \times C1} \qquad F_{P1} = \frac{1}{2\pi \times R_2 \times \left(\frac{C1 \times C2}{C1 + C2}\right)}$$

$$F_{Z2} = \frac{1}{2\pi \times (R1 + R3) \times C3} \qquad F_{P2} = \frac{1}{2\pi \times R3 \times C3}$$

Figure 9 shows an asymptotic plot of the DC-DC converter's gain vs. frequency. The actual Modulator Gain has a high gain peak dependent on the quality factor (Q) of the output filter, which is not shown in Figure 9. Using the above guidelines should yield a Compensation Gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at F_{P2} with the capabilities of the error

amplifier. The Closed Loop Gain is constructed on the log-log graph of Figure 9 by adding the Modulator Gain (in dB) to the Compensation Gain (in dB). This is equivalent to multiplying the modulator transfer function to the compensation transfer function and plotting the gain.

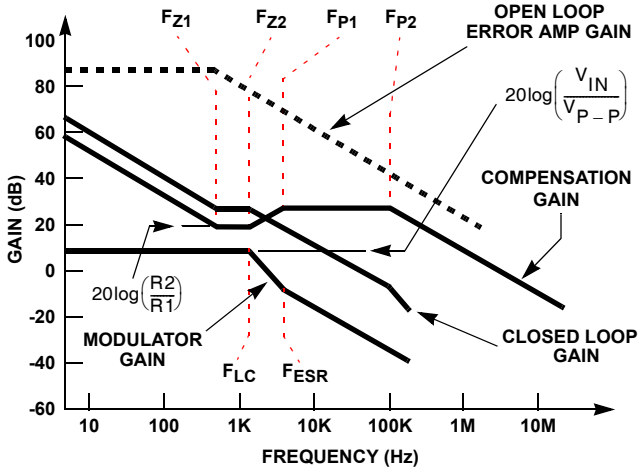


FIGURE 9. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN

The compensation gain uses external impedance networks Z_{FB} and Z_{IN} to provide a stable, high bandwidth (BW) overall loop. A stable control loop has a gain crossing with -20dB/decade slope and a phase margin greater than 45 degrees. Include worst case component variations when determining phase margin.

PWM2 Controller Feedback Compensation

To reduce the number of external small-signal components required by a typical application, the standard PWM controller is internally stabilized. The only stability criteria that needs to be met relates the minimum value of the output inductor to the equivalent ESR of the output capacitor bank, as shown in the following equation:

$$L_{OUT(MIN)} = \frac{ESR_{OUT} \times 10^{1.75}}{2 \times \pi \times BW}$$

where

$L_{OUT(MIN)}$ - minimum output inductor value at full output current

ESR_{OUT} - equivalent ESR of the output capacitor bank

BW - desired converter bandwidth (not to exceed 0.25 to 0.30 of the switching frequency)

The design procedure for this output should follow the following steps:

1. Choose number and type of output capacitors to meet the output transient requirements based on the dynamic loading characteristics of the output.
2. Determine the equivalent ESR of the output capacitor bank and calculate minimum output inductor value.
3. Verify that chosen inductor meets this minimum value criteria (at full output load). As inductors tend to saturate as the current increases, it is recommended the chosen output inductor be no more than 30% saturated at full output load.

Oscillator Synchronization

The PWM controllers use a triangle wave for comparison with the error amplifier output to provide a pulse-width modulated signal. Should the output voltage of the two converters be programmed close to each other, then cross-talk between the converters could cause non-uniform PHASE pulse-widths and increased output voltage ripple. The HIP6020A avoids this problem by appropriately synchronizing the two converters for 1.5V AGP output voltage setting. Thus, for core output voltage settings less than 2.4V, PWM1 operates out of phase with PWM2.

Component Selection Guidelines

Output Capacitor Selection

The output capacitors for each output have unique requirements. In general the output capacitors should be selected to meet the dynamic regulation requirements. Additionally, the PWM converters require an output capacitor to filter the current ripple. The load transient for the microprocessor core requires high quality capacitors to supply the high slew rate (di/dt) current demands.

PWM Output Capacitors

Modern microprocessors produce transient load rates above 1A/ns. High frequency capacitors initially supply the transient current and slow the load rate-of-change seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (effective series resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR determines the output ripple voltage and the initial voltage drop following a high slew-rate transient's edge. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the equivalent series inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Linear Output Capacitors

The output capacitors for the linear regulators provide dynamic load current. Thus capacitors C_{OUT3} and C_{OUT4} should be selected for transient load regulation.

PWM Output Inductor Selection

Each PWM converter requires an output inductor. The output inductor is selected to meet the output voltage ripple requirements and sets the converter's response time to a load transient. Additionally, PWM2 output inductor has to meet the minimum value criteria for loop stability as described in paragraph '**PWM2 Controller Feedback Compensation**'. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current. The ripple voltage and current are approximated by the following equations:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{F_S \times L} \times \frac{V_{OUT}}{V_{IN}} \qquad \Delta V_{OUT} = \Delta I \times ESR$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance values increase the converter's response time to a load transient.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the HIP6020A will provide either 0% or 100% duty cycle in response to a load transient. The response time is the time interval required to slew the inductor current from an initial current value to the post-transient current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitor(s). Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. The following equations give the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L_O \times I_{TRAN}}{V_{IN} - V_{OUT}} \qquad t_{FALL} = \frac{L_O \times I_{TRAN}}{V_{OUT}}$$

where: I_{TRAN} is the transient load current step, t_{RISE} is the response time to the application of load, and t_{FALL} is the response time to the removal of load. Be sure to check both of these equations at the minimum and maximum output levels for the worst case response time.

Input Capacitor Selection

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select bulk input capacitors with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage. The RMS current rating requirement for the input capacitors of a buck regulator is approximately 1/2 of the summation of the DC output load current.

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use ceramic capacitance for the high frequency decoupling and bulk capacitors to supply the RMS current. Small ceramic capacitors can be placed very close to the upper MOSFET to suppress the voltage induced in the parasitic circuit impedances.

For a through-hole design, several electrolytic capacitors (Panasonic HFQ series or Nichicon PL series or Sanyo MV-GX or equivalent) may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge current at power-up. The TPS series available from AVX, and the 593D series from Sprague are both surge current tested.

MOSFET Selection/Considerations

The HIP6020A requires 5 external transistors. Three N-Channel MOSFETs are employed by the PWM converters. The GTL and memory linear controllers can each drive a MOSFET or a NPN bipolar as a pass transistor. All these transistors should be selected based upon $r_{DS(ON)}$, current gain, saturation voltages, gate supply requirements, and thermal management considerations.

PWM1 MOSFET Selection and Considerations

In high-current PWM applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components; conduction loss and switching loss. These losses are distributed between the upper and lower MOSFETs according to the duty factor. The conduction losses are the main component of power dissipation for the lower MOSFETs. Only the upper MOSFET has significant switching losses, since the lower device turns on and off into near zero voltage.

The equations presented assume linear voltage-current transitions and do not model power loss due to the reverse recovery of the lower MOSFET's body diode. The gate charge losses are dissipated by the HIP6020A and don't heat the MOSFETs. However, large gate-charge increases the switching time, t_{SW}, which increases the upper MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

$$P_{UPPER} = \frac{I_O^2 \times r_{DS(ON)} \times V_{OUT}}{V_{IN}} + \frac{I_O \times V_{IN} \times t_{SW} \times F_S}{2}$$

$$P_{LOWER} = \frac{I_O^2 \times r_{DS(ON)} \times (V_{IN} - V_{OUT})}{V_{IN}}$$

The $r_{DS(ON)}$ is different for the two equations above even if the same device is used for both. This is because the gate drive applied to the upper MOSFET is different than the lower MOSFET. Figure 10 shows the gate drive where the upper MOSFET's gate-to-source voltage is approximately V_{CC} less the input supply. For +5V main power and +12VDC for the bias, the gate-to-source voltage of Q1 is 7V. The lower gate drive voltage is +12VDC. A logic-level MOSFET is a good choice for Q1 and a logic-level MOSFET can be used for Q2 if its absolute gate-to-source voltage rating exceeds the maximum voltage applied to V_{CC}.

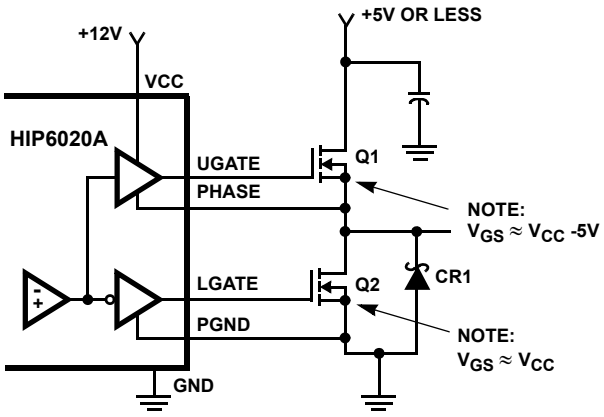


FIGURE 10. UPPER GATE DRIVE - DIRECT V_{CC} DRIVE

Rectifier CR1 is a clamp that catches the negative inductor swing during the dead time between the turn off of the lower MOSFET and the turn on of the upper MOSFET. The diode must be a Schottky type to prevent the lossy parasitic MOSFET body diode from conducting. It is acceptable to omit the diode and let the body diode of the lower MOSFET clamp the negative inductor swing, but efficiency could drop, in some cases, one or two percent as a result. The diode's rated reverse breakdown voltage must be greater than the maximum input voltage.

PWM2 MOSFET and Schottky Selection

The power dissipation in PWM2 converter is similar to PWM1 except that the power losses of the lower device are taking place in a Schottky instead of a MOSFET. The power losses of PWM2 converter are distributed between the upper MOSFET and the Schottky. The following equations describe an approximation of this distribution and assume a linear voltage-current switching transitions.

$$P_{MOS} = \frac{I_O^2 \times r_{DS(ON)} \times V_{OUT}}{V_{IN}} + \frac{I_O \times V_{IN} \times t_{SW} \times F_S}{2}$$

$$P_{SCH} = \frac{I_O \times V_f \times (V_{IN} - V_{OUT})}{V_{IN}}$$

For the fully on option (SELECT pin high) selection of the MOSFET is based on the voltage budget available to this regulator. Since the MOSFET is operated as a switch, its own $r_{DS(ON)}$ is bound by the maximum voltage drop allowable across it at the maximum output current.

Where

$$r_{DS(ON)max} = \frac{V_{IN} - (DCR \cdot I_{OUT})}{I_{OUT}}$$

$r_{DS(ON)max}$ - maximum allowed MOSFET rDS(ON)
DCR - output inductor DC resistance

In applications where both output settings could be engaged (both 1.5V and fully on MOSFET) it is recommended the MOSFET meets criteria outlined for the PWM operation as well as the fully on operation.

Linear Controllers Transistor Selection

The HIP6020A linear controllers are compatible with both NPN bipolar as well as N-Channel MOSFET transistors. The main criteria for selection of pass transistors for the linear regulators is package selection for efficient removal of heat. The power dissipated in a linear regulator is

$$P_{LINEAR} = I_O \times (V_{IN} - V_{OUT})$$

Select a package and heatsink that maintains the junction temperature below the maximum desired temperature with the maximum expected ambient temperature.

When selecting bipolar NPN transistors for use with the linear controllers, insure the current gain at the given operating V_{CE} is sufficiently large to provide the desired output load current when the base is fed with the minimum driver output current.

HIP6020A DC-DC Converter Application Circuit

Figure 11 shows an application circuit of a power supply for a microprocessor computer system. The power supply provides the microprocessor core voltage (V_{OUT1}), the AGP bus voltage (V_{OUT2}), the GTL bus voltage (V_{OUT3}), and the memory voltage (V_{OUT4}) from +3.3V, +5VDC, and +12VDC.

For detailed information on a very similar circuit employing an HIP6020, including a Bill-of-Materials and circuit board description, see Application Note AN9836. Also see Intersil web page (www.intersil.com).

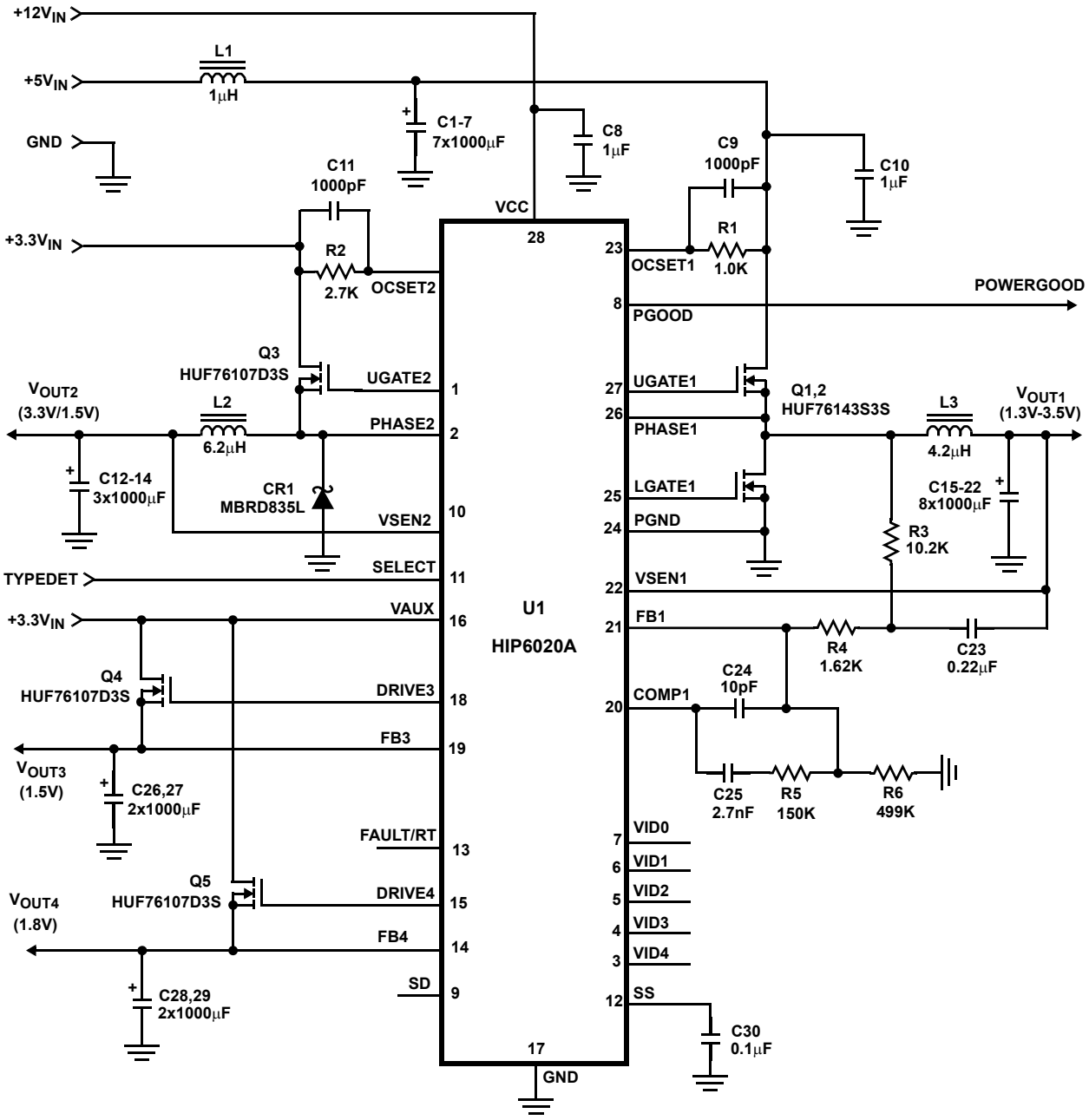
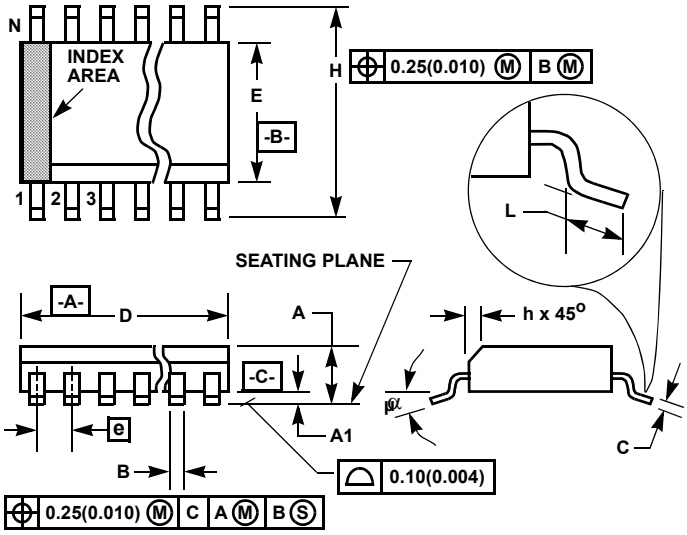


FIGURE 11. POWER SUPPLY APPLICATION CIRCUIT FOR A MICROPROCESSOR COMPUTER SYSTEM

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M28.3 (JEDEC MS-013-AE ISSUE C)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0°	8°	0°	8°	-

Rev. 0 12/93