

MC74HCT04A

Hex Inverter

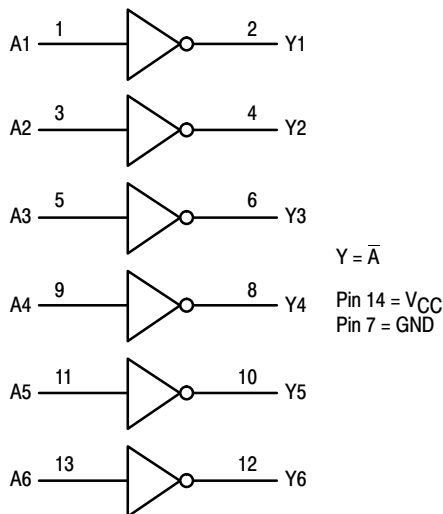
With LSTTL-Compatible Inputs High-Performance Silicon-Gate CMOS

The MC74HCT04A may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

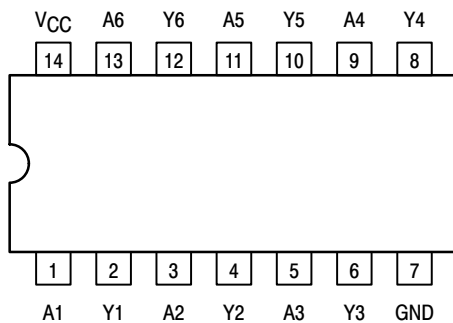
The HCT04A is identical in pinout to the LS04.

- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5V
- Low Input Current: 1µA
- In Compliance With the JEDEC Standard No. 7A Requirements
- Chip Complexity: 48 FETs or 12 Equivalent Gates

LOGIC DIAGRAM



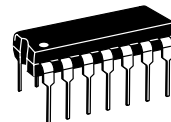
Pinout: 14-Lead Packages (Top View)



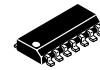
ON Semiconductor

<http://onsemi.com>

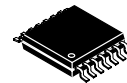
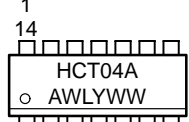
MARKING DIAGRAMS



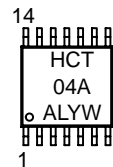
PDIP-14
N SUFFIX
CASE 646



SOIC-14
D SUFFIX
CASE 751A



TSSOP-14
DT SUFFIX
CASE 948G



A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

FUNCTION TABLE

Inputs	Outputs
A	Y
L	H
H	L

ORDERING INFORMATION

Device	Package	Shipping
MC74HCT04AN	PDIP-14	2000 / Box
MC74HCT04AD	SOIC-14	55 / Rail
MC74HCT04ADR2	SOIC-14	2500 / Reel
MC74HCT04ADT	TSSOP-14	96 / Rail
MC74HCT04ADTR2	TSSOP-14	2500 / Reel

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	± 20	mA
I _{out}	DC Output Current, per Pin	± 25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	± 50	mA
PD	Power Dissipation in Still Air	750	mW
	Plastic DIP†	500	
	SOIC Package†	450	
T _{stg}	Storage Temperature Range	- 65 to + 150	C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package	260	C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: - 10 mW/ C from 65 to 125 C
SOIC Package: - 7 mW/ C from 65 to 125 C
TSSOP Package: - 6.1 mW/ C from 65 to 125 C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature Range, All Package Types	- 55	+ 125	C
t _r , t _f	Input Rise/Fall Time (Figure 1)	0	500	ns

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DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V _{CC} V	Guaranteed Limit			Unit
				-55 to 25°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1V I _{out} ≤ 20μA	4.5	2.0	2.0	2.0	V
			5.5	2.0	2.0	2.0	
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = V _{CC} - 0.1V I _{out} ≤ 20μA	4.5	0.8	0.8	0.8	V
			5.5	0.8	0.8	0.8	
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IL} I _{out} ≤ 20μA	4.5	4.4	4.4	4.4	V
		V _{in} = V _{IL} I _{out} ≤ 4.0mA	5.5	5.4	5.4	5.4	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} I _{out} ≤ 20μA	4.5	0.1	0.1	0.1	V
		V _{in} = V _{IH} I _{out} ≤ 4.0mA	5.5	0.1	0.1	0.1	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	5.5	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0μA	5.5	1	10	40	μA
ΔI _{CC}	Additional Quiescent Supply Current	V _{in} = 2.4V, Any One Input V _{in} = V _{CC} or GND, Other Inputs I _{out} = 0μA	5.5	≥ -55°C	25 to 125°C		mA
				2.9	2.4		

1. Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

2. Total Supply Current = I_{CC} + ΣΔI_{CC}.

AC CHARACTERISTICS (V_{CC} = 5.0V ±10%, C_L = 50pF, Input t_r = t_f = 6ns)

Symbol	Parameter	Guaranteed Limit			Unit
		-55 to 25°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	15	19	22	ns
		17	21	26	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	15	19	22	ns
C _{in}	Maximum Input Capacitance	10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

C _{PD}	Power Dissipation Capacitance (Per Inverter)*	Typical @ 25°C, V _{CC} = 5.0 V		pF
		22		

* Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}. For load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

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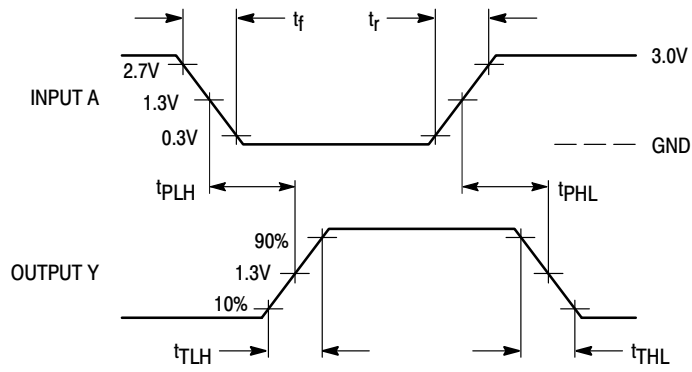
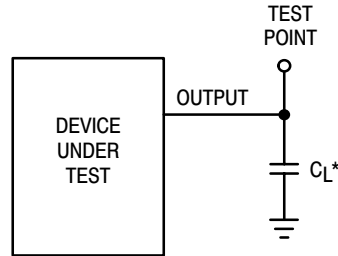


Figure 1. Switching Waveforms



*Includes all probe and jig capacitance

Figure 2. Test Circuit

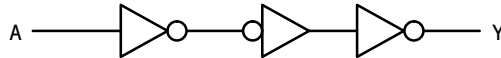


Figure 3. Expanded Logic Diagram
(1/6 of the Device Shown)