DRV8704 52-V Dual H-Bridge PWM Gate Driver

1 Features

- Pulse Width Modulation (PWM) Motor Driver
  - Drives External N-Channel MOSFETs
  - PWM Control Interface for Dual DC Motors
  - Supports 100% PWM Duty Cycle
- 8-V to 52-V Operating Supply Voltage Range
- Adjustable Gate Drive (4 Levels)
  - 50-mA to 200-mA Source Current
  - 100-mA to 400-mA Sink Current
- Integrated PWM Current Regulation
- Flexible Decay Modes
  - Automatic Mixed Decay Mode
  - Slow Decay
  - Fast Decay
  - Mixed Decay (Adjustable Percent Fast)
- Highly Configurable SPI
- Torque DAC to Digitally Scale Current
- Low-Current Sleep Mode (65 µA)
- 5-V, 10-mA LDO Regulator
- Thermally-Enhanced Surface-Mount Package
  - 38-Pin HTSSOP (PowerPAD)

- Protection Features
  - VM Undervoltage Lockout (UVLO)
  - Gate Driver Fault (PDF)
  - Overcurrent Protection (OCP)
  - Thermal Shutdown (TSD)
  - Fault Condition Indication Pin (nFAULT)
  - Fault Diagnostics through SPI

2 Applications

- Automatic Teller and Money Handling Machines
- Office Automation Machines
- Factory Automation and Robotics
- Textile Machines

3 Description

The DRV8704 is a dual-brushed motor controller for industrial equipment applications. The device controls external N-channel MOSFETs configured as two H-bridges.

Motor current can be accurately controlled using adaptive blanking time and various current decay modes, including an automatic mixed decay mode.

A simple PWM interface allows easy interfacing to controller circuits. A SPI serial interface is used to program the device operation. Output current (torque), gate drive settings, and decay mode are all programmable through a SPI serial interface.

Internal shutdown functions are provided for overcurrent protection, short-circuit protection, gate driver faults, undervoltage lockout (UVLO), and overtemperature. Fault conditions are indicated by a FAULTn pin, and each fault condition is reported by a dedicated bit through SPI.

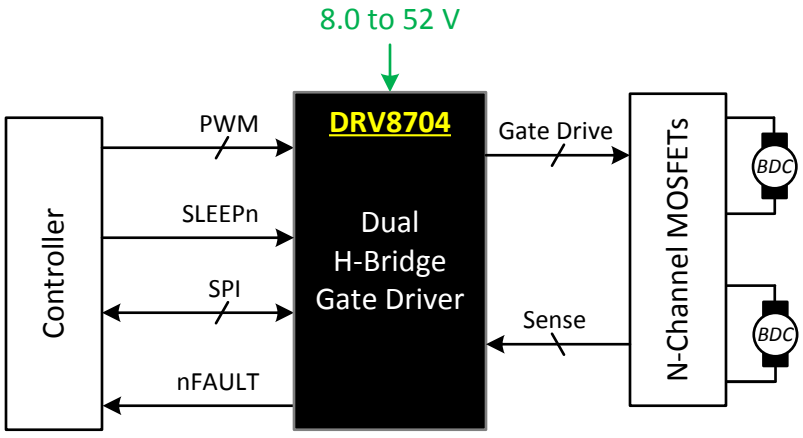
The DRV8704 is packaged in a PowerPAD™ 38-pin HTSSOP package with thermal pad (Eco-friendly: RoHS & no Sb/Br).

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8704	HTSSOP (38)	9.70 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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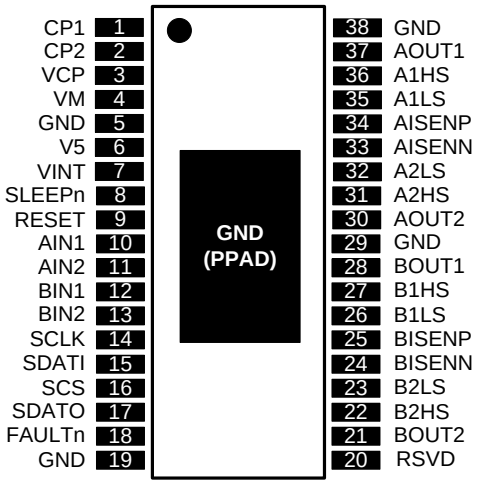
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2015	*	Initial release.

5 Pin Configuration and Functions

DCP Package
38-Pin HTSSOP
Top View



Pin Functions

PIN (1)		TYPE	DESCRIPTION	
NAME	NO.			
POWER AND GROUND				
CP1	1	IO	Charge pump flying capacitor	Connect a 0.1-µF X7R capacitor between CP1 and CP2. Voltage rating must be greater than applied VM voltage.
CP2	2	IO	Charge pump flying capacitor	
GND	5, 19, 29, 38, PPAD	—	Device ground	All pins must be connected to ground
RSVD	20	—	Reserved	Leave this pin disconnected
V5	6	O	5-V regulator output	5-V linear regulator output. Bypass to GND with a 0.1-µF 10-V X7R ceramic capacitor.
VCP	3	IO	High-side gate drive voltage	Connect a 1-µF 16-V X7R ceramic capacitor to VM
VINT	7	—	Internal logic supply voltage	Logic supply voltage. Bypass to GND with a 1-µF 6.3-V X7R ceramic capacitor.
VM	4	—	Motor power supply	Connect to motor supply voltage. Bypass to GND with a 0.1-µF ceramic capacitor plus a 100-µF electrolytic capacitor.
CONTROL				
AIN1	10	I	Bridge A IN1	Controls bridge A OUT1. Internal pulldown.
AIN2	11	I	Bridge A IN2	Controls bridge A OUT2. Internal pulldown.
BIN1	12	I	Bridge B IN1	Controls bridge B OUT1. Internal pulldown.
BIN2	13	I	Bridge B IN2	Controls bridge B OUT2. Internal pulldown.
RESET	9	I	Reset input	Active-high reset input initializes all internal logic and disables the H-bridge outputs. Internal pulldown.
SLEEPn	8	I	Sleep mode input	Logic high to enable device, logic low to enter low-power sleep mode. Internal pulldown.
SERIAL INTERFACE				
SCLK	14	I	Serial clock input	Rising edge clocks data into part for write operations. Falling edge clocks data out of part for read operations. Internal pulldown.
SCS	16	I	Serial chip select input	Active high to enable serial data transfer. Internal pulldown.
SDATI	15	I	Serial data input	Serial data input from controller. Internal pulldown.

(1) Directions: I = Input, O = Output, OZ = Tri-state output, OD = Open-drain output, IO = Input/output

Pin Functions (continued)

PIN (1)		TYPE	DESCRIPTION	
NAME	NO.			
SDATO	17	O	Serial data output	Serial data output to controller. Open-drain output requires external pull-up.
STATUS				
FAULTn	18	OD	Fault	Logic low when in fault condition. Open-drain output requires external pullup.
OUTPUT				
A1HS	36	O	Bridge A out 1 HS gate	Bridge A out 1 HS FET gate
A1LS	35	O	Bridge A out 1 LS gate	Bridge A out 1 LS FET gate
A2HS	31	O	Bridge A out 2 HS gate	Bridge A out 2 HS FET gate
A2LS	32	O	Bridge A out 2 LS gate	Bridge A out 2 LS FET gate
AISENN	33	I	Bridge A Isense – in	Ground at sense resistor for bridge A
AISENP	34	I	Bridge A Isense + in	Current sense resistor for bridge A
AOUT1	37	I	Bridge A output 1	Output node of bridge A out 1
AOUT2	30	I	Bridge A output 2	Output node of bridge A out 2
B1HS	27	O	Bridge B out 1 HS gate	Bridge B out 1 HS FET gate
B1LS	26	O	Bridge B out 1 LS gate	Bridge B out 1 LS FET gate
B2HS	22	O	Bridge B out 2 HS gate	Bridge B out 2 HS FET gate
B2LS	23	O	Bridge B out 2 LS gate	Bridge B out 2 LS FET gate
BISENN	24	I	Bridge B Isense – in	Ground at sense resistor for bridge B
BISENP	25	I	Bridge B Isense + in	Current sense resistor for bridge B
BOUT1	28	I	Bridge B output 1	Output node of bridge B out 1
BOUT2	21	I	Bridge B output 2	Output node of bridge B out 2

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range referenced with respect to GND (unless otherwise noted) (1)

	MIN	MAX	UNIT
Power supply voltage (VM)	–0.6	60	V
Charge pump voltage (CP1, CP2, VCP)	–0.6	VM + 12	V
5-V regulator voltage (V5)	–0.6	5.5	V
Internal regulator voltage (VINT)	–0.6	2.0	V
Digital pin voltage (SLEEPn, RESET, AIN1, AIN2, BIN1, BIN2, SCS, SCLK, SDATI, SDATO, FAULTn)	–0.6	5.5	V
High-side gate drive pin voltage (A1HS, A2HS, B1HS, B2HS)	–0.6	VM + 12	V
Low-side gate drive pin voltage (A1LS, A2LS, B1LS, B2LS)	–0.6	12	V
Phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	–0.6	VM	V
ISENSEx pin voltage (AISENP, AISENN, BISENP, BISENN)	–0.7	+0.7	V
Operating virtual junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
VM	Motor power supply voltage range	8	52	V
V_{IN}	Digital pin voltage range	0	5.3	V
f_{PWM}	Applied PWM signal (xINx)	0	500	kHz
I_{V5}	V5 external load current	0	10	mA
T_A	Operating ambient temperature range	–40	85	°C

6.4 Thermal Information

THERMAL METRIC (1)		DRV8704 DCP (HTSSOP) 38 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_A = 25°C, over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM)						
I_{VM}	VM operating supply current	VM = 24 V		17	22	mA
I_{VMQ}	VM sleep mode supply current	VM = 24 V, SLEEPn low		65	98	µA
INTERNAL LINEAR REGULATORS (V5, VINT)						
V5	V5 output voltage	VM ≥ 12 V, IOUT ≤ 10 mA	4.8	5	5.2	V
VINT	VINT voltage	No external load; reference only	1.7	1.8	1.9	V
LOGIC-LEVEL INPUTS (SLEEPn, AIN1, AIN2, BIN1, BIN2, RESET, SCLK, SDATI, SCS)						
V_{IL}	Input logic low voltage				0.8	V
V_{IH}	Input logic high voltage		1.5			V
V_{HYS}	Input logic hysteresis			300		mV
I_{IL}	Input logic low current	V_{IN} = 0 V	–5		5	µA
I_{IH}	Input logic high current	V_{IN} = 5 V	24	50	70	µA
OPEN DRAIN OUTPUTS (nFAULT, SDATO)						
V_{OL}	Output logic low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output logic high leakage	10kΩ pullup to 3.3 V	–1		1	µA
GATE DRIVERS						
V_{OUTH}	High-side gate drive output voltage	VM = 24 V, I_O = 100 µA		VM + 10		V
V_{OUTL}	Low-side gate drive output voltage	VM = 24 V, I_O = 100 µA		10		V
t_{DEAD}	Output dead time digital delay (dead time is enforced in analog circuits)	DTIME = 00		410		ns
		DTIME = 01		460		
		DTIME = 10		670		
		DTIME = 11		880		
$I_{OUT,SRC}$	Peak output sourcing gate drive current	IDRIVEP = 00		50		mA
		IDRIVEP = 01		100		
		IDRIVEP = 10		150		
		IDRIVEP = 11		200		
$I_{OUT,SNK}$	Peak output sinking gate drive current	IDRIVEN = 00		100		mA
		IDRIVEN = 01		150		
		IDRIVEN = 10		200		
		IDRIVEN = 11		400		
$t_{DRIVE,SRC}$	Peak current drive time for sourcing	TDRIVEP = 00		263		ns
		TDRIVEP = 01		525		
		TDRIVEP = 10		1050		
		TDRIVEP = 11		2100		
$t_{DRIVE,SNK}$	Peak current drive time for sinking	TDRIVEN = 00		263		ns
		TDRIVEN = 01		525		
		TDRIVEN = 10		1050		
		TDRIVEN = 11		2100		
CURRENT REGULATION						
t_{OFF}	PWM off time adjustment range	Set by TOFF register	0.53		134	µs
t_{BLANK}	Current sense blanking time	Set by TBLANK register	1.05		7.0	µs
A_V	Current sense amplifier gain	ISGAIN = 00		5		V/V
		ISGAIN = 01		10		
		ISGAIN = 10		20		
		ISGAIN = 11		40		

Electrical Characteristics (continued)

T_A = 25°C, over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SET}	Settling time (to ±1%)	ISGAIN = 00, ΔVIN = 400 mV		150		ns
		ISGAIN = 01, ΔVIN = 200 mV		300		
		ISGAIN = 10, ΔVIN = 100 mV		600		
		ISGAIN = 11, ΔVIN = 50 mV		1200		
V_{OFS}	Offset voltage	ISGAIN = 00, input shorted			4	mV
V_{IN}	Input differential voltage range		–600		600	mV
V_{REF}	Internal reference voltage		2.50	2.75	3.00	V
PROTECTION CIRCUITS						
V_{UVLO}	Undervoltage lockout	VIN falling; UVLO report		6.3		V
		VIN rising; UVLO recovery		7.1	8	
V_{OCP}	Overcurrent protection trip level (Voltage drop across external FET)	OCPTH = 00	160	250	320	mV
		OCPTH = 01	380	500	580	
		OCPTH = 10	620	750	880	
		OCPTH = 11	840	1000	1200	
T_{TSD} (1)	Thermal shutdown temperature	Die temperature, T_J	150	160	180	°C
T_{HYS} (1)	Thermal shutdown hysteresis	Die temperature, T_J		20		°C

(1) Not tested in production; limits are based on characterization data

6.6 SPI Timing Requirements

over operating free-air temperature range (unless otherwise noted)

NO.			MIN	MAX	UNIT
1	t_{CYC}	Clock cycle time	250		ns
2	t_{CLKH}	Clock high time	25		ns
3	t_{CLCL}	Clock low time	25		ns
4	$t_{SU(SDATI)}$	Setup time, SDATI to SCLK	5		ns
5	$t_{H(SDATI)}$	Hold time, SDATI to SCLK	1		ns
6	$t_{SU(SCS)}$	Setup time, SCS to SCLK	5		ns
7	$t_{H(SCS)}$	Hold time, SCS to SCLK	1		ns
8	$t_{L(SCS)}$	Inactive time, SCS (between writes)	100		ns
9	$t_{D(SDATO)}$	Delay time, SCLK to SDATO (during read)		10	ns
	t_{SLEEP}	Wake time (SLEEPn inactive to high-side gate drive enabled)		1	ms
	t_{RESET}	Delay from power-up or RESETn high until serial interface functional		10	µs

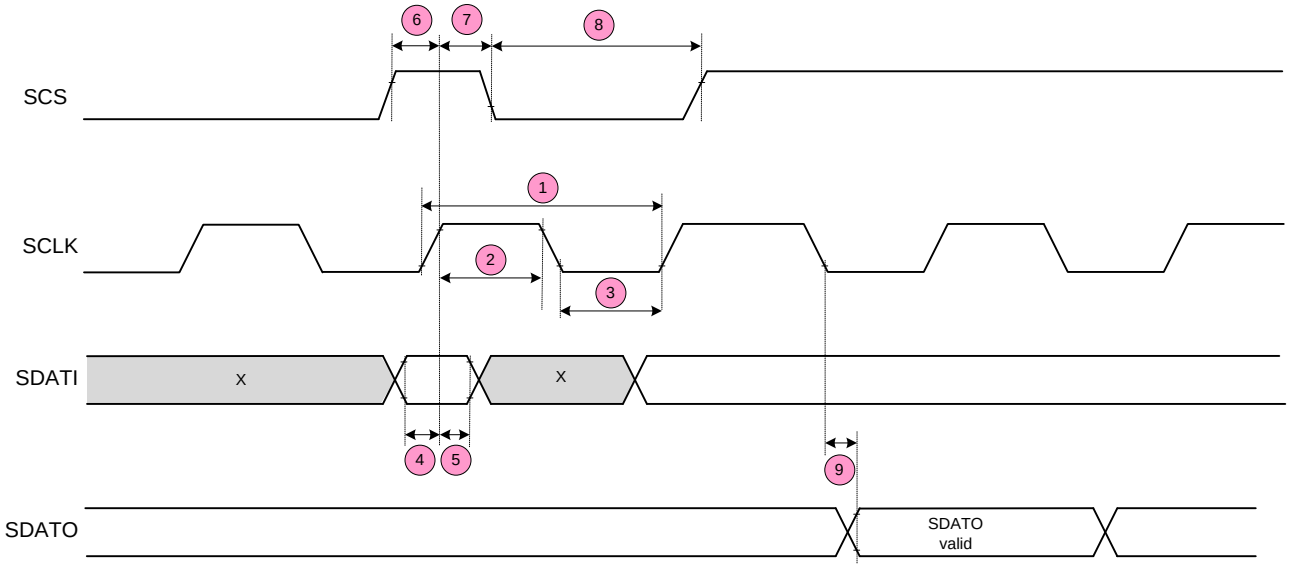


Figure 1. Timing Diagram

6.7 Typical Characteristics

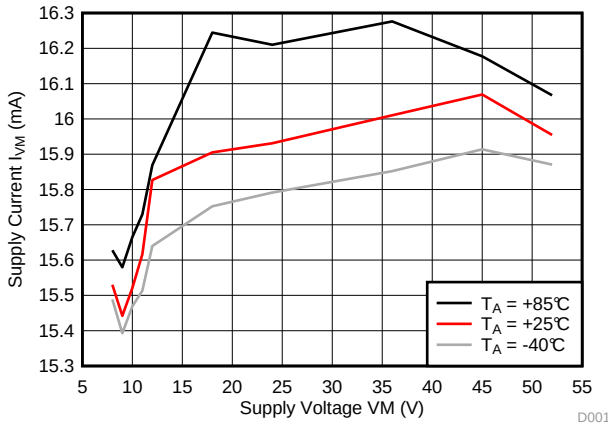


Figure 2. Supply Current over Supply Voltage

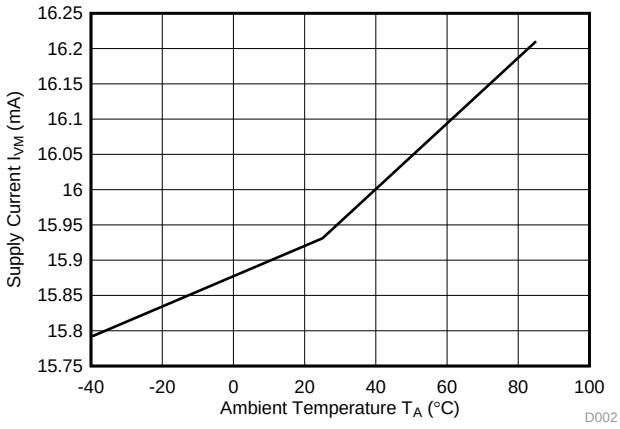


Figure 3. Supply Current over Ambient Temperature at VM = 24 V

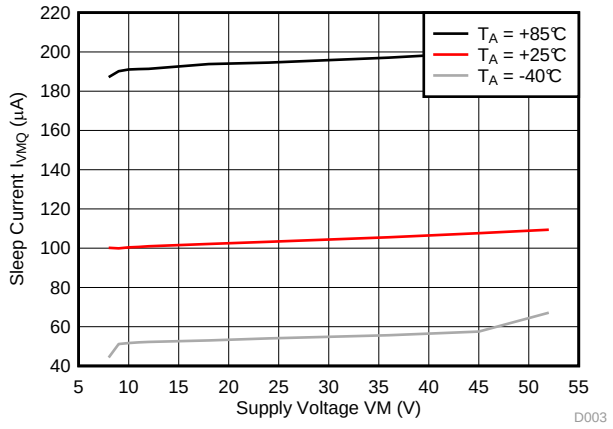


Figure 4. Sleep Current over Supply Voltage

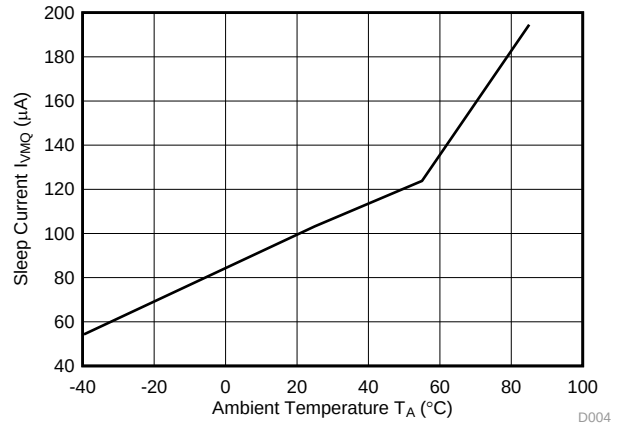


Figure 5. Sleep Current over Ambient Temperature at VM = 24 V

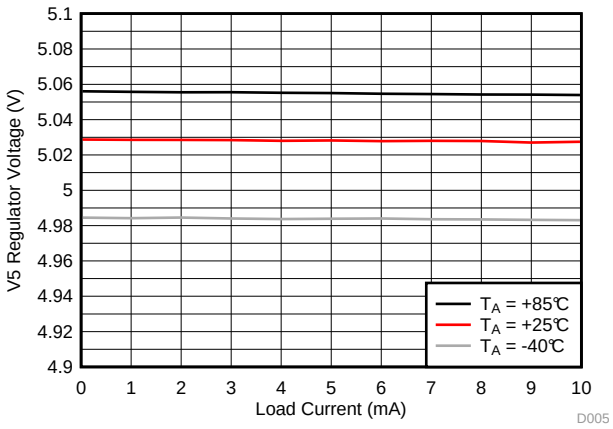


Figure 6. V5 Regulator Voltage over Output Load at VM = 12 V

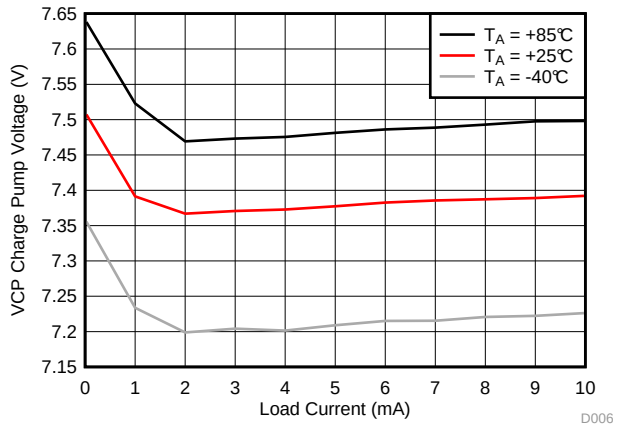


Figure 7. Charge Pump Voltage over DC Current Load at VM = 12 V

7 Detailed Description

7.1 Overview

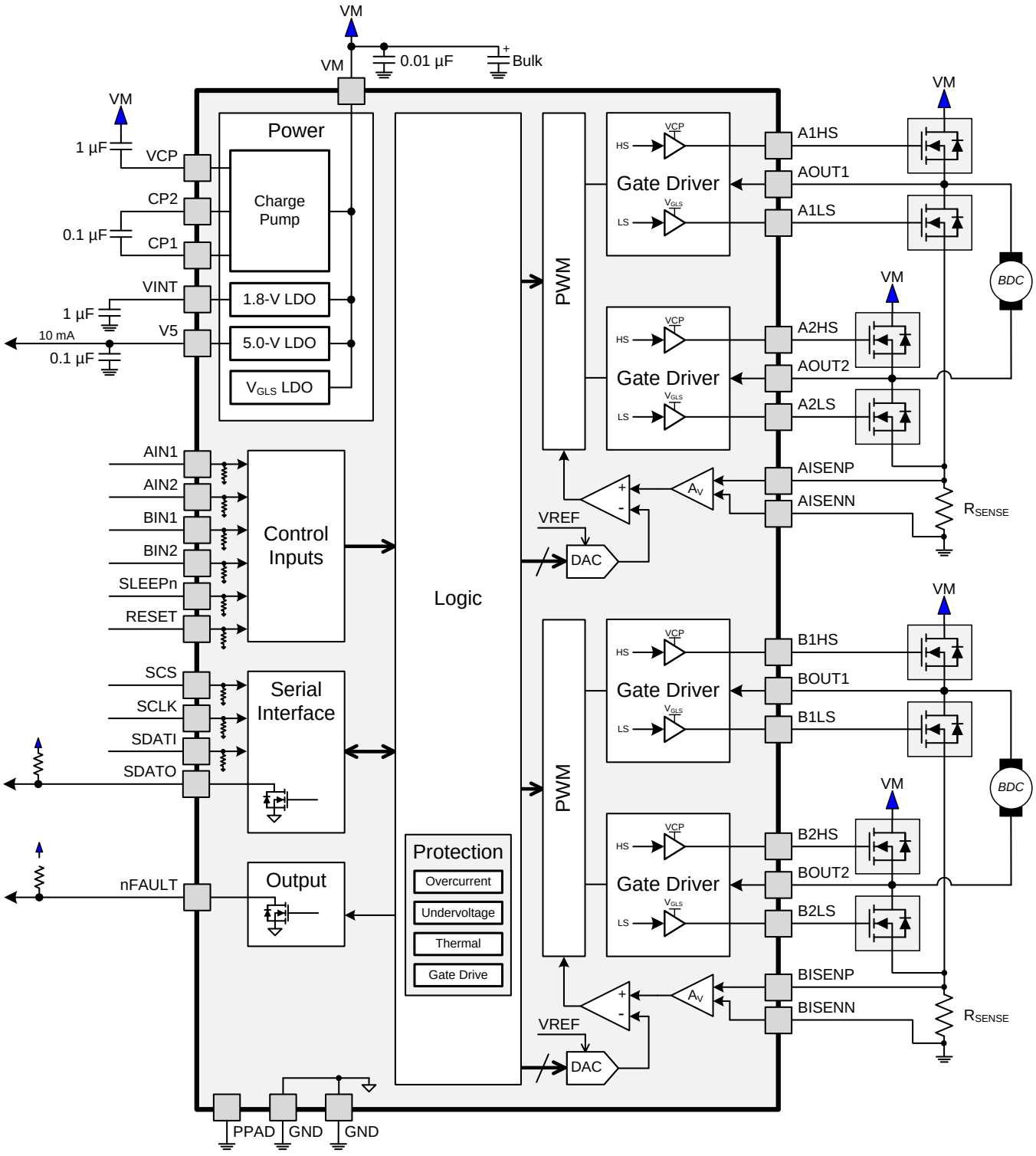
The DRV8704 is a dual-brushed motor controller that uses external N-channel MOSFETs to drive two brushed DC motors.

Motor current can be accurately controlled using adaptive blanking time and various current decay modes, including an auto-mixed decay mode.

A simple PWM interface allows easy interfacing to controller circuits. A SPI serial interface is used to program the device operation. Output current (torque), gate drive settings, and decay mode are all programmable through a SPI serial interface.

Internal shutdown functions are provided for overcurrent protection, short-circuit protection, UVLO, and overtemperature. Fault conditions are indicated by a FAULTn pin, and each fault condition is reported by a dedicated bit through SPI.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM Motor Drivers

The DRV8704 contains two H-bridge motor gate drivers with current-control PWM circuitry.

7.3.2 Direct PWM Input Mode (Dual Brushed DC Gate Driver)

In direct PWM input mode, the AIN1, AIN2, BIN1, and BIN2 directly control the state of the output drivers. This allows for driving up to two brushed DC motors. Table 1 shows the logic.

Table 1. Output Control Logic Table

SLEEPn	xIN1	xIN2	xOUT1	xOUT2	DESCRIPTION
0	X	X	Hi-Z	Hi-Z	Sleep mode; H-bridge disabled Hi-Z
1	0	0	Hi-Z	Hi-Z	Coast; H-bridge disabled Hi-Z
1	0	1	L	H	Reverse (current xOUT2 → xOUT1)
1	1	0	H	L	Forward (current xOUT1 → xOUT2)
1	1	1	L	L	Brake; low-side slow decay

In direct PWM mode, the current control circuitry is still active. The full-scale VREF is set to 2.75 V. The TORQUE register may be used to scale this value, and the ISEN sense amplifier gain may still be set using the ISGAIN bits of the CTRL register.

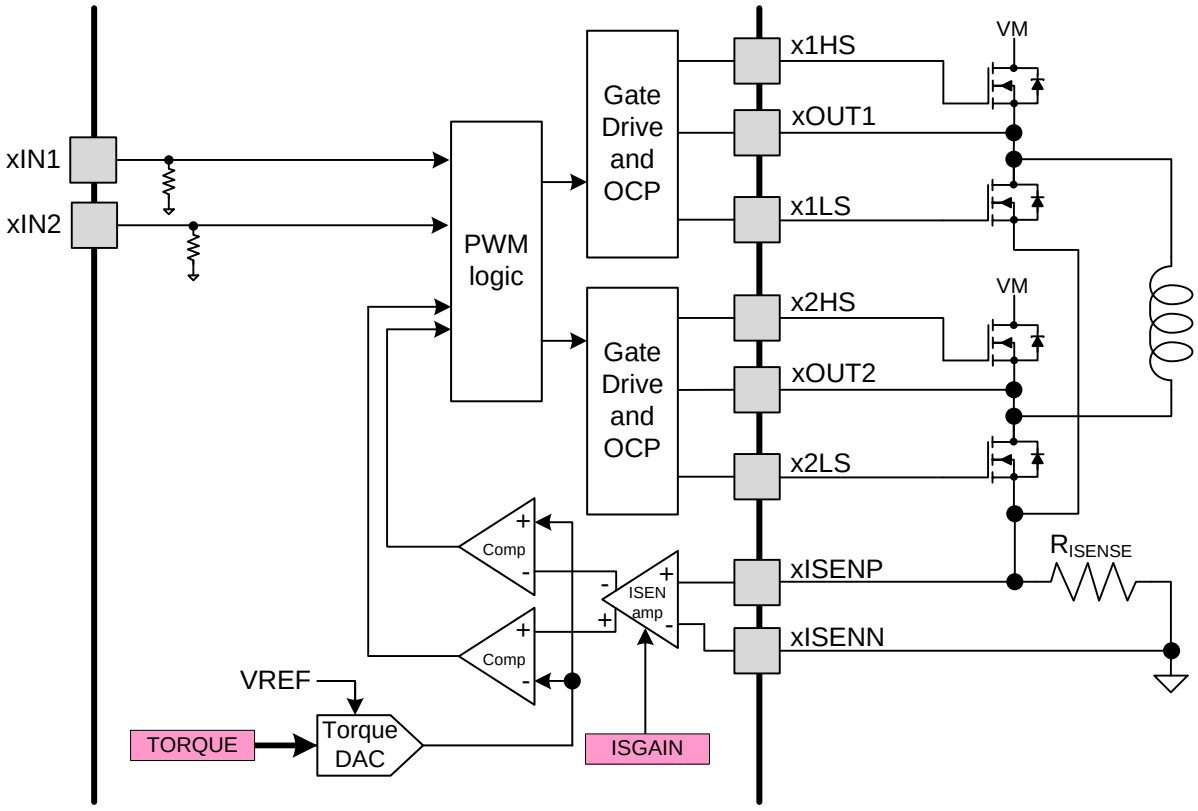


Figure 8. Motor Driver Block Diagram

7.3.3 Current Regulation

The current through the motor windings is regulated by an adjustable fixed-off-time PWM current regulation circuit. When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage and inductance of the winding and the magnitude of the back EMF present. Once the current hits the current chopping threshold, the bridge disables the current for a fixed period of time, which is programmable between 525 ns and 128 µs by writing to the TOFF bits in the OFF register. After the off time expires, the bridge is re-enabled, starting another PWM cycle.

Note that the decay mode is set by DECMOD bits in the DECAY register. Slow, fast, mixed, or auto mixed decay modes are available.

The chopping current is set by a comparator which compares the voltage across a current sense resistor connected to the xISENx pins, multiplied by the gain of the current sense amplifier, with a reference voltage. The current sense amplifier is programmable in the CTRL register.

When driving in PWM mode, the chopping current is calculated as follows:

$$I_{CHOP} = \frac{2.75\ V \times TORQUE}{256 \times ISGAIN \times R_{ISENSE}} \quad (1)$$

where

- TORQUE is the setting of the TORQUE bits
- ISGAIN is the programmed gain of the ISENSE amplifiers (5, 10, 20, or 40).

7.3.4 Decay Modes

During PWM current chopping, the H-bridge is enabled to drive current through the motor winding until the PWM current chopping threshold is reached. This is shown in the diagram below as case 1. The current flow direction shown indicates positive current flow in the step table below.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay.

In fast decay mode, once the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. If the winding current approaches zero, the bridge is disabled to prevent any reverse current flow. Fast decay mode is shown in the diagram below as case 2.

In slow decay mode, winding current is recirculated by enabling both of the low-side FETs in the bridge. This is shown as case 3 in Figure 9.

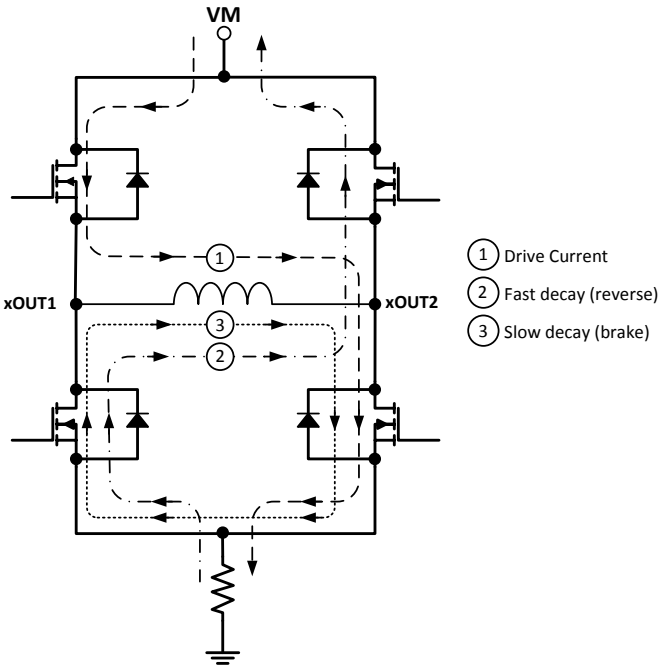


Figure 9. Decay Mode Current

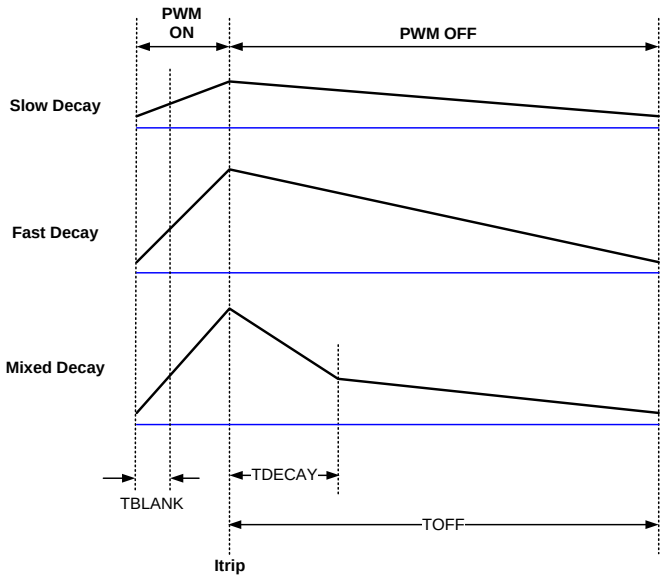


Figure 10. Decay Mode Comparison

The DRV8704 supports fast decay and slow decay modes. In addition it supports fixed mixed decay and auto mixed decay modes. Decay mode is selected by the DECMOD bits in the DECAY register.

Mixed decay mode begins as fast decay, but after a programmable period of time (set by the TDECAY bits in the DECAY register) switches to slow decay mode for the remainder of the fixed off time.

Auto mixed decay mode samples the current level at the end of the blanking time, and if the current is above the Itrip threshold, immediately changes the H-bridge to fast decay. During fast decay, the (negative) current is monitored, and when it falls below the Itrip threshold (and another blanking time has passed), the bridge is switched to slow decay. Once the fixed off time expires, a new cycle is started.

If the bridge is turned on and at the end of t_{BLANK} the current is below the Itrip threshold, the bridge remains on until the current reaches Itrip. Then slow decay is entered for the fixed off time, and a new cycle begins.

Refer to Figure 11.

The upper waveform shows the behavior if I < Itrip at the end of t_{BLANK}. This is a stable, slow decay mode of operation.

The lower waveform shows what happens when I > Itrip at the end of t_{BLANK}. Note that (at slow motor speeds, where back EMF is not significant), the current increase during the ON phase is the same magnitude as the current decrease in fast decay, since both times are controlled by t_{BLANK}, and the rate of change is the same (full VM is applied to the load inductance in both cases, but in opposite directions). In this case, the current will gradually be driven down until the peak current is just hitting Itrip at the end of the blanking time, after which some cycles will be slow decay, and some will be mixed decay.

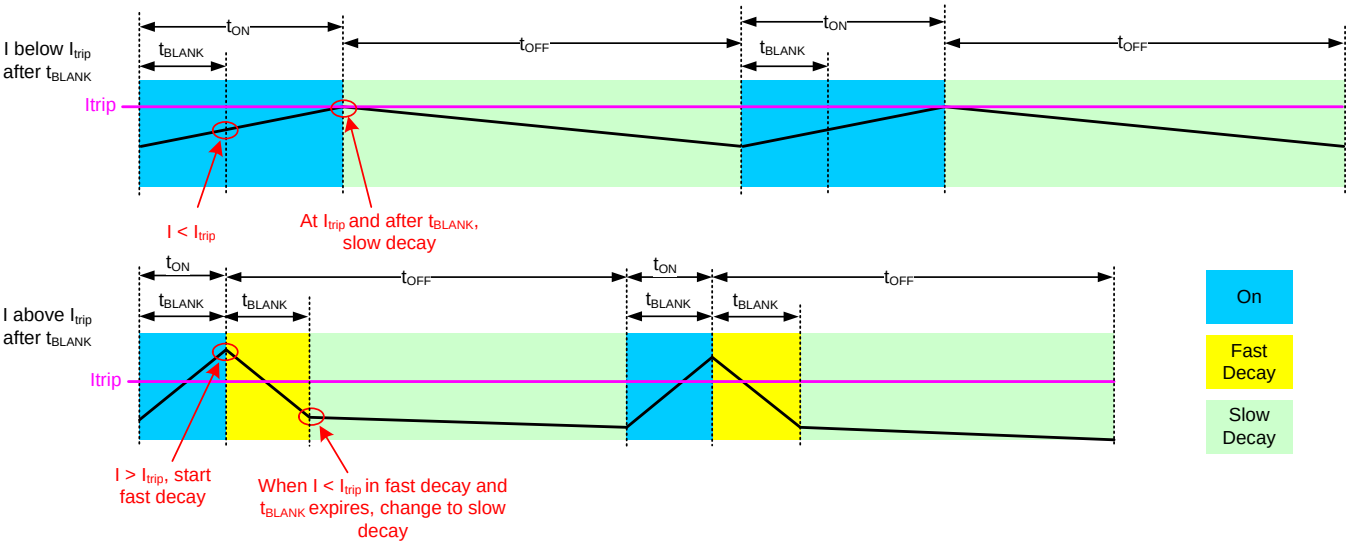


Figure 11. Auto Mixed Decay

To accurately detect zero current, an internal offset has been intentionally placed in the zero current detection circuit. If an external filter is placed on the current sense resistor to the xISENN and xISENP pins, symmetry must be maintained. This means that any resistance between the bottom of the R_{ISENSE} resistor and xISENN must be matched by the same resistor value (1% tolerance) between the top of the R_{ISENSE} resistor and xISENP. Ensure a maximum resistance of 500 Ω. The capacitor value should be chosen such that the RC time constant is between 50 and 60 ns. Any external filtering on these pins is optional and not required for operation.

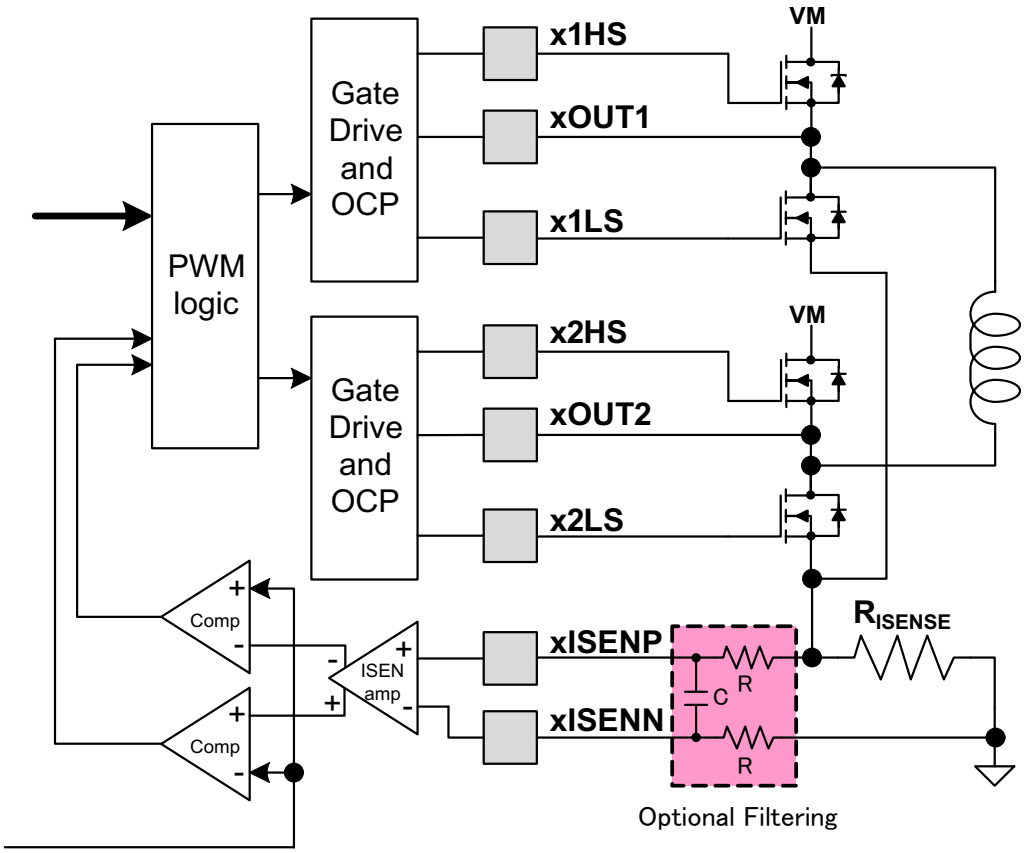


Figure 12. Optional Filtering for Sense Amplifiers

7.3.5 Blanking Time

After the current is enabled in an H-bridge, the voltage on the ISEN pin is ignored for a period of time before enabling the current sense circuitry. This blanking time is adjustable from 500 ns to 5.14 µs, in 20-ns increments, by setting the TBLANK bits in the BLANK register. Note that the blanking time also sets the minimum drive time of the PWM.

The same blanking time is applied to the fast decay period in auto mixed decay mode. The PWM will ignore any transitions on Itrip after entering fast decay mode, until the blanking time has expired.

7.3.6 Gate Drivers

An internal charge pump circuit and pre-drivers inside the DRV8704 directly drive N-channel MOSFETs, which drive the motor current.

The peak drive current of the pre-drivers is adjustable by setting the bits in the DRIVE register. Peak source currents may be set to 50 mA, 100 mA, 150 mA, or 200 mA. The peak sink current is approximately 2× the peak source current. Adjusting the peak current will change the output slew rate, which also depends on the FET input capacitance and gate charge.

When changing the state of the output, the peak current is applied for a short period of time (t_{DRIVE}), to charge the gate capacitance. After this time, a weak current source is used to keep the gate at the desired state. When selecting the gate drive strength for a given external FET, the selected current must be high enough to fully charge and discharge the gate during the time when driven at full current, or excessive power will be dissipated in the FET.

During high-side turn-on, the low-side gate is pulled low. This prevents the gate-drain capacitance of the low-side FET from inducing turn-on.

The pre-driver circuits include enforcement of a dead time in analog circuitry, which prevents the high-side and low-side FETs from conducting at the same time. Additional dead time is added with digital delays. This delay can be selected by setting the DTIME bits in the CTRL register.

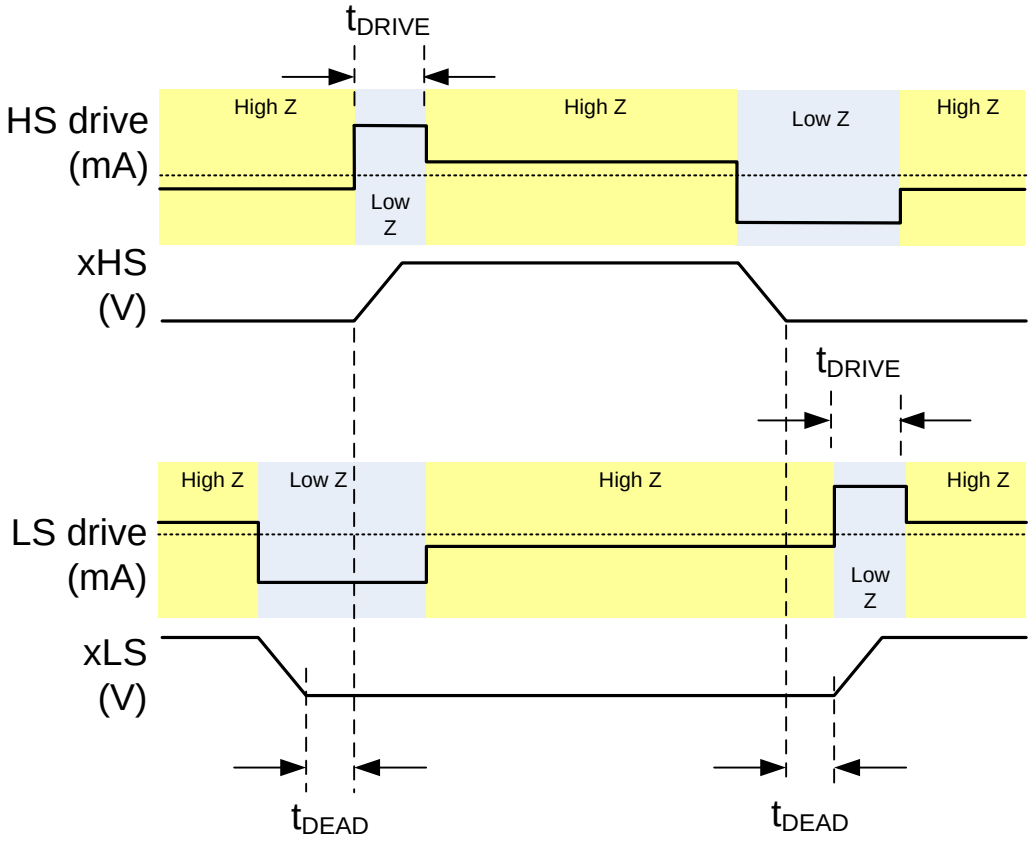


Figure 13. Gate Driver

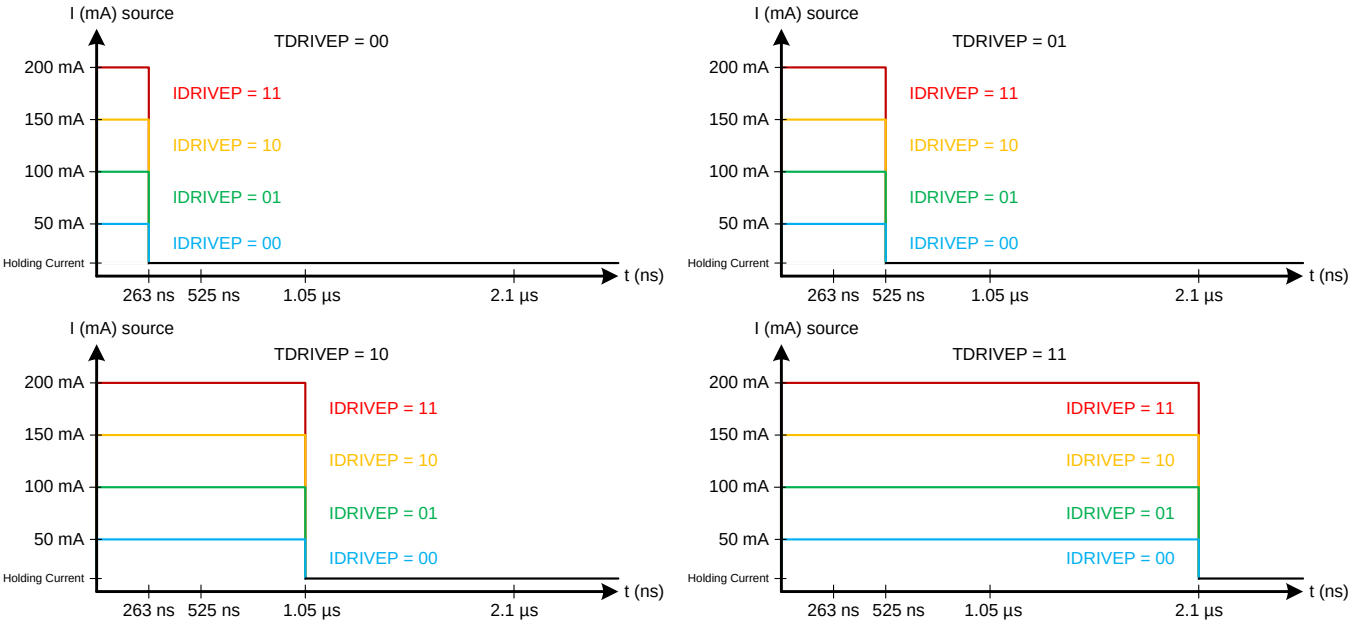


Figure 14. Gate Driver Source Capability

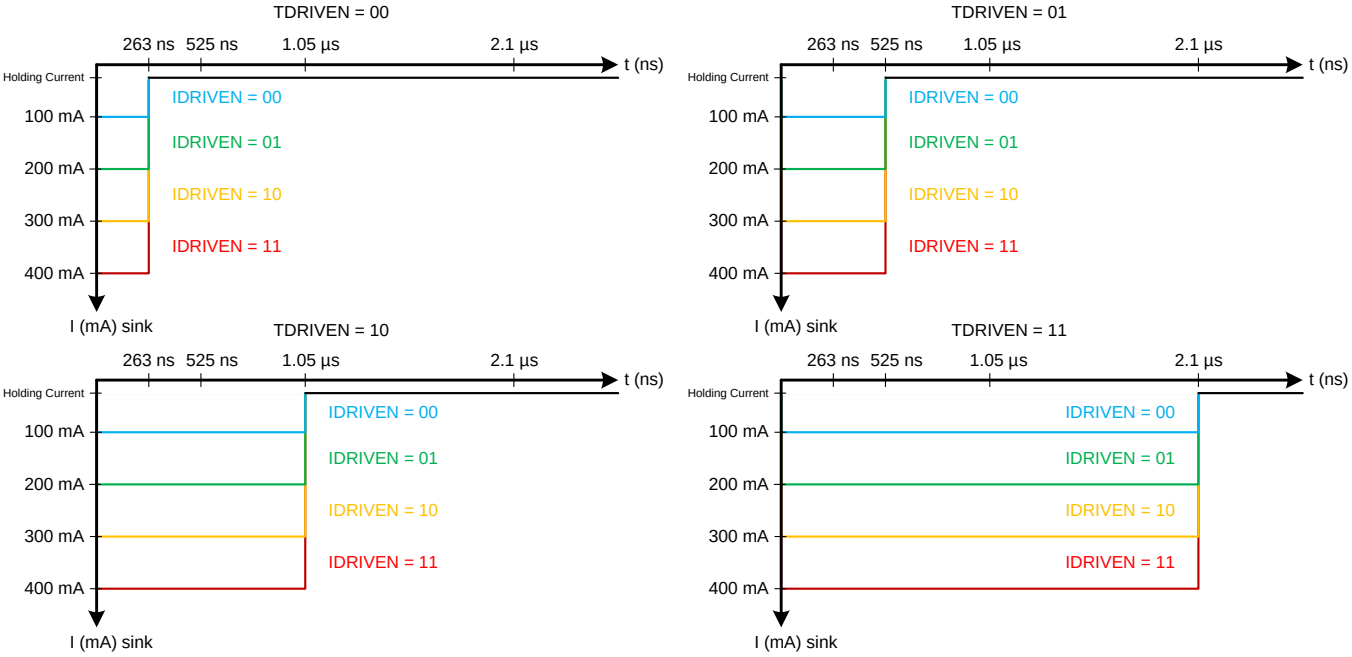


Figure 15. Gate Driver Sink Capability

7.3.7 Configuring Gate Drivers

IDRIVE and TDRIVE are selected based on the size of external FETs used. These registers need to be configured so that the FET gates are charged completely during TDRIVE. If IDRIVE and TDRIVE are chosen to be too low for a given FET, then the FET may not turn on completely. It is suggested to adjust these values in-system with the required external FETs and motors in order to determine the best possible setting for any application.

Note that TDRIVE will not increase the PWM time or change the PWM chopping frequency.

In a system with capacitor charge Q and desired rise time RT, IDRIVE, and TDRIVE can be initially selected based on:

$$IDRIVE > \frac{Q}{RT} \quad (2)$$

$$TDRIVE > 2 \times RT \quad (3)$$

For best results, select the smallest IDRIVE and TDRIVE that meet the above conditions.

Example:

If the gate charge is 15 nC and the desired rise time is 400 ns, then select

IDRIVEP = 50 mA, IDRIVEN = 100 mA

TDRIVEP = TDRIVEN = 1050 ns

7.3.8 External FET Selection

In a typical setup, the DRV8704 can support external FETs over 50 nC each. However, this capacity can be lower or higher based on the device operation. For an accurate calculation of FET driving capacity, use Equation 4.

$$Q < \frac{20\ mA \times (2 \times DTIME + TBLANK + TOFF)}{4} \quad (4)$$

Example:

If a DTIME is set to 0 (410 ns), TBLANK is set to 0 (1 µs), and TOFF is set to 0 (525 ns), then the DRV8704 will support Q < 11.5 nC FETs. (Please note that this is an absolute worst-case scenario with a PWM frequency about 430 kHz)

If a DTIME is set to 0 (410 ns), TBLANK is set to 0 (1 µs), and TOFF is set to 0x14 (10 µs), then the DRV8704 will support Q < 59 nC FETs (PWM frequency about 85 kHz).

If a DTIME is set to 0 (410 ns), TBLANK is set to 0 (1 µs), and TOFF is set to 0x60 (48 µs), then the DRV8704 will support Q < 249 nC FETs (PWM frequency about 20 kHz).

7.3.9 Protection Circuits

The DRV8704 is fully protected against undervoltage, overcurrent, and overtemperature events.

7.3.9.1 Overcurrent Protection (OCP)

Overcurrent is sensed by monitoring the voltage drop across the external FETs. If the voltage across a driven FET exceeds the value programmed by the OCPTH bits in the DRIVE register for more than the time period specified by the OCPDEG bits in the DRIVE register, an OCP event is recognized. During an OCP event, the H-bridge experiencing the OCP event is disabled. In addition, the corresponding xOCP bit in the STATUS register is set, and the FAULTn pin is driven low. The H-bridge (or H-bridges) will remain off, and the xOCP bit will remain set, until it is written to 0, or the device is reset.

7.3.9.2 Gate Driver Fault (PDF)

If excessive current is detected on the gate drive outputs (which would be indicative of a failed/shorted output FET or PCB fault), the H-bridge experiencing the fault is disabled, the xPDF bit in the STATUS register is set, and the FAULTn pin is driven low. The H-bridge will remain off, and the xPDF bit will remain set until it is written to 0, or the device is reset.

7.3.9.3 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled, the OTS bit in the STATUS register will be set, and the FAULTn pin will be driven low. Once the die temperature has fallen to a safe level operation will automatically resume and the OTS bit will reset. The FAULTn pin will be released after operation has resumed.

7.3.9.4 Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the undervoltage lockout threshold voltage, all FETs in the H-bridge will be disabled, the UVLO bit in the STATUS register will be set, and the FAULTn pin will be driven low. Operation will resume and the UVLO bit will reset when VM rises above the UVLO threshold. The FAULTn pin will be released after operation has resumed.

7.3.10 Serial Data Format

The serial data consists of a 16-bit serial write, with a read/write bit, 3 address bits and 12 data bits. The three address bits identify one of the registers defined in the register section above. To complete the read or write transaction, SCS must be set to a logic 0.

To write to a register, data is shifted in after the address as shown in the timing diagram below. The first bit at the beginning of the access must be logic low for a write operation.

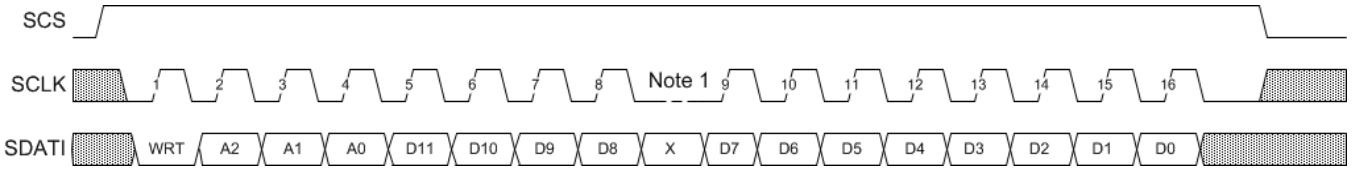
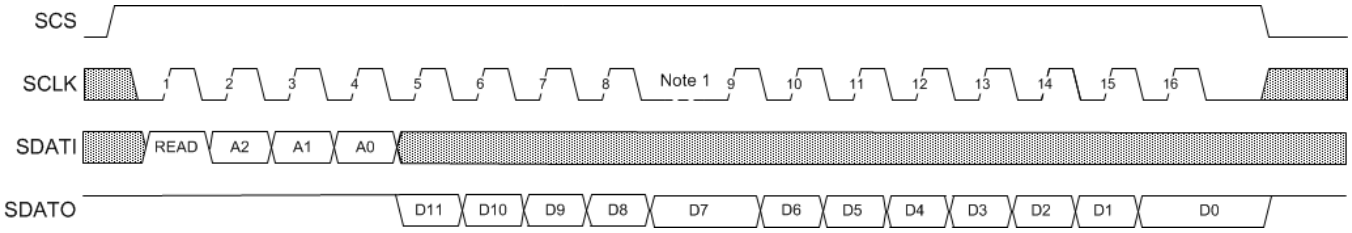


Figure 16. Serial Write Operation

Data may be read from the registers through the SDATO pin. During a read operation, only the address is used form the SDATI pin; the data bits following are ignored. The first bit at the beginning of the access must be logic high for a read operation.



(1) Any amount of time may pass between bits, as long as SCS stays active high. This allows two 8-bit writes to be used

Figure 17. Serial Read Operation

7.4 Device Functional Modes

The DRV8704 is active unless the nSLEEP pin is brought logic low. In sleep mode the charge pump is disabled, the H-bridge FETs are disabled Hi-Z, and the V5 regulator is disabled. The DRV8704 is brought out of sleep mode automatically if nSLEEP is brought logic high.

If a '0' is written to the ENBL bit, the H-bridge outputs are disabled, but the internal logic will still be active.

Table 2. Functional Modes

CONDITION		H-BRIDGE	CHARGE PUMP	SPI	V5
Operating	8 V < VM < 52 V nSLEEP pin = 1 ENBL bit = 1	Operating	Operating	Operating	Operating
Disabled	8 V < VM < 52 V nSLEEP pin = 1 ENBL bit = 0	Disabled	Operating	Operating	Operating
Sleep mode	8 V < VM < 52 V nSLEEP pin = 0	Disabled	Disabled	Disabled	Disabled
Fault encountered	Any fault condition met	Disabled	Depends on fault	Depends on fault	Depends on fault

7.5 Register Maps

7.5.1 Control Registers

The DRV8704 uses internal registers to control the operation of the motor. The registers are programmed by a serial SPI communications interface. At power-up or reset, the registers will be pre-loaded with default values as shown in Table 3.

Following is a map of the DRV8704 registers:

Table 3. DRV8704 Register Map

NAME	11	10	9	8	7	6	5	4	3	2	1	0		ADDRESS HEX
CTRL	DTIME		ISGAIN		Reserved							ENBL	R/W	00
TORQUE	Reserved				TORQUE								R/W	01
OFF	Reserved			PWMMODE	TOFF								R/W	02
BLANK	Reserved				TBLANK								R/W	03
DECAY	Reserved	DECMOD			TDECAY								R/W	04
RESERVED	Reserved												R/W	05
DRIVE	IDRIVEP		IDRIVEN		TDRIVEP		TDRIVEN		OCPDEG		OCPTH		R/W	06
STATUS	Reserved						UVLO	BPDF	APDF	BOCP	AOCP	OTS	R/W	07

Individual register contents are defined in the following sections.

7.5.1.1 CTRL Register (Address = 0x00h)

Table 4. CTRL Register

BIT	NAME	SIZE	R/W	DEFAULT	DESCRIPTION
0	ENBL	1	R/W	1	0: Disable motor **1: Enable motor**
7-1	Reserved	7	—	—	Reserved
9-8	ISGAIN	2	R/W	11	ISENSE amplifier gain set 00: Gain of 5 V/V 01: Gain of 10 V/V 10: Gain of 20 V/V **11: Gain of 40 V/V**
11-10	DTIME	2	R/W	00	Dead time set **00: 410-ns dead time** 01: 460-ns dead time 10: 670-ns dead time 11: 880-ns dead time

7.5.1.2 TORQUE Register (Address = 0x01h)

Table 5. TORQUE Register

BIT	NAME	SIZE	R/W	DEFAULT	DESCRIPTION
7-0	TORQUE	8	R/W	0xFFh	Sets full-scale output current for both H-bridges
11-8	Reserved	4	—	—	Reserved

7.5.1.3 OFF Register (Address = 0x02h)

Table 6. OFF Register

BIT	NAME	SIZE	R/W	DEFAULT	DESCRIPTION
7-0	TOFF	8	R/W	0x30h	Sets fixed off time, in increments of 525 ns 0x00h: 525 ns 0xFFh: 133.8 µs
8	PWMMODE	1	R/W	1	0: Do not write ‘0’ to this register **1: PWM control mode**
11-9	Reserved	3	—	—	Reserved

7.5.1.4 BLANK Register (Address = 0x03h)

Table 7. BLANK Register

BIT	NAME	SIZE	R/W	DEFAULT	DESCRIPTION
7-0	TBLANK	8	R/W	0x80h	Sets current trip blanking time, in increments of 21 ns 0x00h: 1.05 µs … 0x32h: 1.05 µs 0x33h: 1.07 µs … 0xFEh: 5.859 µs 0xFFh: 5.880 µs Also sets minimum on-time of PWM
11-8	Reserved	4	—	—	Reserved

7.5.1.5 DECAY Register (Address = 0x04h)

Table 8. DECAY Register

BIT	NAME	SIZE	R/W	DEFAULT	DESCRIPTION
7-0	TDECAY	8	R/W	0x10h	Sets mixed decay transition time, in increments of 525ns
10-8	DECMOD	3	R/W	000	**000: Force slow decay at all times** 001: Reserved 010: Force fast decay at all times 011: Use mixed decay at all times 100: Reserved 101: Use auto mixed decay at all times 110 – 111: Reserved
11	Reserved	1	—	—	Reserved

7.5.1.6 Reserved Register Address = 0x05h

Table 9. Reserved Register

BIT	NAME	SIZE	R/W	DEFAULT	DESCRIPTION
11-0	Reserved	12	—	—	Reserved

7.5.1.7 DRIVE Register Address = 0x06h

Table 10. DRIVE Register

BIT	NAME	SIZE	R/W	DEFAULT	DESCRIPTION
1-0	OCPTH	2	R/W	01	OCP threshold 00: 250 mV **01: 500 mV** 10: 750 mV 11: 1000 mV
3-2	OCPDEG	2	R/W	01	OCP deglitch time 00: 1.05 µs **01: 2.1 µs** 10: 4.2 µs 11: 8.4 µs
5-4	TDRIVEN	2	R/W	10	Gate drive sink time 00: 263 ns 01: 525 ns **10: 1.05 µs** 11: 2.10 µs

Table 10. DRIVE Register (continued)

BIT	NAME	SIZE	R/W	DEFAULT	DESCRIPTION
7-6	TDRIVEP	2	R/W	10	Gate drive source time 00: 263 ns 01: 525 ns **10: 1.05 µs** 11: 2.10 µs
9-8	IDRIVEN	2	R/W	11	Gate drive peak sink current 00: 100-mA peak (sink) 01: 200-mA peak (sink) 10: 300-mA peak (sink) **11: 400-mA peak (sink)**
11-10	IDRIVEP	2	R/W	11	Gate drive peak source current 00: 50-mA peak (source) 01: 100-mA peak (source) 10: 150-mA peak (source) **11: 200-mA peak (source)**

7.5.1.8 STATUS Register (Address = 0x07h)

Table 11. STATUS Register

BIT	NAME	SIZE	R/W	DEFAULT	DESCRIPTION
0	OTS	1	R	0	0: Normal operation 1: Device has entered overtemperature shutdown Write a '0' to this bit to clear the fault and resume operation Operation automatically resumes once temperature has fallen to safe levels
1	AOCP	1	R/W	0	0: Normal operation 1: Channel A overcurrent shutdown Write a '0' to this bit to clear the fault and resume operation
2	BOCP	1	R/W	0	0: Normal operation 1: Channel B overcurrent shutdown Write a '0' to this bit to clear the fault and resume operation
3	APDF	1	R/W	0	0: Normal operation 1: Channel A predriver fault Write a '0' to this bit to clear the fault and resume operation
4	BPDF	1	R/W	0	0: Normal operation 1: Channel B predriver fault Write a '0' to this bit to clear the fault and resume operation
5	UVLO	1	R	0	0: Normal operation 1: Undervoltage lockout Write a '0' to this bit to clear the fault and resume operation The UVLO bit cannot be cleared in sleep mode Operation automatically resumes once VM has risen
11-6	Reserved	5	—	—	Reserved

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8704 is used in brushed DC motor control.

8.2 Typical Application

The following design procedure can be used to configure the DRV8704.

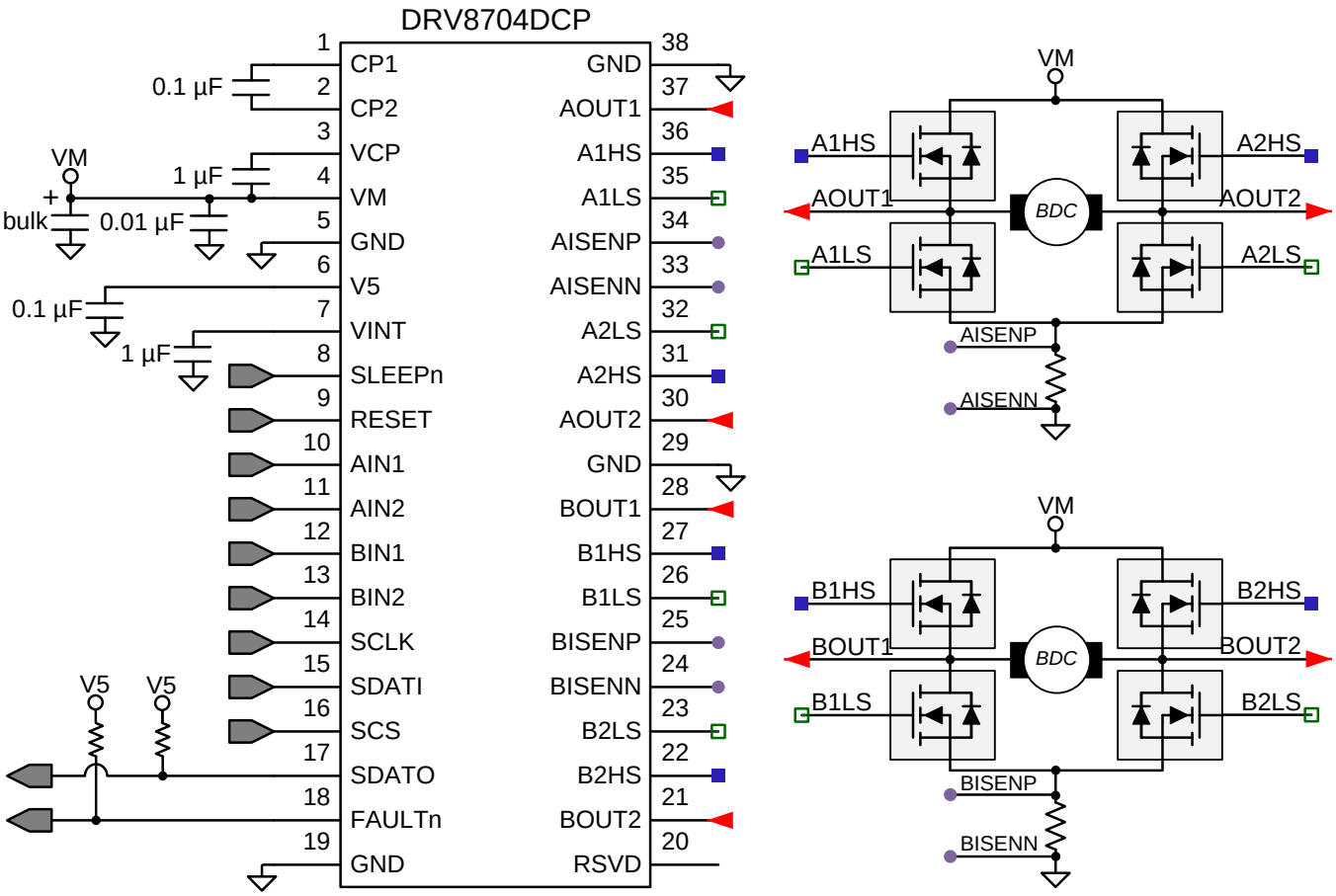


Figure 18. Dual Brushed-DC Motor Control

Typical Application (continued)

8.2.1 Design Requirements

Table 12 shows design input parameters for system design.

Table 12. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	VM	24 V
FET total gate charge (1)	Q_g	41 nC (typically)
FET gate-to-drain charge (1)	Q_{gd}	6.7 nC (typically)
Target FET gate rise time	RT	20 to 100 ns
Motor winding resistance	R_L	400 mΩ
Motor winding inductance	L_L	258 µH
Target chopping current	I_{CHOP}	5.5 A

(1) FET part number is CSD18540Q5B

8.2.2 Detailed Design Procedure

8.2.2.1 External FET Selection

The DRV8704 FET support is based on the charge pump capacity and output PWM frequency. For a quick calculation of FET driving capacity, use the following equations when drive and brake (slow decay) are the primary modes of operation:

$$Q_g < \frac{I_{VCP}}{2 \times f_{PWM}} \quad (5)$$

where

- f_{PWM} is the maximum desired PWM frequency to be applied to the DRV8704 inputs or the current chopping frequency, whichever is larger.
- I_{VCP} is the charge pump capacity, which is 20 mA.

The factor of two arises because there are two H-bridges present.

The current chopping frequency is at most:

$$f_{PWM} < \frac{1}{t_{OFF} + t_{BLANK}} \quad (6)$$

Example:

If a system uses a maximum PWM frequency of 40 kHz, then the DRV8704 will support Q_g < 250 nC FETs.

If the application will require a forced fast decay (or alternating between drive and reverse drive), the maximum FET driving capacity is given by:

$$Q_g < \frac{I_{VCP}}{4 \times f_{PWM}} \quad (7)$$

8.2.2.2 IDRIVE Configuration

IDRIVE is selected based on the gate charge of the FETs. The IDRIVEx and TDRIVEx registers need to be configured so that the FET gates are charged completely during TDRIVE. If IDRIVE is chosen to be too low for a given FET, or if TDRIVE is less than the intended rise time, then the FET may not turn on completely. TI suggests to adjust these values in-system with the required external FETs and motor to determine the best possible setting for any application.

For FETs with a known gate-to-drain charge Q_{gd} and desired rise time RT, IDRIVE and TDRIVE can be selected based on:

$$IDRIVE > \frac{Q_{gd}}{RT} \quad (8)$$

$$TDRIVE > 2 \times RT \quad (9)$$

Example:

If the gate-to-drain charge is 5.9 nC, and the desired rise time is around 20 to 100 ns:

$IDRIVE_1$ = 6.7 nC / 20 ns = 335 mA

$IDRIVE_2$ = 6.7 nC / 100 ns = 67 mA

Select IDRIVE between 67 and 335 mA.

We select IDRIVEP as 200-mA source and IDRIVEP as 400-mA sink.

We select TDRIVEN and TDRIVEP as 525 ns.

8.2.2.3 Current Chopping Configuration

The chopping current is set based on the sense resistor value, shunt amplifier gain set by the ISGAIN register, and the TORQUE register setting. The following is used to calculate the current:

$$I_{CHOP} = \frac{2.75\ V \times TORQUE}{256 \times ISGAIN \times R_{ISENSE}} \quad (10)$$

Example:

If the desired chopping current is 5.5 A:

Set R_{SENSE} = 100 mΩ.

Set ISGAIN to the 5 V/V setting.

The TORQUE register can be (decimal) 255.

8.2.2.4 Decay Modes

The DRV8704 supports several different decay modes: slow decay, fast decay, mixed decay, and automatic mixed decay. The current through the motor windings is regulated using an adjustable fixed-time-off scheme. This means that after any drive phase, when a motor winding current has hit the current chopping threshold (I_{TRIP}), the DRV8704 will place the winding in one of the decay modes for TOFF. After TOFF, a new drive phase starts.

8.2.2.5 Sense Resistor

For optimal performance, it is important for the sense resistor to be:

- Surface-mount
- Low inductance
- Rated for high enough power
- Placed closely to the motor driver

The power dissipated by the sense resistor equals $I_{RMS}^{\ 2} \times R$. For example, if peak motor current is 3 A, RMS motor current is 2 A, and a 0.05-Ω sense resistor is used, the resistor will dissipate 2 A^2 × 0.05 Ω = 0.2 W. The power quickly increases with higher current levels.

Resistors typically have a rated power within some ambient temperature range, along with a derated power curve for high ambient temperatures. When a PCB is shared with other components generating heat, margin should be added. It is always best to measure the actual sense resistor temperature in a final system, along with the power MOSFETs, as those are often the hottest components.

Because power resistors are larger and more expensive than standard resistors, it is common practice to use multiple standard resistors in parallel, between the sense node and ground. This distributes the current and heat dissipation.

8.2.3 Application Curves

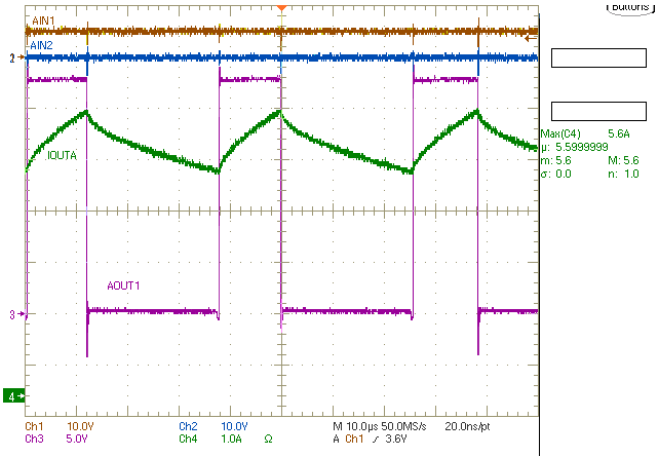


Figure 19. Current Regulation

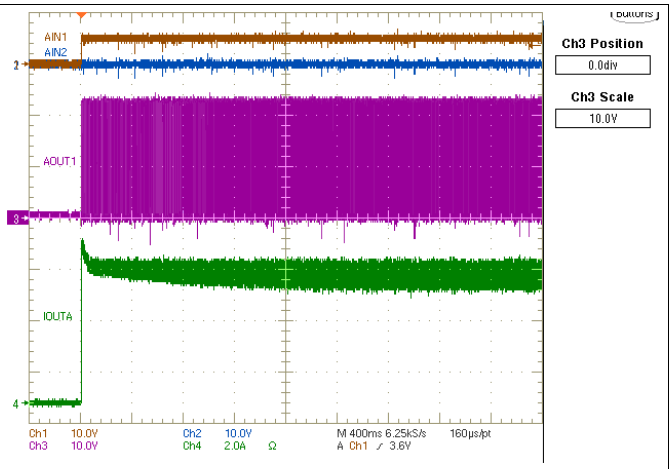


Figure 20. Motor Startup

9 Power Supply Recommendations

The DRV8704 is designed to operate from an input voltage supply (VM) range between 8 and 52 V. A 0.01-µF ceramic capacitor rated for VM must be placed as close to the DRV8704 as possible. In addition, a bulk capacitor must be included on VM.

9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

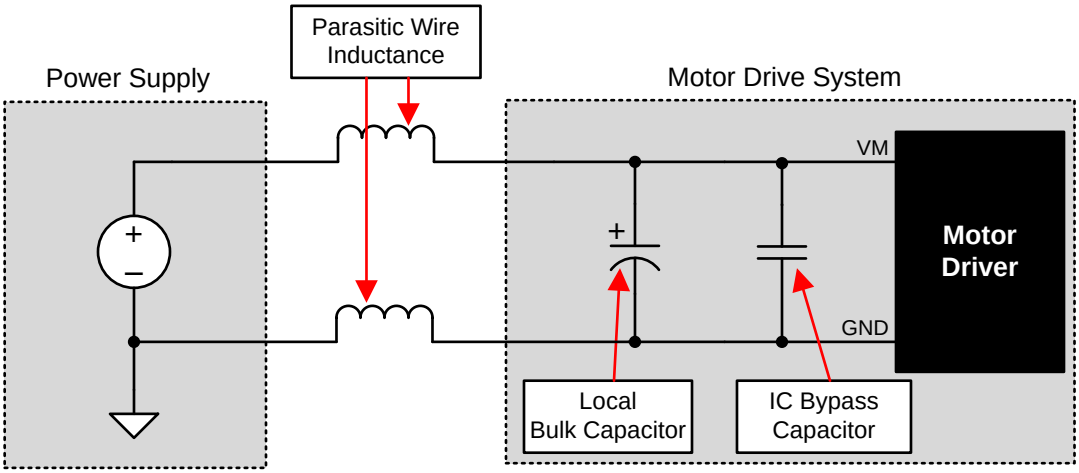


Figure 21. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

10 Layout

10.1 Layout Guidelines

The VM terminal should be bypassed to GND using a low-ESR ceramic bypass capacitor with a recommended value of 0.01 µF rated for VM. This capacitor should be placed as close to the VM pin as possible with a thick trace or ground plane connection to the device GND pin.

The VM pin must be bypassed to ground using a bulk capacitor rated for VM. This component may be an electrolytic. The bulk capacitor should be placed to minimize the distance of the high-current path through the external FETs. The connecting metal trace widths should be as wide as possible, and numerous vias should be used when connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

A low-ESR ceramic capacitor must be placed in between the CPL and CPH pins. A value of 0.1 µF rated for VM is recommended. Place this component as close to the pins as possible.

A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. A value of 1 µF rated for 16 V is recommended. Place this component as close to the pins as possible.

Bypass VINT to ground with a ceramic capacitor rated 6.3 V. Place this bypassing capacitor as close to the pin as possible.

Bypass V5 to ground with a ceramic capacitor rated 6.3 V. Place this bypassing capacitor as close to the pin as possible.

If desired, align the external NMOS FETs as shown on the next page to facilitate layout. Route the AOUT1, AOUT2, BOUT1, and BOUT2 nets to the motor windings.

Use separate traces to connect the xISENP and xISENN pins to the sense resistor terminals.

10.2 Layout Example

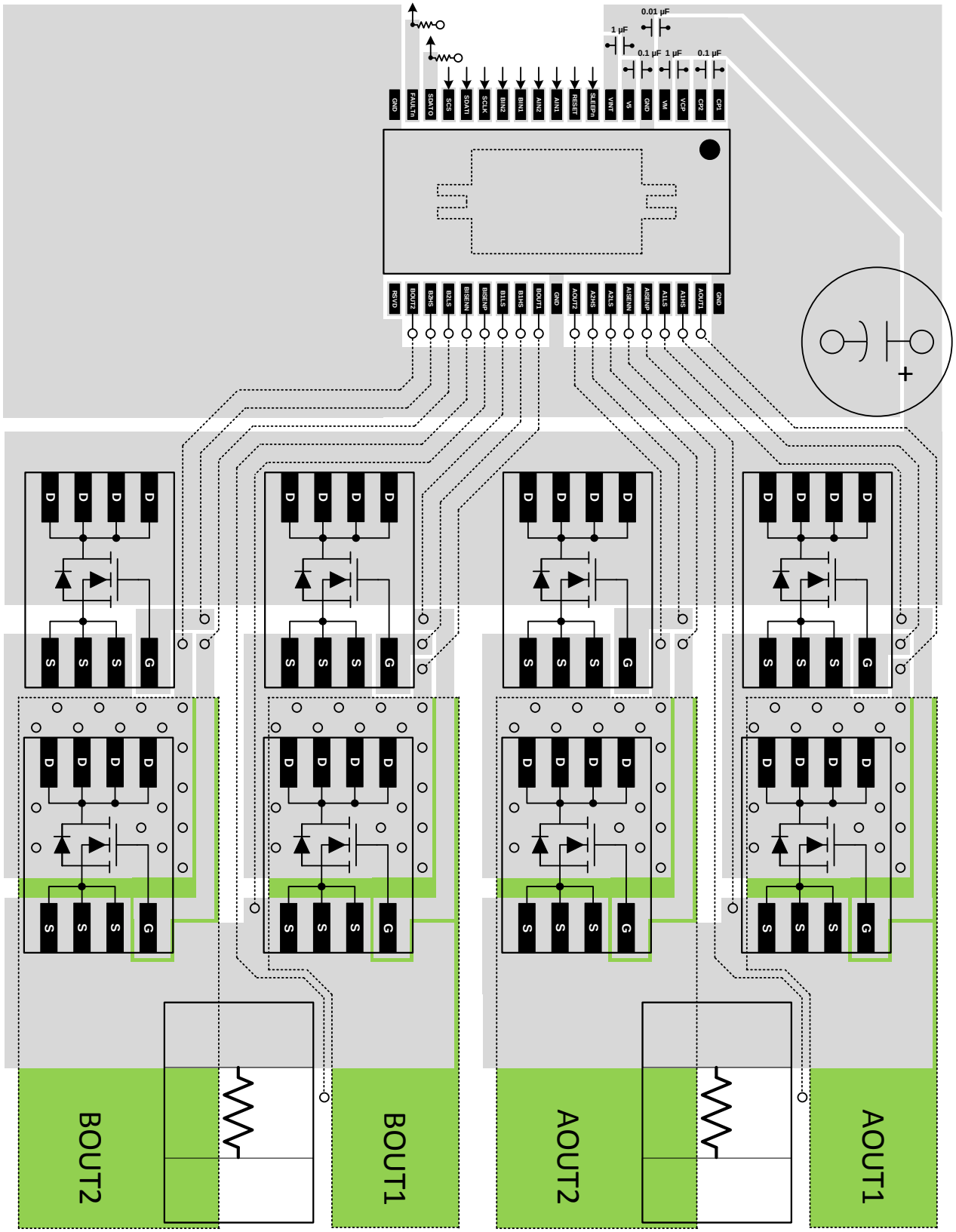


Figure 22. Board Layout Example

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8704DCP	ACTIVE	HTSSOP	DCP	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV8704	Samples
DRV8704DCPR	ACTIVE	HTSSOP	DCP	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV8704	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

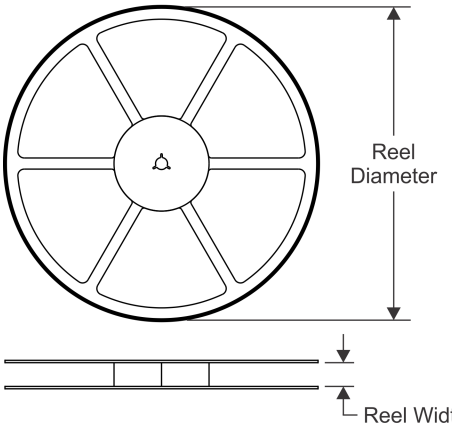
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

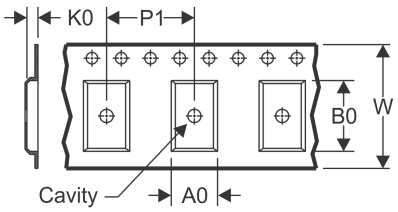
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

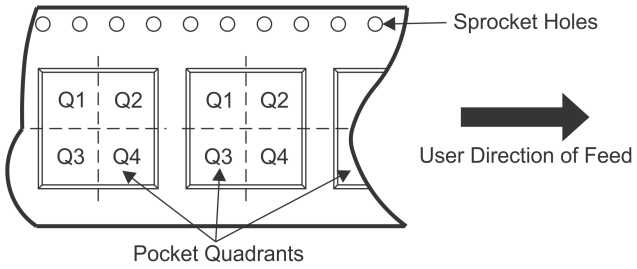


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

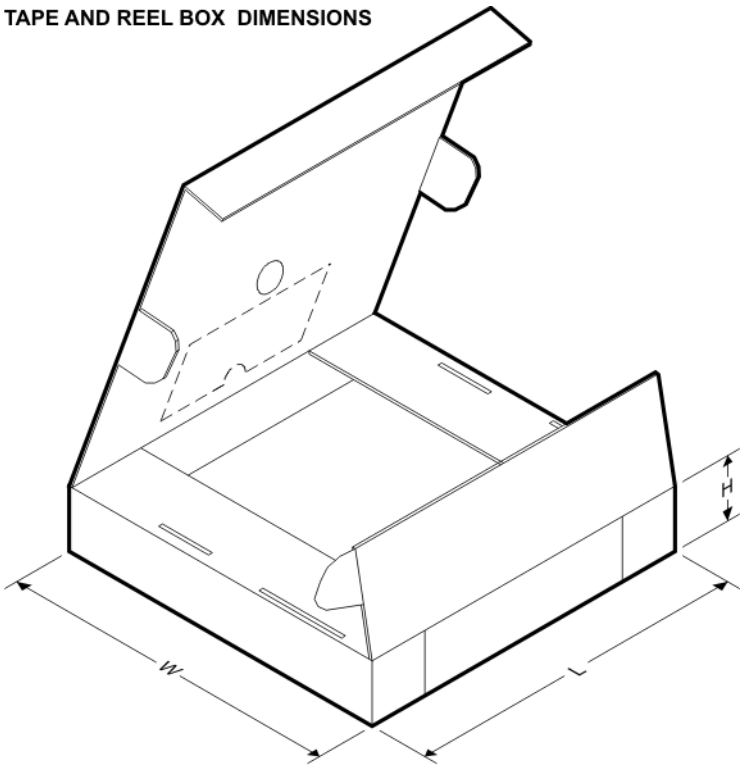
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8704DCPR	HTSSOP	DCP	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

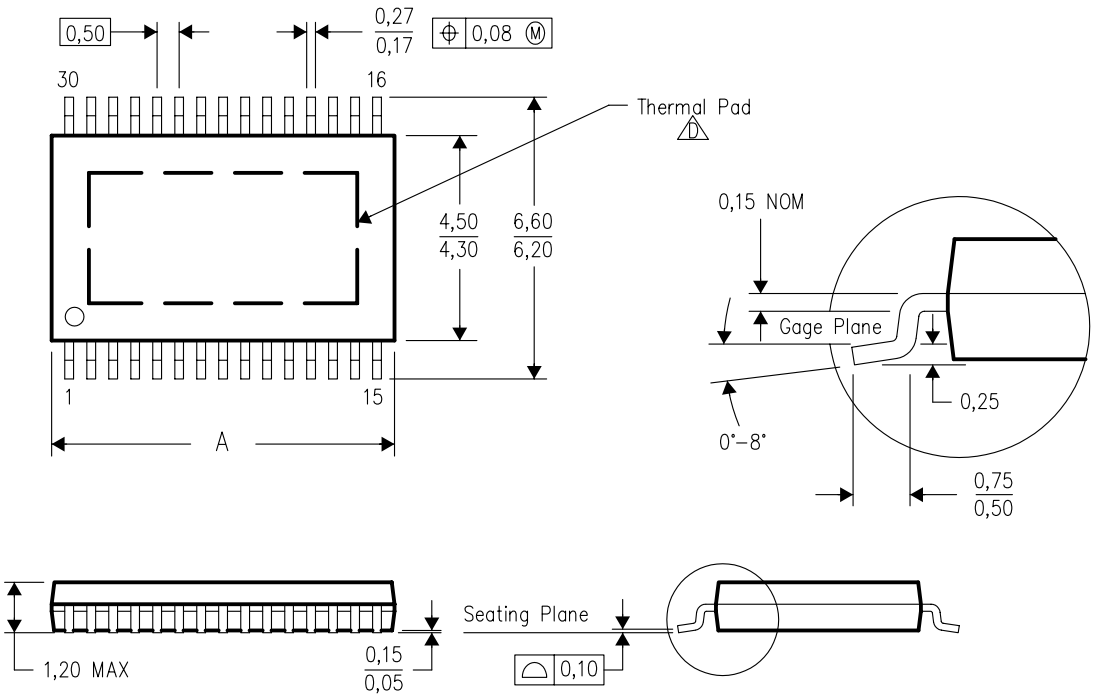


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8704DCPR	HTSSOP	DCP	38	2000	367.0	367.0	38.0

DCP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

30 PIN SHOWN



DIM \ PINS **	28	30	38	44	50
A MAX	7,90	7,90	9,80	11,40	12,60
A MIN	7,70	7,70	9,60	11,20	12,40

4073267/C 03/05

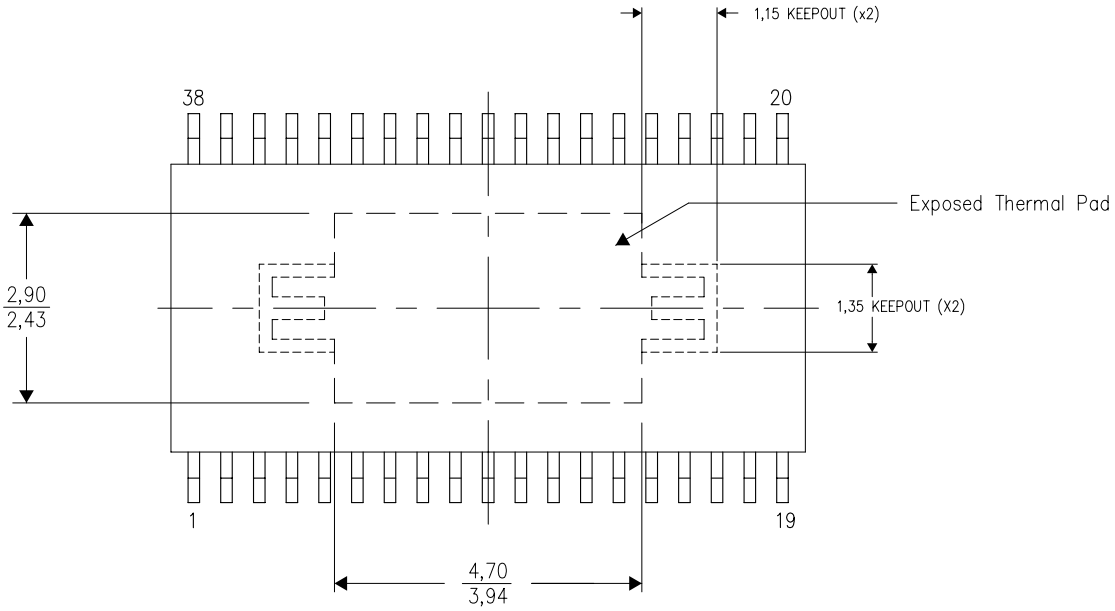
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protusions, mold flash not to exceed 0.15mm.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com. See the product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–153

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

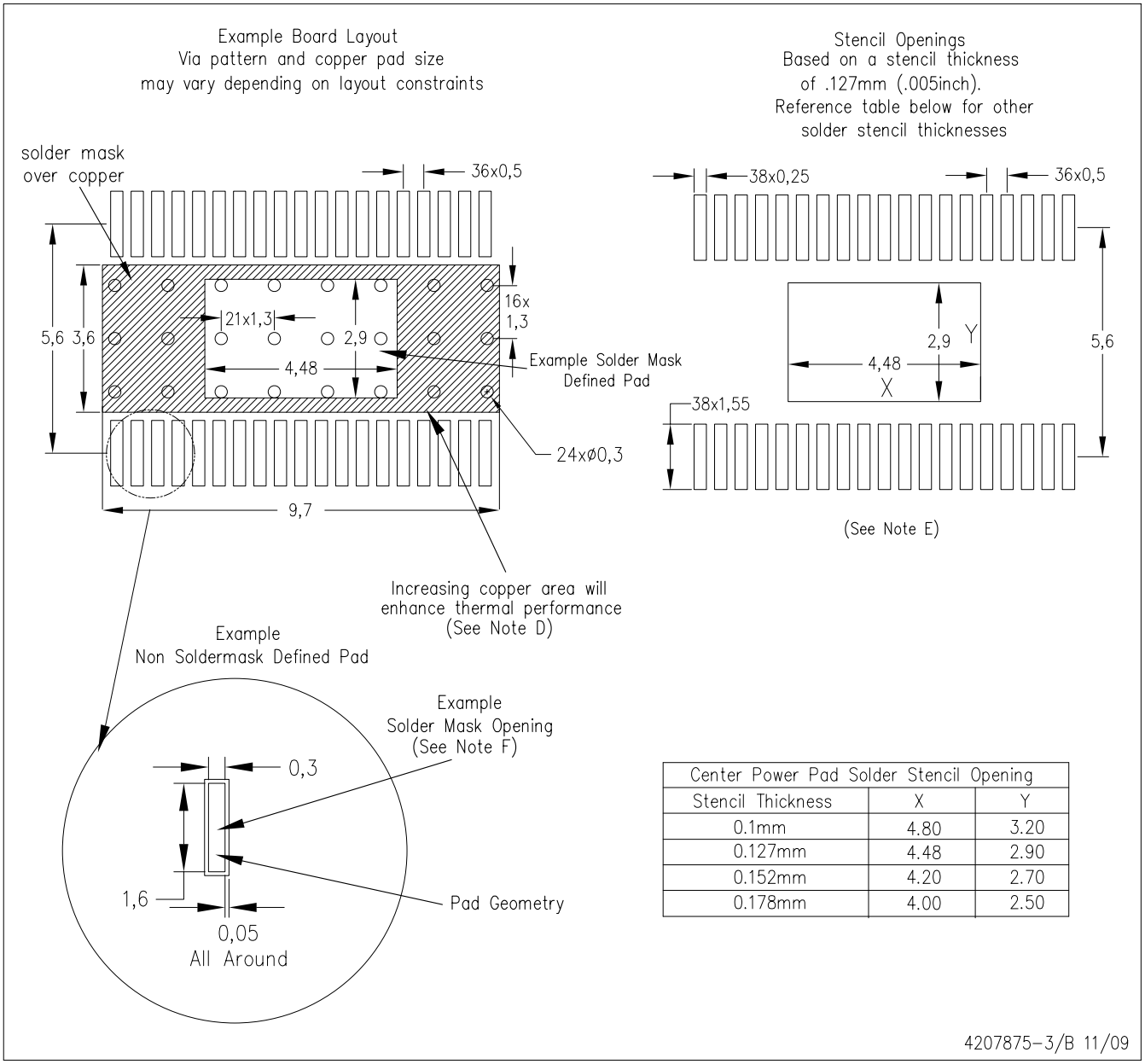


Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DCP (R–PDSO–G38) PowerPAD™



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	4.80	3.20
0.127mm	4.48	2.90
0.152mm	4.20	2.70
0.178mm	4.00	2.50

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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