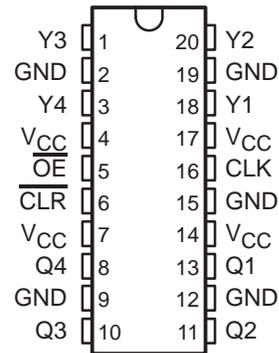


# CDC337 CLOCK DRIVER WITH 3-STATE OUTPUTS

SCAS330B – DECEMBER 1990 – REVISED OCTOBER 1998

- **Low Output Skew, Low Pulse Skew for Clock-Distribution and Clock-Generation Applications**
- **TTL-Compatible Inputs and CMOS-Compatible Outputs**
- **Distributes One Clock Input to Eight Outputs**
  - Four Same-Frequency Outputs
  - Four Half-Frequency Outputs
- **Distributed  $V_{CC}$  and Ground Pins Reduce Switching Noise**
- **High-Drive Outputs ( $-48\text{-mA } I_{OH}$ ,  $48\text{-mA } I_{OL}$ )**
- **State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Package Options Include Plastic Small-Outline (DW)**

**DW PACKAGE  
(TOP VIEW)**



## description

The CDC337 is a high-performance, low-skew clock driver. It is specifically designed for applications requiring synchronized output signals at both the clock frequency and one-half the clock frequency. The four Y outputs switch in phase and at the same frequency as the clock (CLK) input. The four Q outputs switch at one-half the frequency of CLK.

When the output-enable ( $\overline{OE}$ ) input is low and the clear ( $\overline{CLR}$ ) input is high, the Y outputs follow CLK and the Q outputs toggle on low-to-high transitions at CLK. Taking  $\overline{CLR}$  low asynchronously resets the Q outputs to the low level. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

The CDC337 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

**FUNCTION TABLE**

INPUTS			OUTPUTS	
$\overline{OE}$	$\overline{CLR}$	CLK	Y1–Y4	Q1–Q4
H	X	X	Z	Z
L	L	L	L	L
L	L	H	H	L
L	H	L	L	$Q_0^{\dagger}$
L	H	$\uparrow$	H	$\overline{Q_0}^{\dagger}$

† The level of the Q outputs before the indicated steady-state input conditions were established



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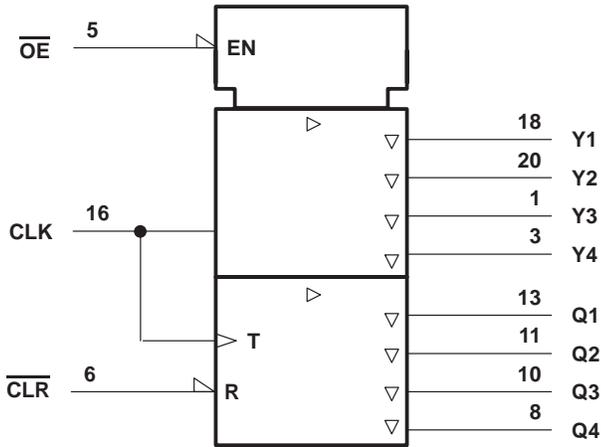
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# CDC337 CLOCK DRIVER WITH 3-STATE OUTPUTS

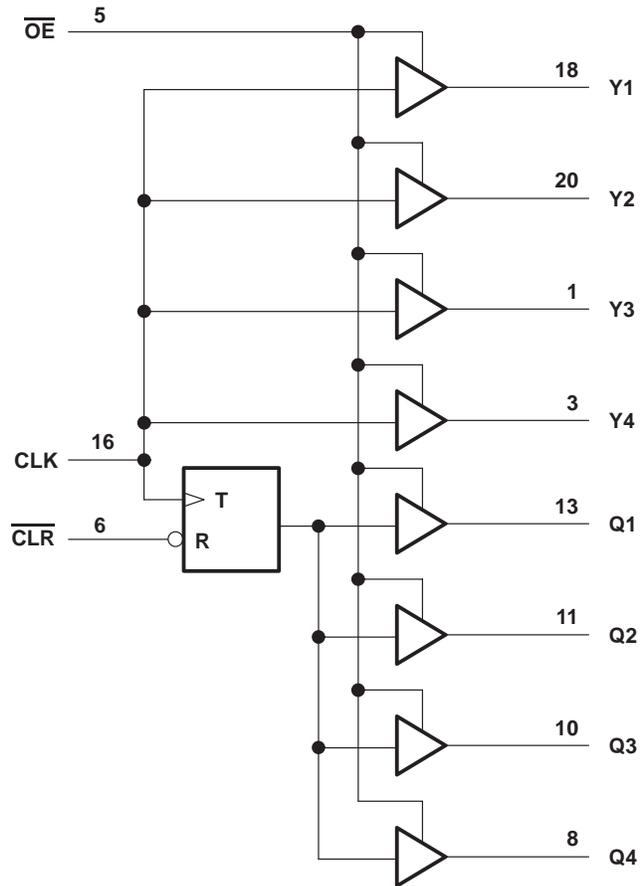
SCAS330B – DECEMBER 1990 – REVISED OCTOBER 1998

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, $I_O$ .....	96 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-18 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2) .....	1.6 W
Storage temperature range, $T_{stg}$ .....	$-65^\circ\text{C}$ to $150^\circ\text{C}$

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of  $150^\circ\text{C}$  and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

**CDC337**  
**CLOCK DRIVER**  
**WITH 3-STATE OUTPUTS**

SCAS330B – DECEMBER 1990 – REVISED OCTOBER 1998

**recommended operating conditions (see Note 3)**

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4.75	5.25	V
$V_{IH}$	High-level input voltage	2		V
$V_{IL}$	Low-level input voltage		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current		-48	mA
$I_{OL}$	Low-level output current		48	mA
$f_{clock}$	Input clock frequency		80	MHz
$T_A$	Operating free-air temperature	-40	85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$	$V_{CC} = 4.75\text{ V}$ ,	$I_I = -18\text{ mA}$			-1.2	V
$V_{OH}$	$V_{CC} = 4.75\text{ V}$ ,	$I_{OH} = -32\text{ mA}$	3.75			V
$V_{OL}$	$V_{CC} = 4.75\text{ V}$ ,	$I_{OL} = 32\text{ mA}$			0.55	V
$I_{IH}$	$V_{CC} = 5.25\text{ V}$ ,	$V_I = 2.7\text{ V}$			50	μA
$I_{IL}$	$V_{CC} = 5.25\text{ V}$ ,	$V_I = 0.5\text{ V}$			-50	μA
$I_{OZ}$	$V_{CC} = 5.25\text{ V}$ ,	$V_O = V_{CC}$ or GND			±50	μA
$I_{CC}$	$V_{CC} = 5.25\text{ V}$ ,	$V_I = V_{CC}$ or GND, $I_O = 0$	Outputs high		70	mA
			Outputs low		85	
			Outputs disabled		70	
$C_i$	$V_I = 2.5\text{ V}$ or $0.5\text{ V}$			3	pF	
$C_o$	$V_O = V_{CC}$ or GND			10	pF	

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

		MIN	MAX	UNIT
$f_{clock}$	Clock frequency		80	MHz
$t_w$	Pulse duration	$\overline{\text{CLR}}$ low	4	ns
		CLK low	4	
		CLK high	4	
$t_{su}$	Setup time, $\overline{\text{CLR}}$ inactive before $\text{CLK}\uparrow$	2		ns
	Clock duty cycle	40%	60%	



**CDC337**  
**CLOCK DRIVER**  
**WITH 3-STATE OUTPUTS**

SCAS330B – DECEMBER 1990 – REVISED OCTOBER 1998

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Note 4 and Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
$f_{max}$			80			MHz
$t_{PLH}$	CLK	Any Y or Q	4		9	ns
$t_{PHL}$			4		9	
$t_{PHL}$	$\overline{CLR}$	Any Q	4		10	ns
$t_{PZH}$	$\overline{OE}$	Any Y or Q	3		7	ns
$t_{PZL}$			3		7	
$t_{PHZ}$	$\overline{OE}$	Any Y or Q	2		7	ns
$t_{PLZ}$			2		7	
$t_{sk(o)}$	CLK↑	Y↑			0.75	ns
		Q↑			0.9	
		Y↑ and Q↑			0.9	
$t_r$				0.9		ns
$t_f$				0.7		ns

† All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

NOTE 4: All specifications are valid only for all outputs switching.

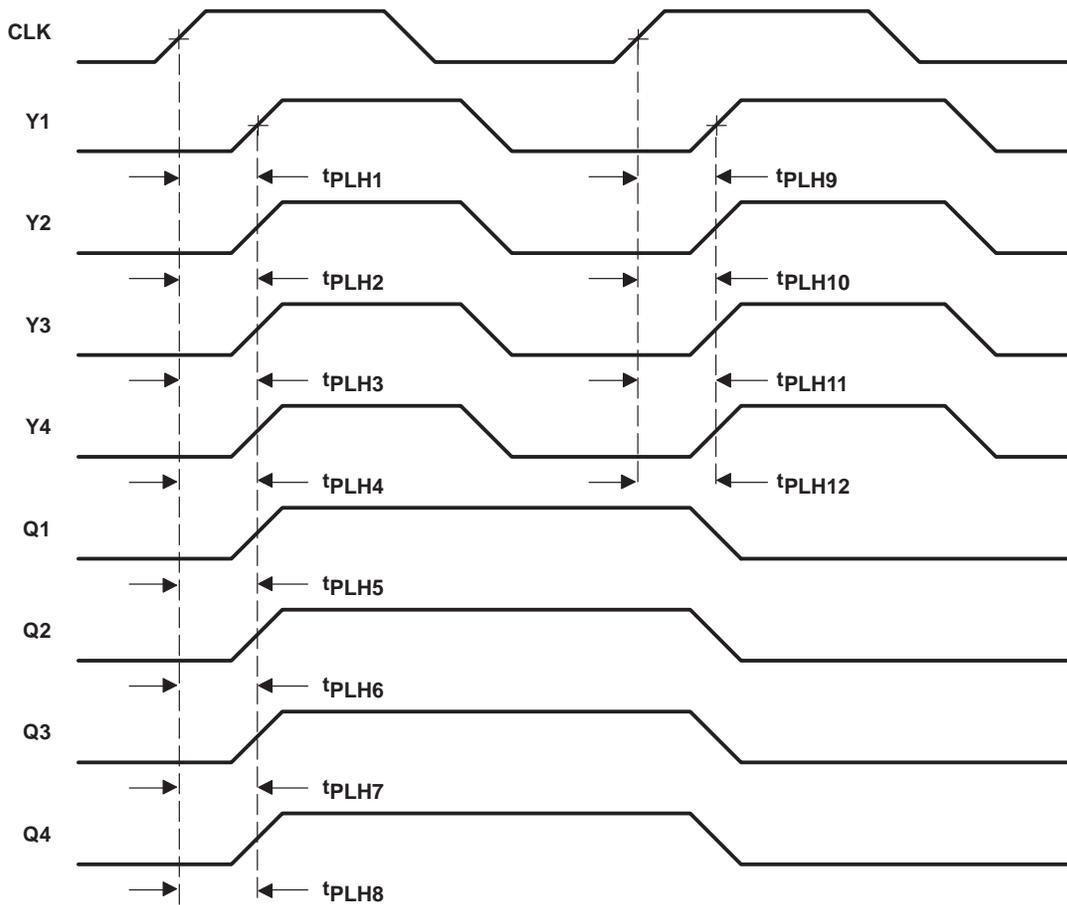




**CDC337  
CLOCK DRIVER  
WITH 3-STATE OUTPUTS**

SCAS330B – DECEMBER 1990 – REVISED OCTOBER 1998

**PARAMETER MEASUREMENT INFORMATION**



- NOTES: A. Output skew,  $t_{sk(o)}$ , from  $CLK\uparrow$  to  $Y\uparrow$ , is calculated as the greater of the difference between the fastest and slowest of  $t_{PLHn}$  ( $n = 1, 2, 3, 4$ ) or  $t_{PLHn}$  ( $n = 9, 10, 11, 12$ ).
- B. Output skew,  $t_{sk(o)}$ , from  $CLK\uparrow$  to  $Q\uparrow$ , is calculated as the greater of the difference between the fastest and slowest of  $t_{PLHn}$  ( $n = 5, 6, 7, 8$ ).
- C. Output skew,  $t_{sk(o)}$ , from  $CLK\uparrow$  to  $Y\uparrow$  and  $Q\uparrow$ , is calculated as the greater of the difference between the fastest and slowest of  $t_{PLHn}$  ( $n = 1, 2, \dots, 8$ ).

**Figure 2. Waveforms for Calculation of  $t_{sk(o)}$**

**CDC337  
CLOCK DRIVER  
WITH 3-STATE OUTPUTS**

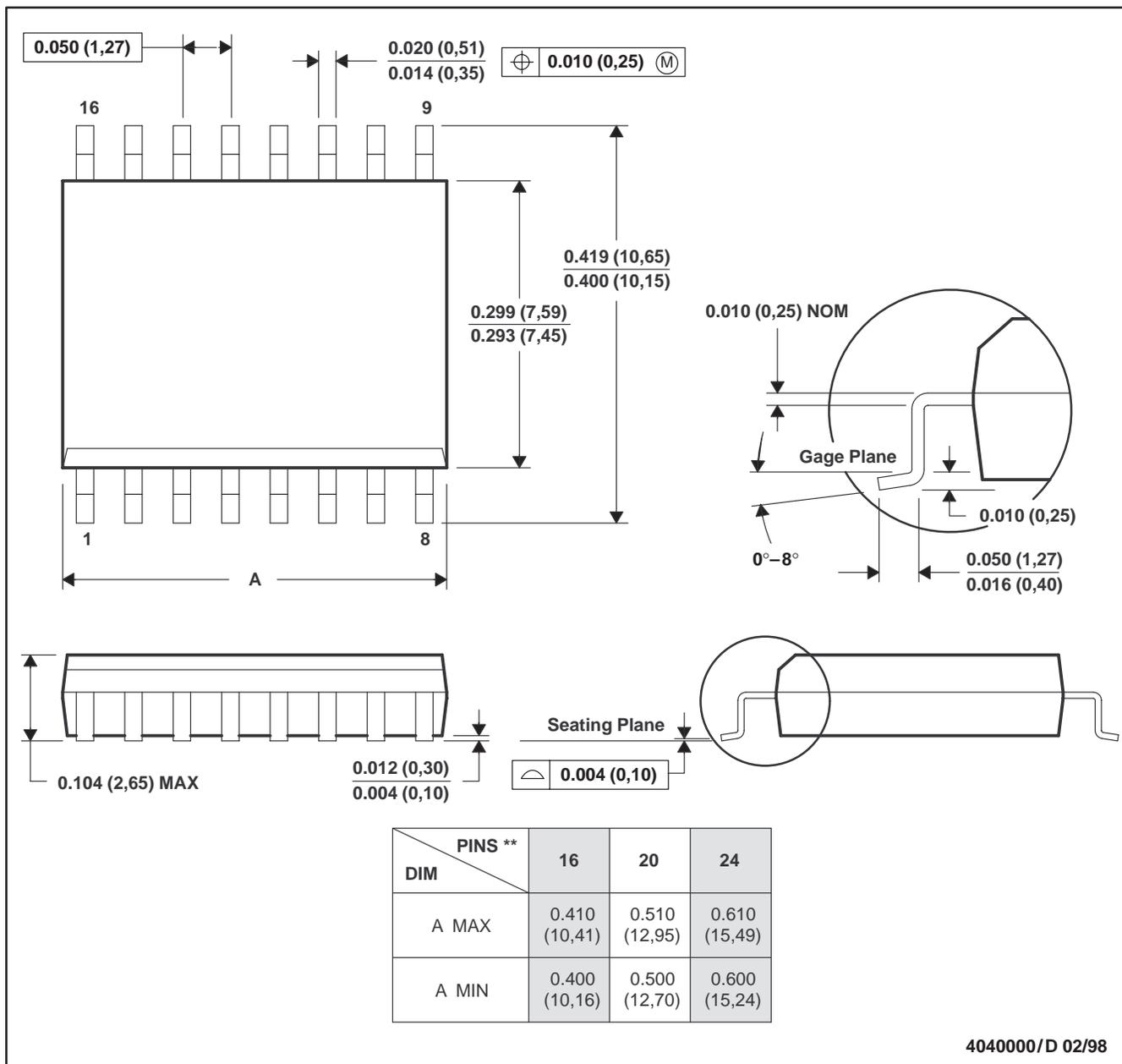
SCAS330B – DECEMBER 1990 – REVISED OCTOBER 1998

**MECHANICAL INFORMATION**

**DW (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

16 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MS-013



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDC337DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDC337	<a href="#">Samples</a>
CDC337DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDC337	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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