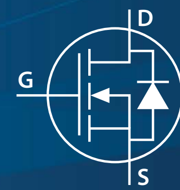
EPC2204 – Enhancement Mode Power Transistor

V_{DS} , 100 V
$R_{DS(on)}$, 6 mΩ
I_D , 29 A



EFFICIENT POWER CONVERSION

RoHS Halogen-Free

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

EPC2204 eGaN® FETs are supplied only in passivated die form with solder bars.
Die Size: 2.5 mm x 1.5 mm

Applications

- DC-DC Converters
- Isolated DC-DC Converters
- Lidar
- Sync rectification for AC-DC and DC-DC
- Point of Load Converters
- USB-C
- Class-D Audio
- LED Lighting
- E-Mobility

Benefits

- Ultra High Efficiency
- No Reverse Recovery
- Ultra Low Q_G
- Small Footprint

Maximum Ratings

	PARAMETER	VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
V_{DS}	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150 °C)	120	V
I_D	Continuous (T_A = 25°C)	29	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	125	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	

Thermal Characteristics

	PARAMETER	TYP	UNIT
$R_{θJC}$	Thermal Resistance, Junction-to-Case	1	°C/W
$R_{θJB}$	Thermal Resistance, Junction-to-Board	2.5	
$R_{θJA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	64	

Note 1: $R_{θJA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Static Characteristics (T_J = 25°C unless otherwise stated)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 0.25 mA	100			V
I_{DSS}	Drain-Source Leakage	V_{GS} = 0 V, V_{DS} = 80 V		0.04	0.2	mA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.01	0.25	
	Gate-to-Source Forward Leakage#	V_{GS} = 5 V, T_J = 125°C		0.3	6.7	
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		0.03	0.2	
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 4 mA	0.8	1.1	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 16 A		4.4	6	mΩ
V_{SD}	Source-Drain Forward Voltage	I_S = 0.5 A, V_{GS} = 0 V		1.6		V

Defined by design. Not subject to production test.

Dynamic Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance#	V_{DS} = 50 V, V_{GS} = 0 V		644	851	pF
C_{RSS}	Reverse Transfer Capacitance			2.3		
C_{OSS}	Output Capacitance#			304	456	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	V_{DS} = 0 to 50 V, V_{GS} = 0 V		401		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			501		
R_G	Gate Resistance			0.4		Ω
Q_G	Total Gate Charge#	V_{DS} = 50 V, V_{GS} = 5 V, I_D = 16 A		5.7	7.4	nC
Q_{GS}	Gate-to-Source Charge	V_{DS} = 50 V, I_D = 16 A		1.8		
Q_{GD}	Gate-to-Drain Charge			0.8		
$Q_{G(TH)}$	Gate Charge at Threshold			1		
Q_{OSS}	Output Charge#	V_{DS} = 50 V, V_{GS} = 0 V		25	38	
Q_{RR}	Source-Drain Recovery Charge			0		

Defined by design. Not subject to production test.
Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25°C

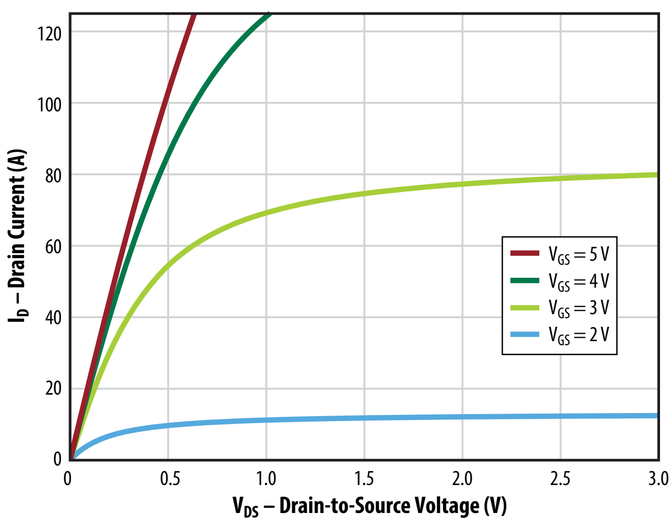


Figure 2: Transfer Characteristics

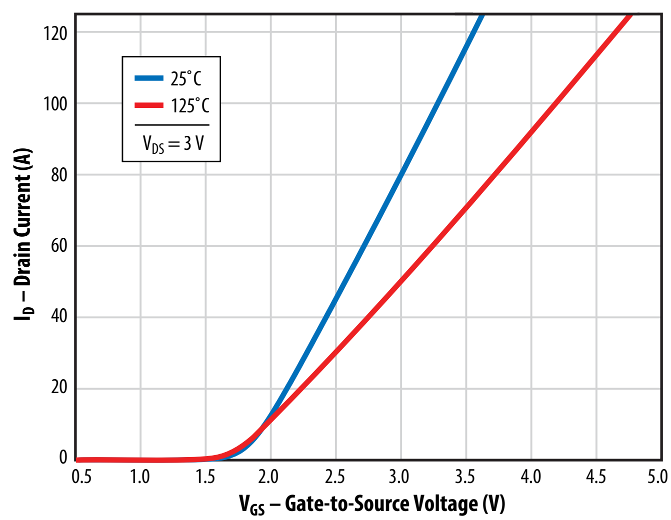


Figure 3: $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

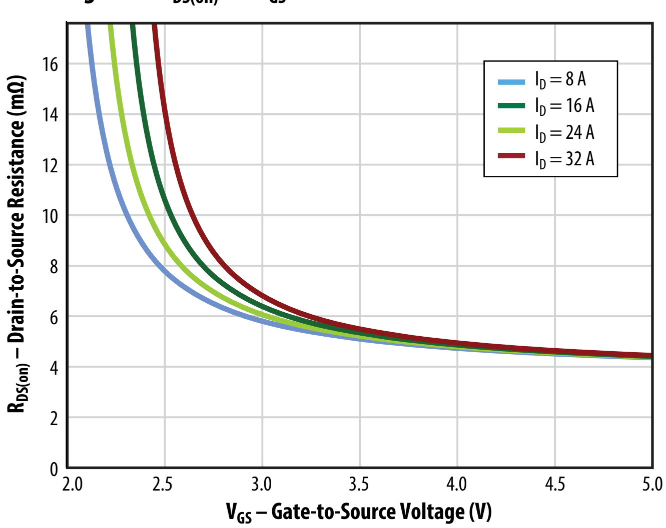


Figure 4: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

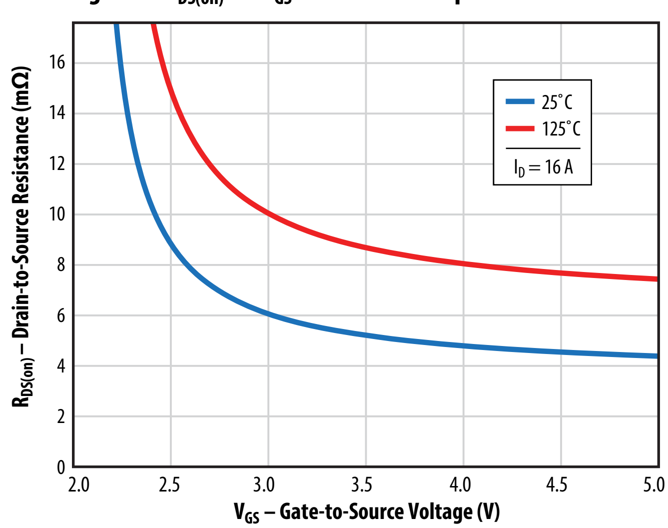


Figure 5a: Capacitance (Linear Scale)

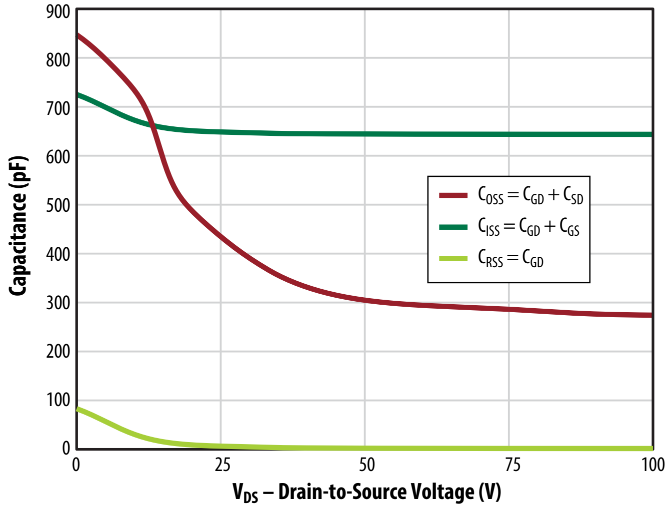


Figure 5b: Capacitance (Log Scale)

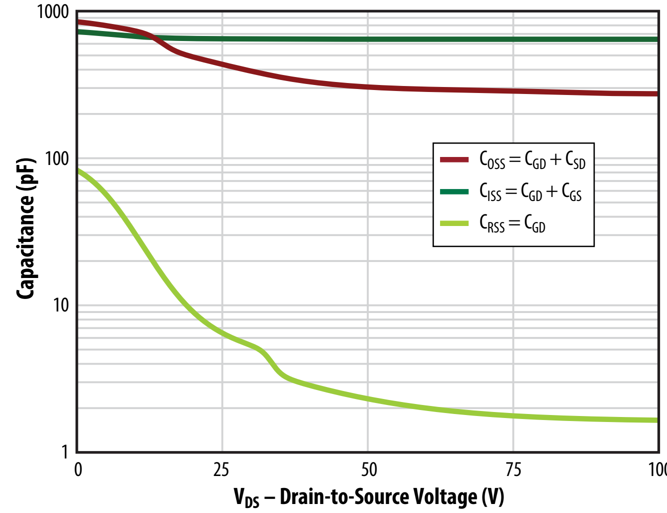


Figure 6: Output Charge and C_{OSS} Stored Energy

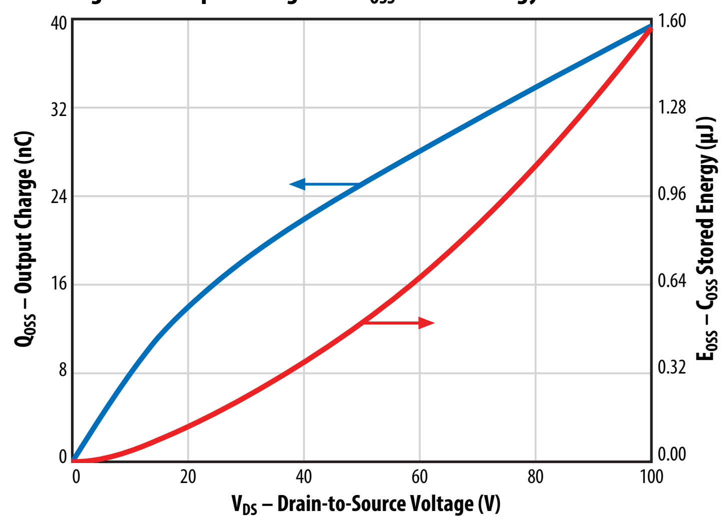


Figure 7: Gate Charge

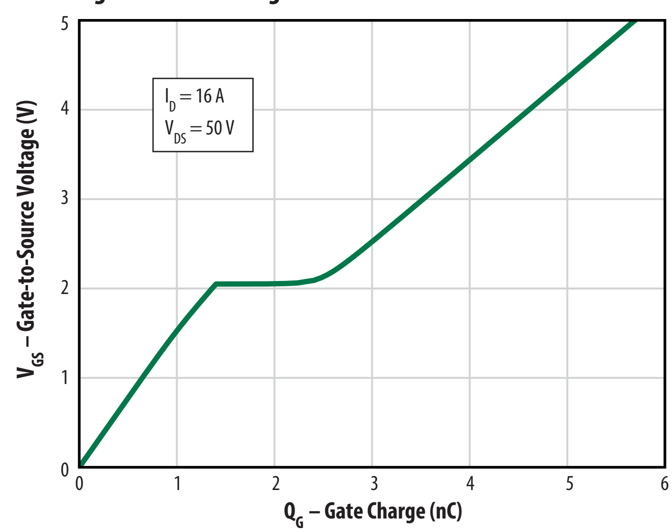


Figure 8: Reverse Drain-Source Characteristics

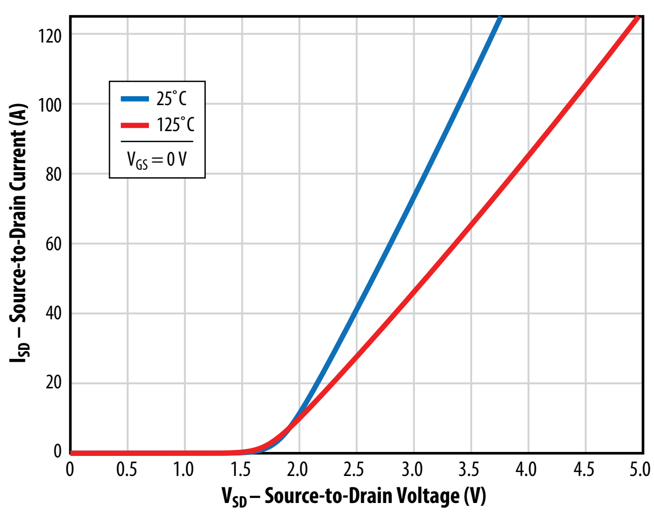


Figure 9: Normalized On-State Resistance vs. Temperature

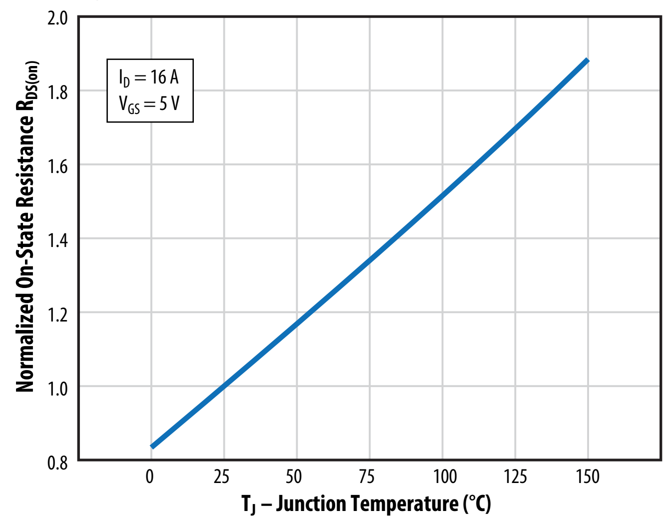


Figure 10: Normalized Threshold Voltage vs. Temperature

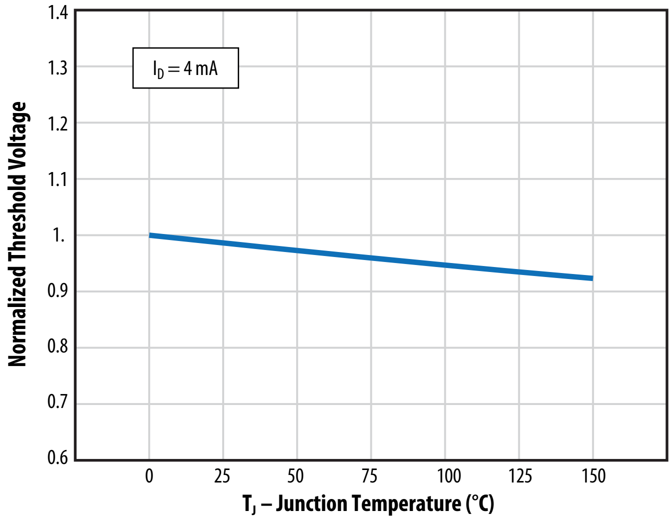
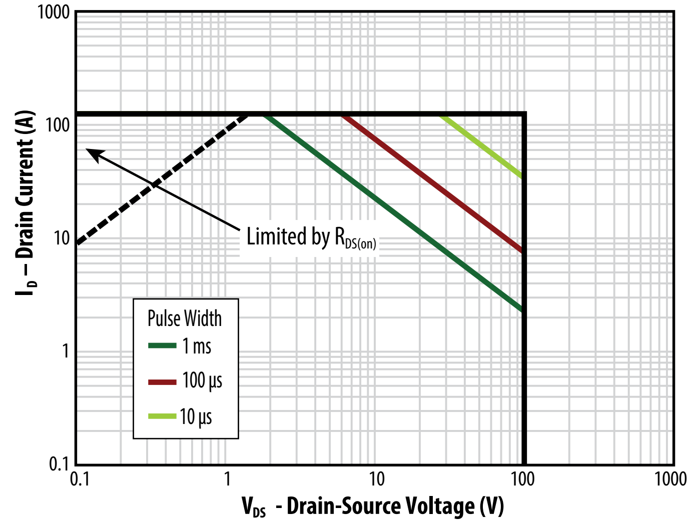


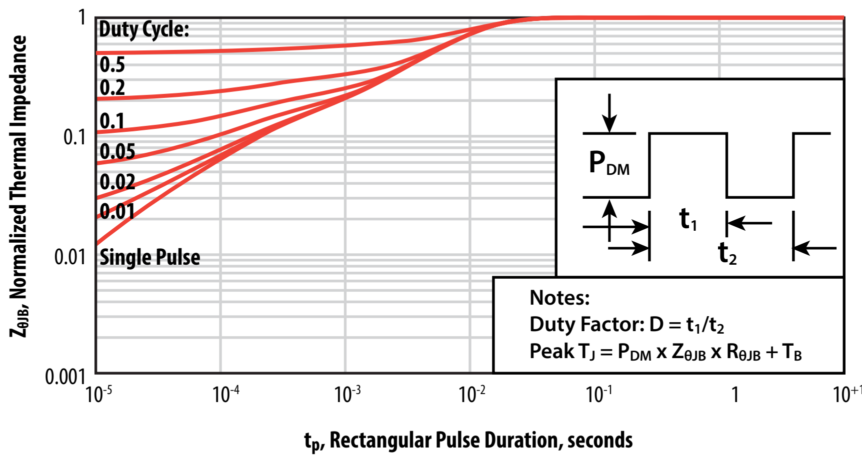
Figure 11: Safe Operating Area



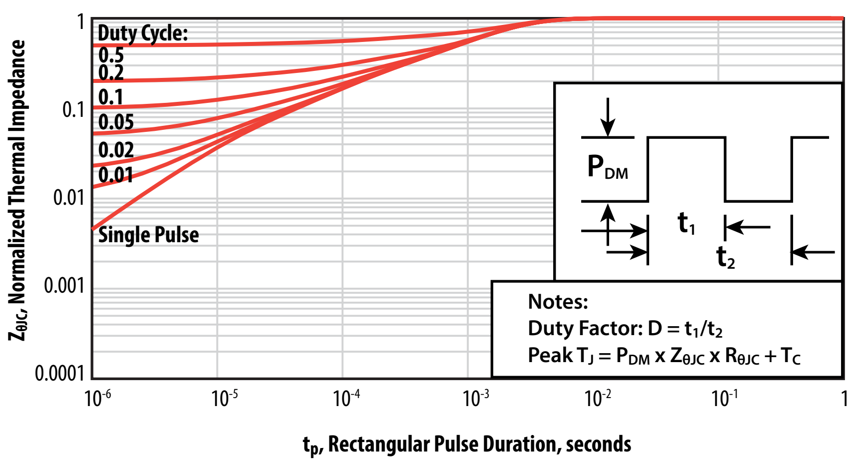
T_J = Max Rated, T_C = +25°C, Single Pulse

Figure 12: Transient Thermal Response Curves

Junction-to-Board



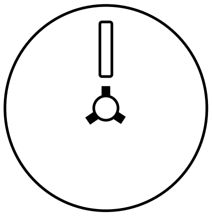
Junction-to-Case

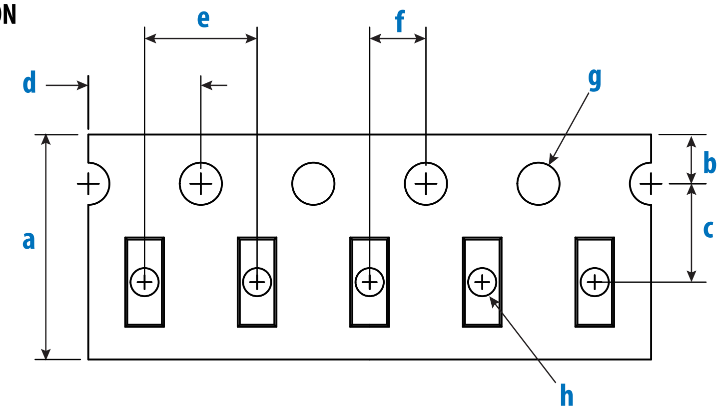


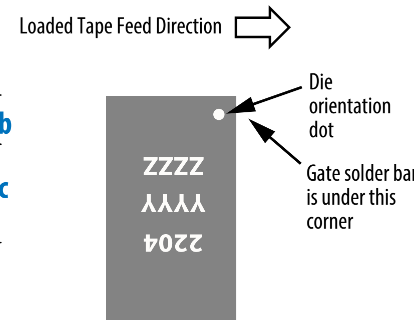
TAPE AND REEL CONFIGURATION

4 mm pitch, 8 mm wide tape on 7" reel

7" inch reel







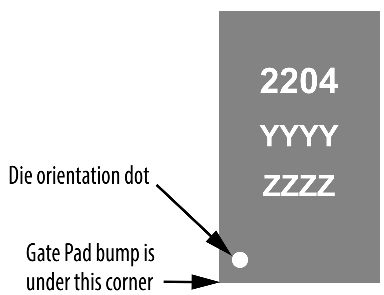
Die is placed into pocket solder bump side down (face side down)

	Dimension (mm)		
EPC2204 (Note 1)	Target	MIN	MAX
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (Note 2)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60
h	0.50	0.45	0.55

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

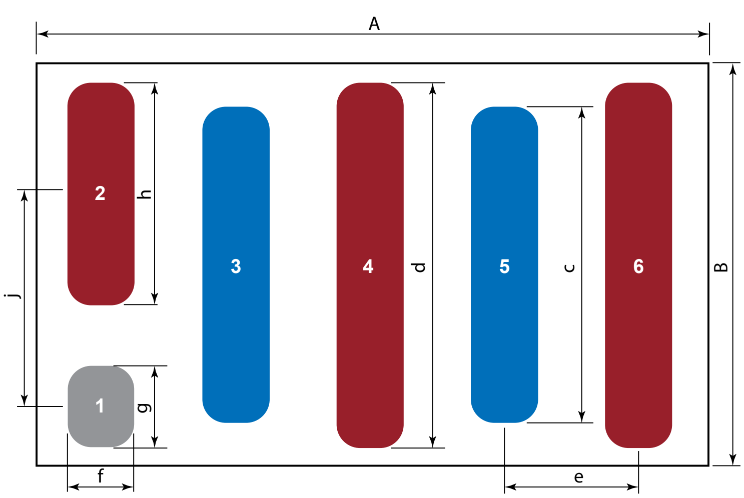
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2204	2204	YYYY	ZZZZ

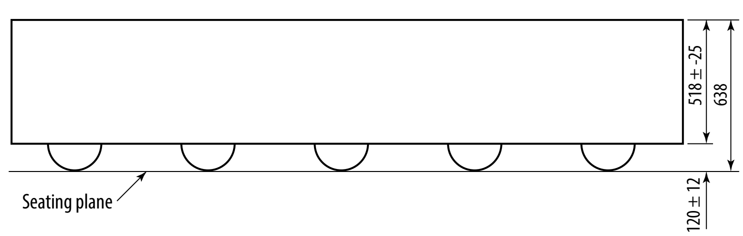
DIE OUTLINE

Solder Bump View



DIM	Micrometers		
	MIN	Nominal	MAX
A	2470	2500	2530
B	1470	1500	1530
c		1175	
d		1350	
e		500	
f		250	
g		300	
h		825	
j		787.5	

Side View

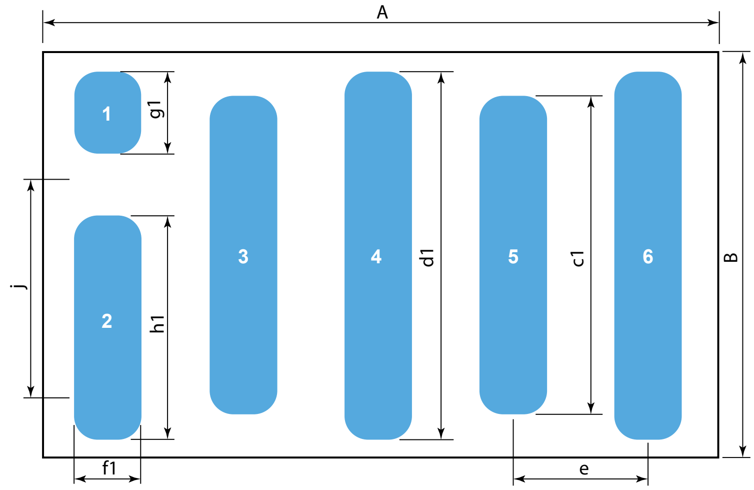


Pad 1 is Gate;

Pads 2 ,4, 6 are Source;

Pads 3, 5 are Drain

RECOMMENDED LAND PATTERN
(units in µm)

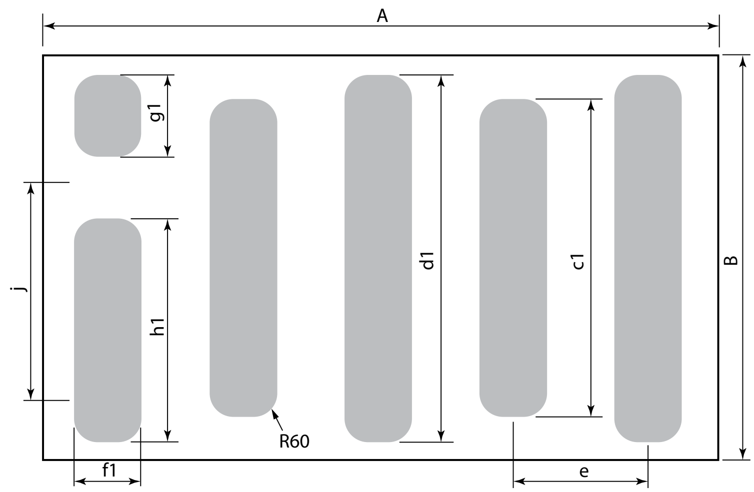


Land pattern is solder mask defined
Solder mask opening is 180 µm
It is recommended to have on-Cu trace PCB vias

Pad 1 is Gate;
Pads 2 ,4, 6 are Source;
Pads 3, 5 are Drain

DIM	Nominal
A	2500
B	1500
c1	1155
d1	1330
e	500
f1	230
g1	280
h1	805
j	787.5

RECOMMENDED STENCIL DRAWING
(units in µm)



DIM	Nominal
A	2500
B	1500
c1	1155
d1	1330
e	500
f1	230
g1	280
h1	805
j	787.5

Recommended stencil should be 4 mil (100 µm) thick, must be laser cut, openings per drawing.

The corner has a radius of R60.

Intended for use with SAC305 Type 3 solder, reference 88.5% metals content.

Split stencil design can be provided upon request, but EPC has tested this stencil design and not found any scooping issues.

Additional assembly resources available at https://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx

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Information subject to change without notice.
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