

Dual N-Channel 60 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY	
V _{DS} (V)	60
R _{DS(on)} (Ω) at V _{GS} = 10 V	0.028
R _{DS(on)} (Ω) at V _{GS} = 4.5 V	0.030
I _D (A) per leg	7
Configuration	Dual

FEATURES

- TrenchFET® power MOSFET
- 100 % R_G and UIS tested



RoHS
COMPLIANT
HALOGEN
FREE



ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	60	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current	I _D	T _C = 25 °C	7
		T _C = 125 °C	4
Continuous Source Current (Diode Conduction) ^a	I _S	3.6	A
Pulsed Drain Current ^b	I _{DM}	28	
Single Pulse Avalanche Current	I _{AS}	18	
Single Pulse Avalanche Energy	E _{AS}	16.2	mJ
Maximum Power Dissipation ^b	P _D	T _C = 25 °C	4
		T _C = 125 °C	1.3
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +175	°C

THERMAL RESISTANCE RATINGS			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient	R _{thJA}	110	°C/W
Junction-to-Foot (Drain)	R _{thJF}	34	

Notes

- Package limited.
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- When mounted on 1" square PCB (FR4 material).

SPECIFICATIONS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		60	-	-	V
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		1.5	2.0	2.5	
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}$	$V_{DS} = 60\text{ V}$	-	-	1	μA
		$V_{GS} = 0\text{ V}$	$V_{DS} = 60\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	50	
		$V_{GS} = 0\text{ V}$	$V_{DS} = 60\text{ V}, T_J = 175\text{ }^\circ\text{C}$	-	-	150	
On-State Drain Current ^a	$I_{D(on)}$	$V_{GS} = 10\text{ V}$	$V_{DS} \geq 5\text{ V}$	20	-	-	A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 4.5\text{ A}$	-	0.028	-	Ω
		$V_{GS} = 10\text{ V}$	$I_D = 4.5\text{ A}, T_J = 125\text{ }^\circ\text{C}$	-	0.066	-	
		$V_{GS} = 10\text{ V}$	$I_D = 4.5\text{ A}, T_J = 175\text{ }^\circ\text{C}$	-	0.081	-	
		$V_{GS} = 4.5\text{ V}$	$I_D = 4\text{ A}$	-	0.030	-	
Forward Transconductance ^f	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 4.5\text{ A}$		-	15	-	S
Dynamic ^b							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 25\text{ V}, f = 1\text{ MHz}$	-	600	750	μF
Output Capacitance	C_{oss}			-	110	140	
Reverse Transfer Capacitance	C_{rss}			-	50	62	
Total Gate Charge ^c	Q_g	$V_{GS} = 10\text{ V}$	$V_{DS} = 30\text{ V}, I_D = 5.3\text{ A}$	-	11.7	18	nC
Gate-Source Charge ^c	Q_{gs}			-	1.8	2.7	
Gate-Drain Charge ^c	Q_{gd}			-	2.8	4.2	
Gate Resistance	R_g	$f = 1\text{ MHz}$		1.3	-	6	Ω
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = 30\text{ V}, R_L = 6.8\text{ }\Omega$ $I_D \cong 4.4\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		-	7	11	ns
Rise Time ^c	t_r			-	3.3	5	
Turn-Off Delay Time ^c	$t_{d(off)}$			-	22.4	33.5	
Fall Time ^c	t_f			-	2.1	3.2	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed Current ^a	I_{SM}			-	-	28	A
Forward Voltage	V_{SD}	$I_F = 2\text{ A}, V_{GS} = 0\text{ V}$		-	0.75	1.1	V

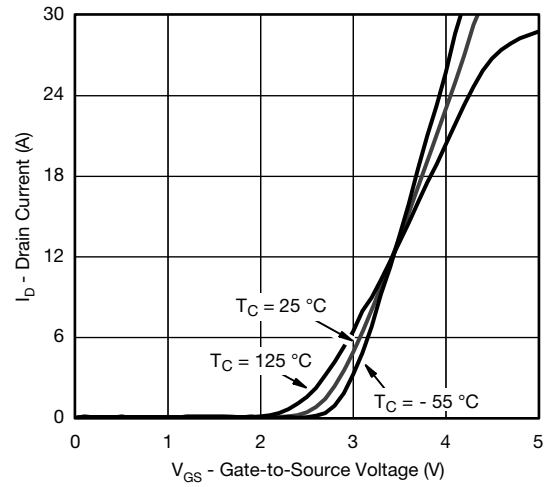
Notes

- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

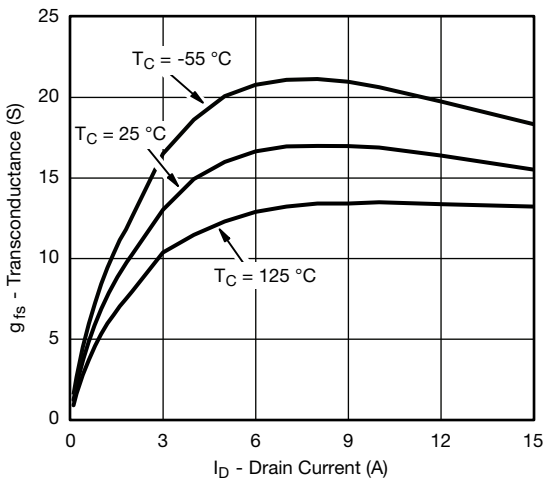
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Output Characteristics



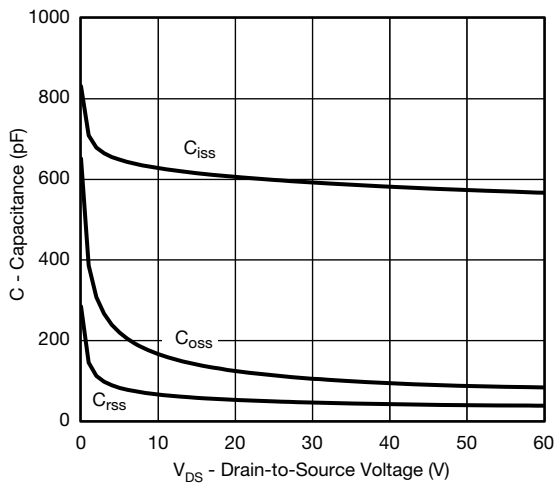
Transfer Characteristics



Transconductance



On-Resistance vs. Drain Current



Capacitance



Gate Charge

TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



On-Resistance vs. Junction Temperature



Drain Source Breakdown vs. Junction Temperature



Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

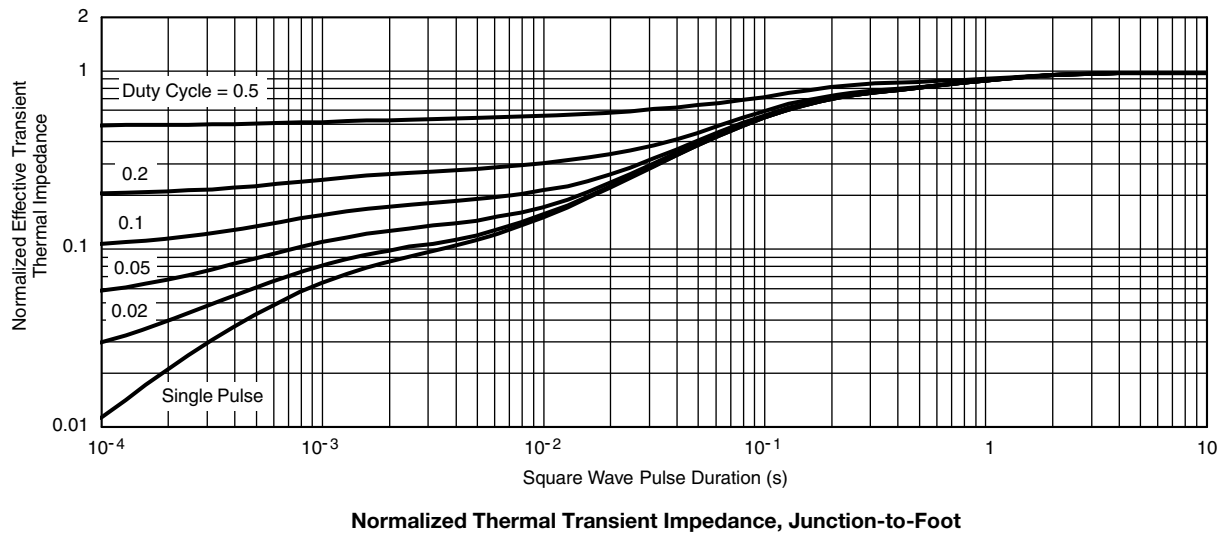


Threshold Voltage

THERMAL RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



THERMAL RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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