ft2128

3.4W Class-D Audio Power Amplifier with Dual Modes of Automatic Level Control

GENERAL DESCRIPTION

The ft2128 is a high-efficiency, high-performance, Class-D audio power amplifier with dual modes of automatic level control (ALC). It operates from 3V to 5.5V supply. When powered with 5V supply voltage, it is capable of delivering a continuous average output of 3.4W into 3Ω load or 2.8W into 4Ω load with 4% THD+N.

The ft2128 features ALC to constantly monitor and safeguard the audio output signals against clipping. Once an over-level condition, caused by either the over-level input signals or low battery supply voltage, is detected, the ALC adjusts the voltage gain of the amplifiers to minimize output clipping while maintaining a maximally-allowed dynamic range of the audio output signals. While minimizing output clipping distortion, the ALC also helps prevent excessive power dissipation and protect speakers.

As a Class-D audio power amplifier, the ft2128 features high efficiency up to 90%, which make the device ideal for use in battery-powered portable devices. Also, the ft2128 incorporates shutdown mode to minimize power consumption and comprehensive protection features against various operating faults for a safe and reliable operation.

FEATURES

- Wide supply voltage range from 3V to 5.5V
- Filterless Class-D operation
- Automatic level control to eliminate output clipping
- Dual ALC modes of operation
- High efficiency up to 90%
- Constant output power at 5V supply (ALC-1)
  - 3.2W (3Ω load, 1% THD+N)
  - 2.6W (4Ω load, 1% THD+N)
  - 1.4W (8Ω load, 1% THD+N)
- Constant output power at 5V supply (ALC-2)
  - 3.4W (3Ω load, 4% THD+N)
  - 2.8W (4Ω load, 4% THD+N)
  - 1.5W (8Ω load, 4% THD+N)
- ALC Range: 12dB
- Low quiescent current: 3mA @ V_{DD}=3.6V
- Analog or digital scheme to set ALC operating mode
- Short-circuit & thermal overload protection
- Available in SOP-8L & MSOP-8L packages

APPLICATIONS

- Portable navigation devices
- Multimedia internet devices
- Portable or Blue-tooth speakers

APPLICATION CIRCUIT

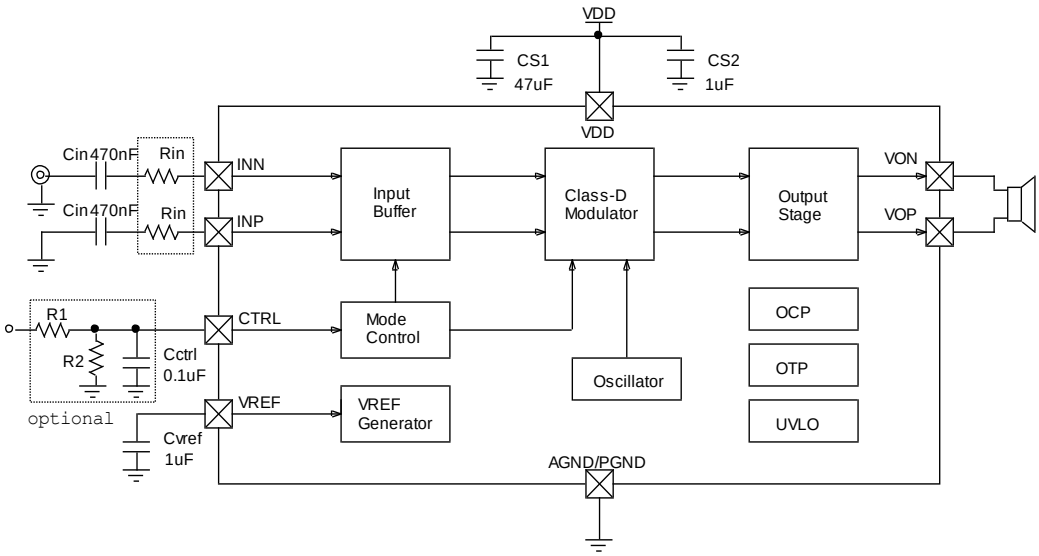
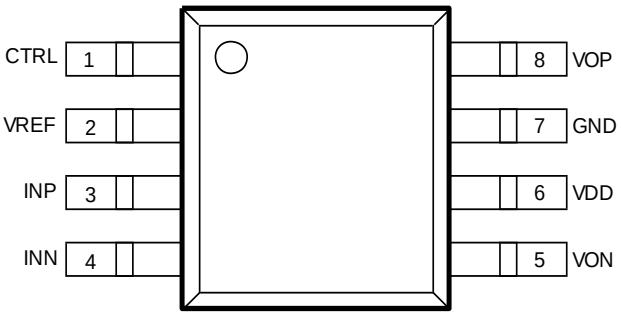
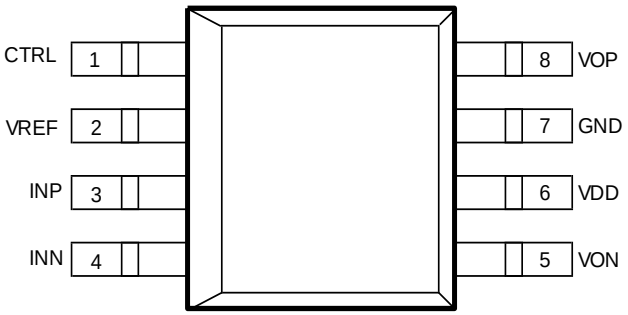


Figure 1: Typical Application Circuit Diagram

PIN CONFIGURATION AND DESCRIPTION



ft2128M (MSOP-8L)
(TOP VIEW)



ft2128P (SOP-8L)
(TOP VIEW)

PIN NAME	PIN #	TYPE	DESCRIPTION
CTRL	1	DI	Shutdown and operating mode control.
VREF	2	AO	Analog reference at VDD/2, the common-mode bias for audio inputs. Place a bypass capacitor of 1μF to ground for noise injection.
INP	3	AI	Positive audio input terminal.
INN	4	AI	Negative audio input terminal.
VON	5	AO	Negative BTL audio output terminal.
VDD	6	P	Power supply.
GND	7	G	Power ground.
VOP	8	AO	Positive BTL audio output terminal.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ft2128P	-40°C to +85°C	SOP-8L
ft2128M	-40°C to +85°C	MSOP-8L

ABSOLUTE MAXIMUM RATINGS (Note 1)

PARAMETER	UNIT
Supply Voltage	-0.3V to 6.0V
All other Pins	-0.3V to V_{DD}+0.3V
Power Dissipation	Internally Limited
Junction Temperature	150°C
Solder Information Vapor Phase (60 sec.) Infrared (15 sec.)	 215°C 220°C
Storage Temperature	−45°C to +150°C

Note 1: Stresses beyond those listed under absolute maximun ratings may cause permanent damage to the device. These are stress ratings only,and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied.Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PACKAGE DISSIPATION RATINGS

PACKAGE	Θ_{JA}	UNIT
SOP-8L	140	°C/W
MSOP-8L	180	°C/W

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage，V_{DD}		3.0		5.5	V
Operating Free-Air Temperature, T_A		-40		85	°C
Minimum Load Resistance, R_{LOAD}		2.6			Ω

IMPORTANT APPLICATION NOTES

1. The ft2128, as a high performance Class-D audio amplifier, requires adequate power supply decoupling to ensure its optimum operation and performance in output power, efficiency, THD+N, and EMI emissions. Place decoupling capacitors as close to the VDD pin as possible. For applications where the load resistance is less than 6Ω, it is strongly recommended to use a 47μF or larger capacitor for power supply decoupling.
2. It is recommended to employ a ground (GND) plane for ft2128 on the system board.
3. Use a simple ferrite bead filter for further EMI suppression. Choose a ferrite bead with a rated current no less than 2A or greater for applications with a load resistance less than 6Ω. Also, place the respective ferrite beard filters as close to the output pins, VOP and VON, as possible.
4. For applications where the power supply is rated more than 4.6V or the load resistance less than 6Ω, it is strongly recommended to add a simple snubber circuit, as depicted in Figure 41, between the two output pins, VOP and VON, to prevent the device from accelerated deterioration or abrupt destruction due to excessive inductive flybacks that are induced on fast output switching or by an over-current or short-circuit condition.

ELECTRICAL CHARACTERISTICS

V_{DD}=5V, T_A=25°C, R_{IN}=10KΩ, C_{IN}=0.47μF, A_V=21.6dB, f=1kHz, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Supply Voltage		3.0		5.5	V
V_{UVLU}	Power-up Threshold Voltage	V_{DD} from Low to High		2.2		V
V_{UVLD}	Power-off Threshold Voltage	V_{DD} from High to Low		2.0		V
I_{DD}	Power Supply Quiescent Current Inputs AC-Grounded	V_{DD}=5V, No Load		3.5	5.0	mA
		V_{DD}=3.6V, No Load		3.0	4.2	mA
I_{SD}	Shutdown Current	CTRL Low		0.1		μA
$P_{O, ALC1}$	Constant Output Power (ALC-1) Load=8Ω	V_{IN}=0.6V_{RMS}, V_{DD}=5V		1.45		W
		V_{IN}=0.4V_{RMS}, V_{DD}=3.6V		0.75		W
	Constant Output Power (ALC-1) Load=4Ω	V_{IN}=0.6V_{RMS}, V_{DD}=5V		2.6		W
		V_{IN}=0.4V_{RMS}, V_{DD}=3.6V		1.3		W
	Constant Output Power (ALC-1) Load=3Ω	V_{IN}=0.6V_{RMS}, V_{DD}=5V		3.2		W
		V_{IN}=0.4V_{RMS}, V_{DD}=3.6V		1.6		W
$P_{O, ALC2}$	Constant Output Power (ALC-2) Load=8Ω	V_{IN}=0.6V_{RMS}, V_{DD}=5V		1.55		W
		V_{IN}=0.4V_{RMS}, V_{DD}=3.6V		0.8		W
	Constant Output Power (ALC-2) Load=4Ω	V_{IN}=0.6V_{RMS}, V_{DD}=5V		2.8		W
		V_{IN}=0.4V_{RMS}, V_{DD}=3.6V		1.4		W
	Constant Output Power (ALC-2) Load=3Ω	V_{IN}=0.6V_{RMS}, V_{DD}=5V		3.4		W
		V_{IN}=0.4V_{RMS}, V_{DD}=3.6V		1.7		W
A_V	Overall Voltage Gain	R_{IN}=0Ω		27.6		dB
		R_{IN}=10KΩ		21.6		dB
Z_{IN}	Input Impedance			10		KΩ
Z_{OUT}	Output Impedance	CTRL Low		2		KΩ
V_{REF}	VREF Voltage	V_{DD}=5V		V_{DD} /2		V
THD+N	Total Harmonic Distortion+Noise	Po=0.5W，R_L=8Ω		0.3		%
		Po=1.0W，R_L=4Ω		0.2		%
V_{OS}	Output Offset Voltage	No Load		±10		mV
V_N	Output Voltage Noise	f=20Hz to 20kHz, A_V=21.6dB Inputs AC-Grounded		100		μV_{RMS}
η	Power Efficiency	V_{DD}=5V，Po=1W，R_L=8Ω		90		%
PSRR	Power Supply Rejection Ratio	f=1kHz		50		dB
CMRR	Common Mode Rejection Ratio	f=1kHz, A_V=27.6dB		60		dB
SNR	Signal-to-Noise Ratio			85		dB
A_{MAX}	Maximum ALC Attenuation			12		dB
ALC Mode Control (Voltage Setting)						
V_{ALC2}	ALC-2 Mode Threshold		1.6			V
V_{ALC1}	ALC-1 Mode Threshold		1.0		1.4	V
V_{SD}	Shutdown Mode Threshold				0.4	V
T_{SD}	Shutdown Mode Settling Time			10		ms

ELECTRICAL CHARACTERISTICS (Cont'd)

V_{DD}=5V, T_A=25°C, R_{IN}=10KΩ, C_{IN}=0.47μF, A_V=21.6dB, f=1kHz, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
ALC Mode Control (One-Wire Interface)						
V_H	Digital Logic High		1.6			V
V_L	Digital Logic Low				0.4	V
T_{LO}	Time of CTRL Low		1		10	μs
T_{HI}	Time of CTRL High		1			μs
T_{SHDN}	Time for Shutdown, Active Low		15			ms
I_{LIMIT}	Over-Current Limit	V_{DD}=3.6V		1.8		A
		V_{DD}=4.2V		2.1		A
		V_{DD}=5V		2.6		A
T_{OTP}	Over-Temperature Threshold			160		°C
T_{HYS}	Over-Temperature Hysteresis			25		°C
T_{STUP}	Startup Time			120		ms
T_{ATT}	Attack Time			64		ms
T_{REL}	Release Time			840		ms
f_{SW}	PWM Carrier Frequency			450		kHz

TYPICAL PERFORMANCE CHARACTERISTICS

T_A=25°C, R_{IN}=10KΩ, C_{IN}=0.47μF, A_V=21.6dB, f=1kHz, unless otherwise specified.

List of Performance Characteristics

DESCRIPTION	CONDITIONS	FIGURE #
Output Power vs. Supply Voltage	R_L=8Ω+33μH, ALC-1 & ALC-2 Mode (Vin=0.5V_{RMS})	2
	R_L=4Ω+33μH, ALC-1 & ALC-2 Mode (Vin=0.5V_{RMS})	3
Output Power vs. Input Voltage	V_{DD}=5V, R_L=8Ω+33μH, ALC-1 & ALC-2 Mode	4
	V_{DD}=5V, R_L=4Ω+33μH, ALC-1 & ALC-2 Mode	5
	V_{DD}=3.6V, R_L=8Ω+33μH, ALC-1 & ALC-2 Mode	6
	V_{DD}=3.6V, R_L=4Ω+33μH, ALC-1 & ALC-2 Mode	7
Efficiency vs. Output Power	V_{DD}=5V, R_L=8Ω+33μH, ALC-2 Mode	8
	V_{DD}=5V, R_L=4Ω+33μH, ALC-2 Mode	9
	V_{DD}=3.6V, R_L=8Ω+33μH, ALC-2 Mode	10
	V_{DD}=3.6V, R_L=4Ω+33μH, ALC-2 Mode	11
THD+N vs. Output Power	V_{DD}=5V, f=1kHz, R_L=8Ω+33μH, ALC-2 Mode	12
	V_{DD}=5V, f=1kHz, R_L=4Ω+33μH, ALC-2 Mode	13
	V_{DD}=3.6V, f=1kHz, R_L=8Ω+33μH, ALC-2 Mode	14
	V_{DD}=3.6V, f=1kHz, R_L=4Ω+33μH, ALC-2 Mode	15
THD+N vs. Input Voltage	V_{DD}=5V, f=1kHz, R_L=8Ω+33μH, ALC-1 & ALC-2 Mode	16
	V_{DD}=5V, f=1kHz, R_L=4Ω+33μH, ALC-1 & ALC-2 Mode	17
	V_{DD}=3.6V, f=1kHz, R_L=8Ω+33μH, ALC-1 & ALC-2 Mode	18
	V_{DD}=3.6V, f=1kHz, R_L=4Ω+33μH, ALC-1 & ALC-2 Mode	19
THD+N vs. Input Frequency	V_{DD}=5V, Po=0.8W, R_L=8Ω+33μH, ALC-1 Mode	20
	V_{DD}=5V, Po=1.6W, R_L=4Ω+33μH, ALC-1 Mode	21
	V_{DD}=3.6V, Po=0.4W, R_L=8Ω+33μH, ALC-1 Mode	22
	V_{DD}=3.6V, Po=0.8W, R_L=4Ω+33μH, ALC-1 Mode	23
PSRR vs. Input Frequency	V_{DD}=5V, R_L=8Ω+33μH, Input AC-Grounded, ALC-2 Mode	24
	V_{DD}=5V, R_L=4Ω+33μH, Input AC-Grounded, ALC-2 Mode	25
	V_{DD}=3.6V, R_L=8Ω+33μH, Input AC-Grounded, ALC-2 Mode	26
	V_{DD}=3.6V, R_L=4Ω+33μH, Input AC-Grounded, ALC-2 Mode	27
Quiescent Current vs. Supply Voltage	Input AC-Grounded, No Load, ALC On, ALC-2 Mode	28
ALC Attack & Release Time	V_{DD}=5V, Vin=0.26V_{RMS} ~ 0.82V_{RMS}, R_L=4Ω+33μH, ALC-1 Mode	29
(VOP-VON) Startup Waveforms	V_{DD}=5V, R_L=4Ω+33μH, ALC-2 Mode	30
(VOP-VON) Shutdown Waveforms	V_{DD}=5V, R_L=4Ω+33μH, ALC-2 Mode	31

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

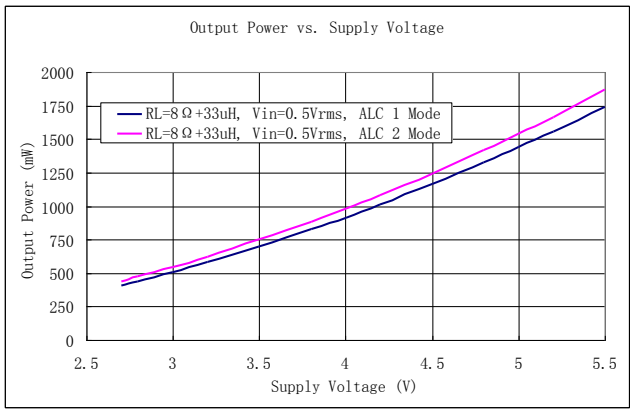


Figure 2: Output Power vs. Supply Voltage

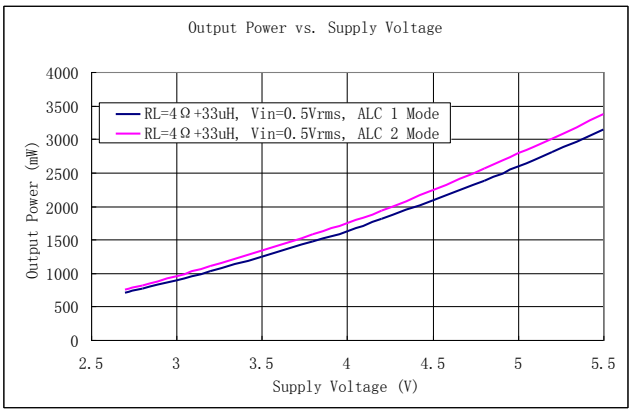


Figure 3: Output Power vs. Supply Voltage

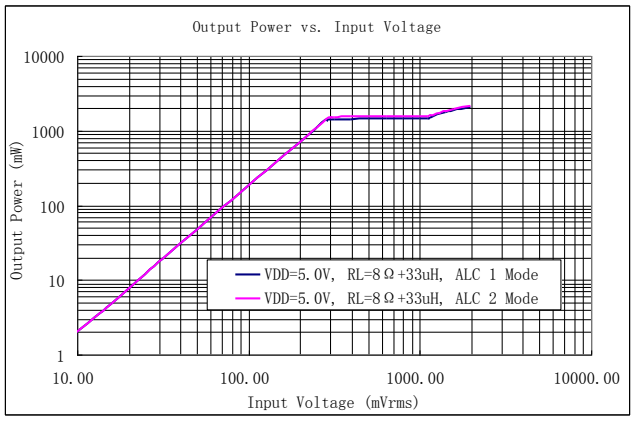


Figure 4: Output Power vs. Input Voltage

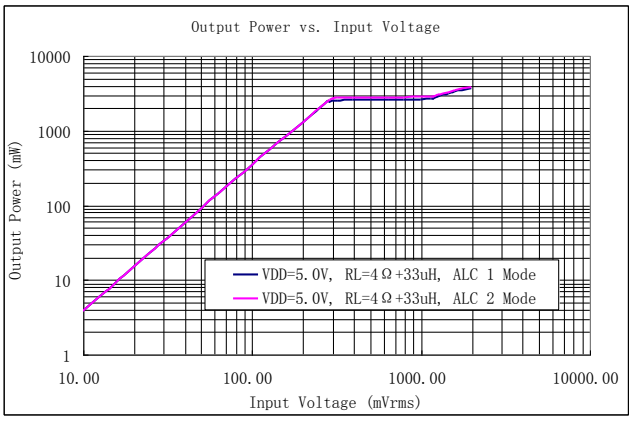


Figure 5: Output Power vs. Input Voltage

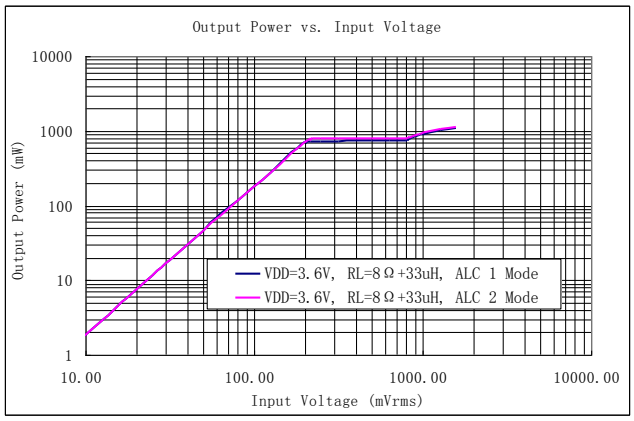


Figure 6: Output Power vs. Input Voltage

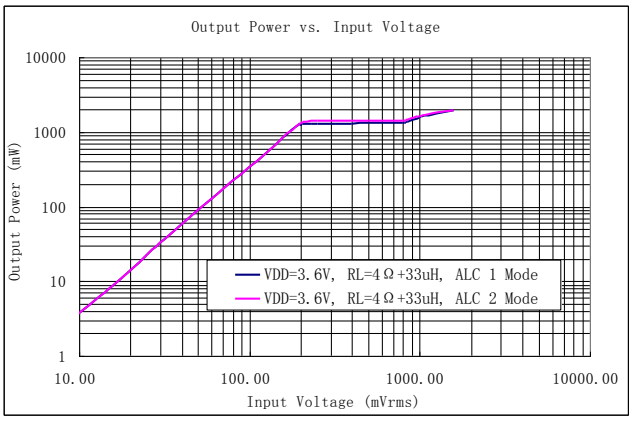


Figure 7: Output Power vs. Input Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

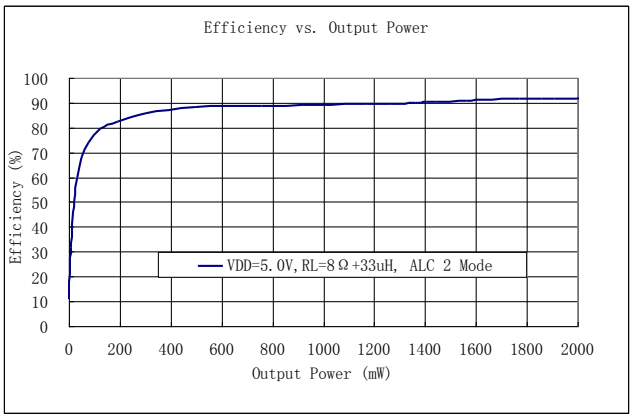


Figure 8: Efficiency vs. Output Power

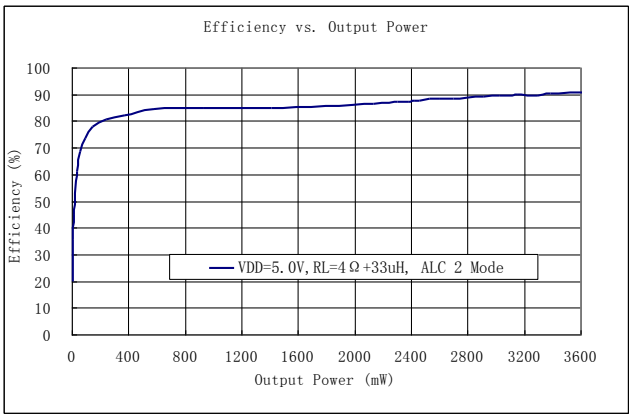


Figure 9: Efficiency vs. Output Power

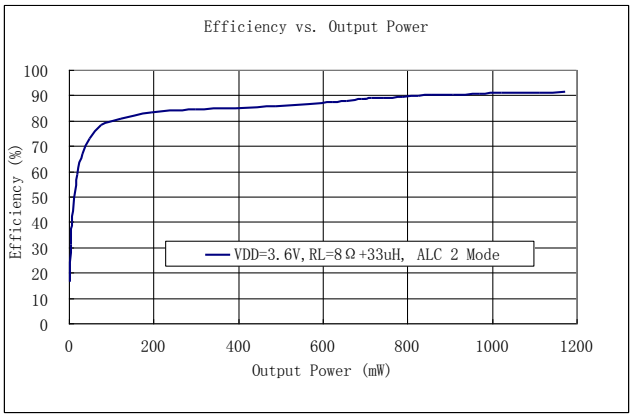


Figure 10: Efficiency vs. Output Power

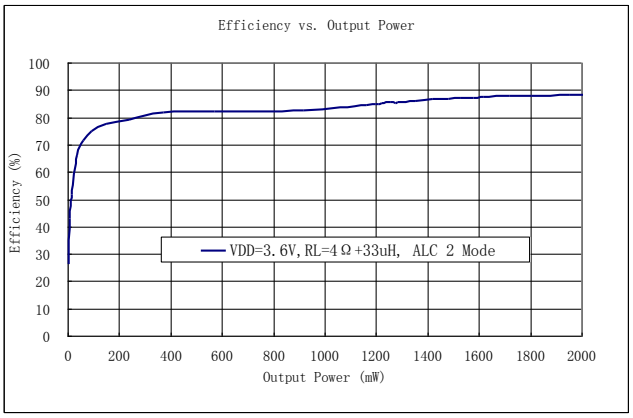


Figure 11: Efficiency vs. Output Power

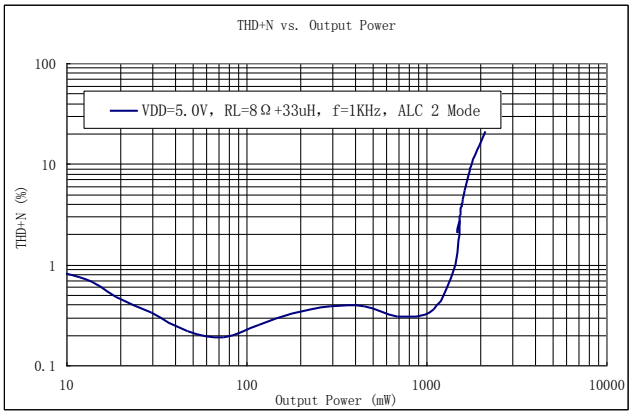


Figure 12: THD+N vs. Output Power

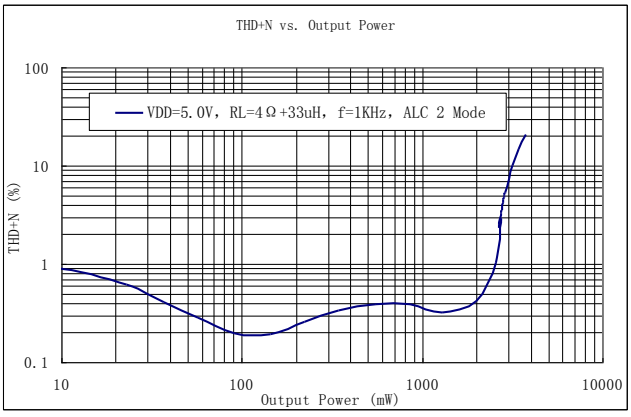


Figure 13: THD+N vs. Output Power

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

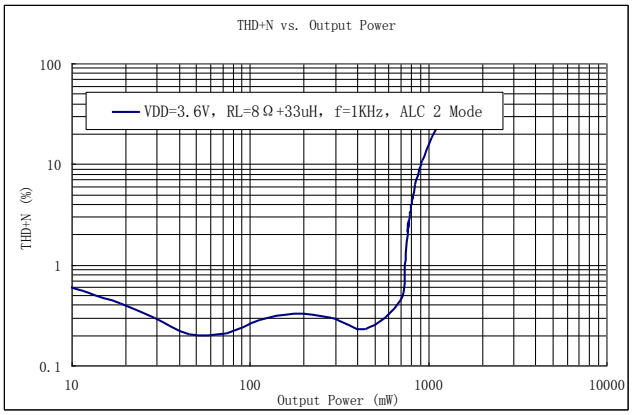


Figure 14: THD+N vs. Output Power

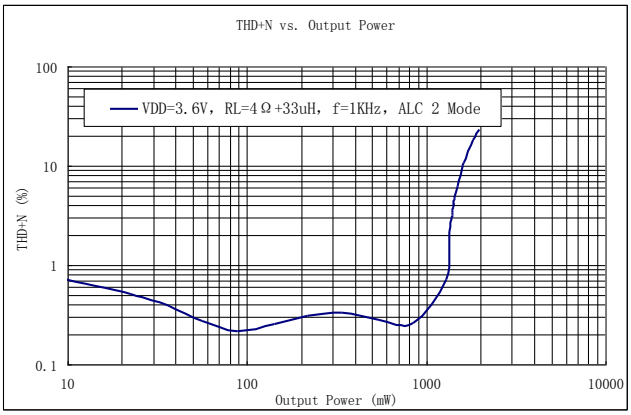


Figure 15: THD+N vs. Output Power

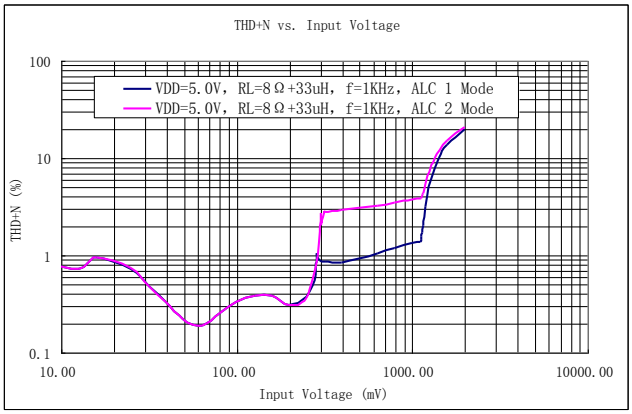


Figure 16: THD+N vs. Input Voltage

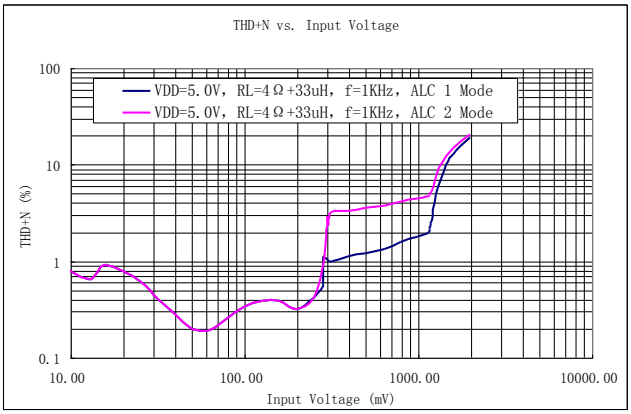


Figure 17: THD+N vs. Input Voltage

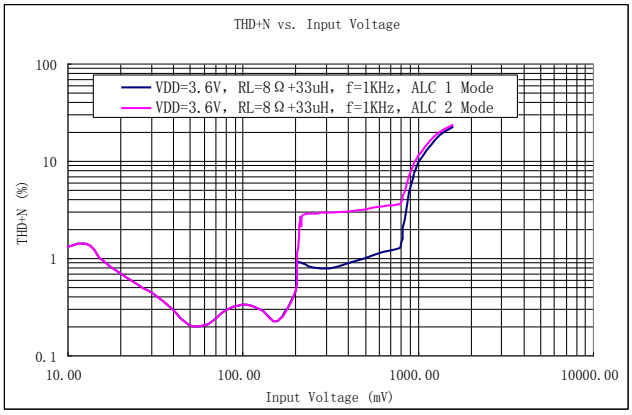


Figure 18: THD+N vs. Input Voltage

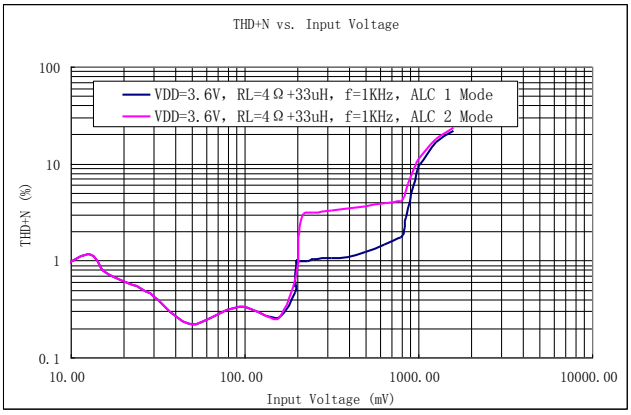


Figure 19: THD+N vs. Input Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

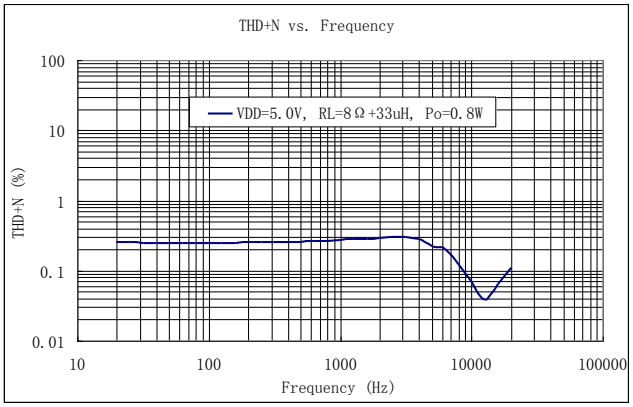


Figure 20: THD+N vs. Frequency

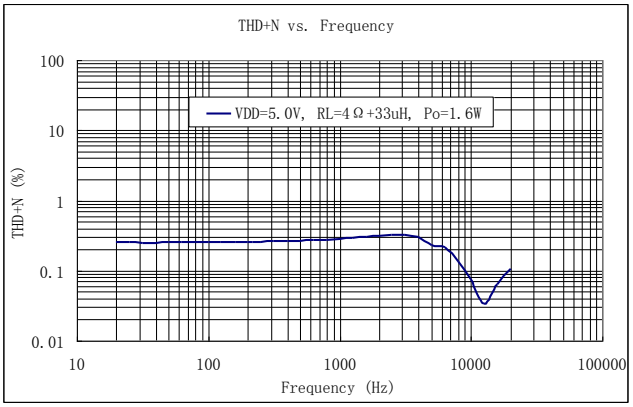


Figure 21: THD+N vs. Frequency

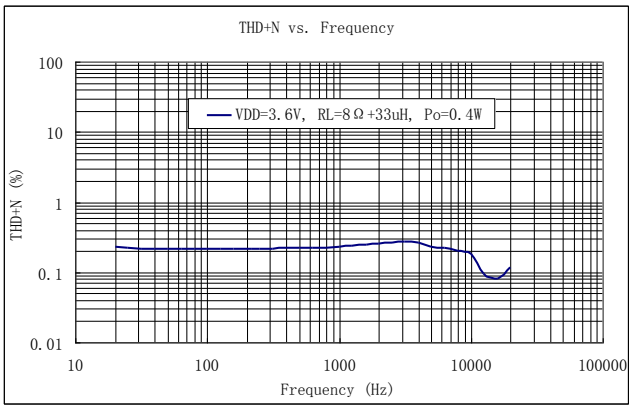


Figure 22: THD+N vs. Frequency

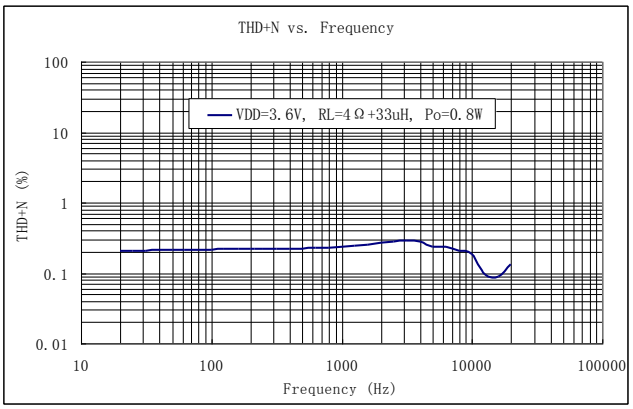


Figure 23: THD+N vs. Frequency

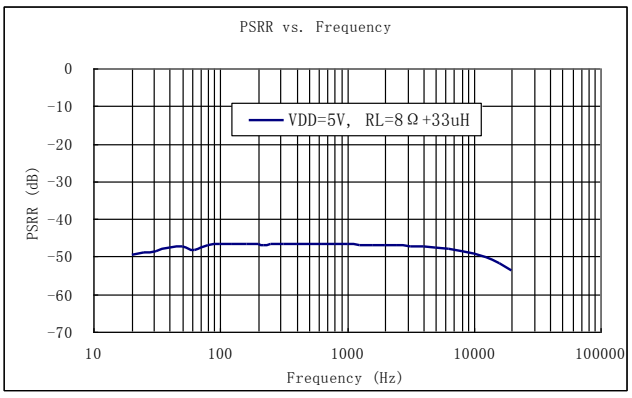


Figure 24: PSRR vs. Frequency

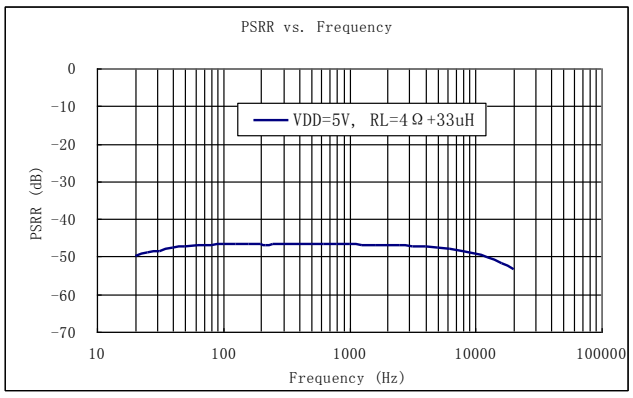


Figure 25: PSRR vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

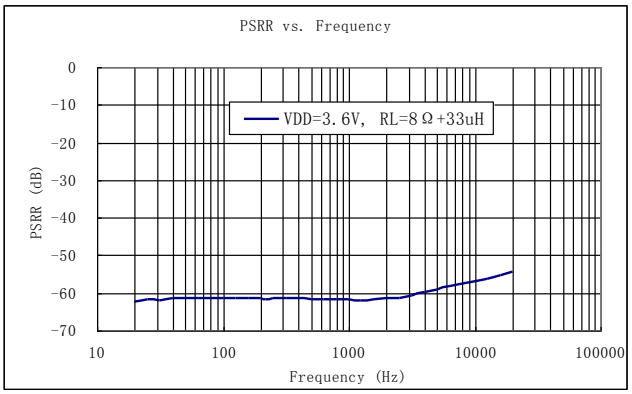


Figure 26: PSRR vs. Frequency

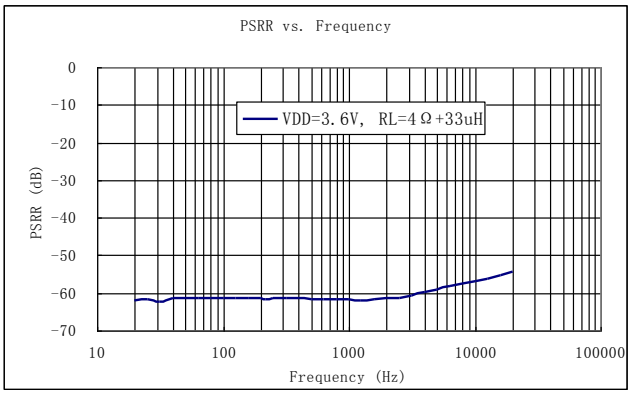


Figure 27: PSRR vs. Frequency

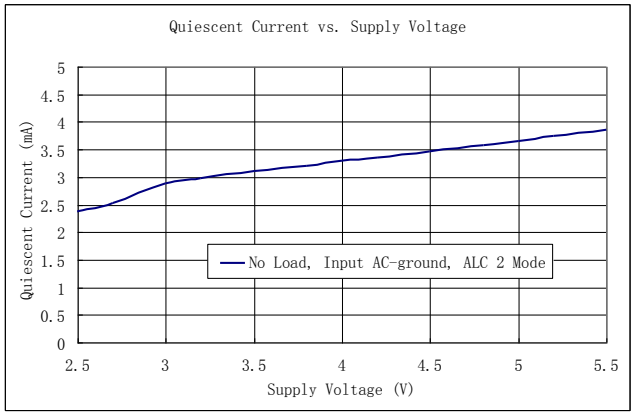


Figure 28: Quiescent Current vs. Supply Voltage

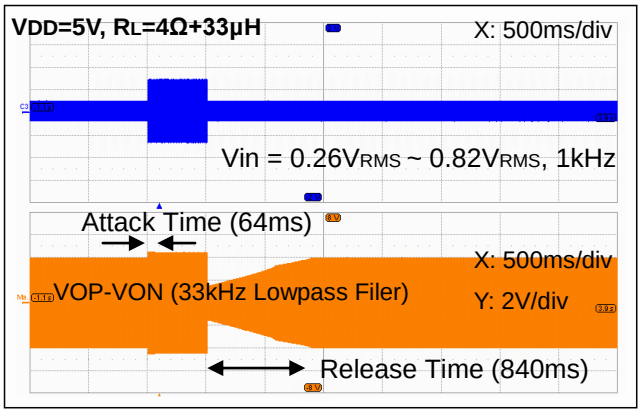


Figure 29: ALC Attack Time & Release Time

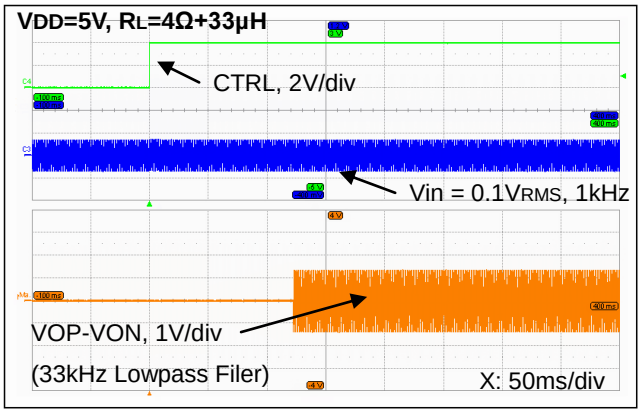


Figure 30: Startup Waveforms

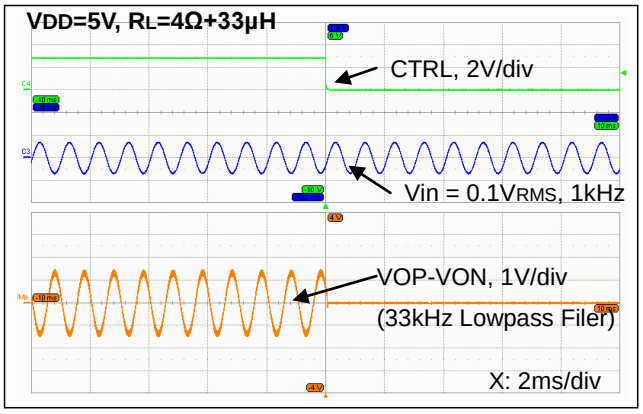


Figure 31: Shutdown Waveforms

APPLICATIONS INFORMATION

The ft2128 is a high-efficiency, high-performance, filterless Class-D audio power amplifier with dual modes of automatic level control (ALC). It operates from 3V to 5.5V supply. When powered with 5V supply voltage, the ft2128 is capable of delivering a continuous average output of 3.2W into 3Ω load or 2.6W into 4Ω load with 1% THD+N, in ALC-1 mode; and 3.4W into 3Ω load or 2.8W into 4Ω load with 4% THD+N, in ALC-2 mode.

The ft2128 features ALC to constantly monitor and safeguard the audio output signals against clipping. Once an over-level condition, caused by either the over-level input signals or low battery supply voltage, is detected, the ALC adjusts the voltage gain of the amplifiers to minimize output clipping while maintaining a maximally-allowed dynamic range of the audio output signals. While minimizing output clipping distortion, the ALC also helps prevent excessive power dissipation and protect speakers. To meet various application requirements, two ALC modes, i.e., ALC-1 and ALC-2, are available in ft2128 for two distinctive audio experiences. In ALC-1 mode, the output clipping is substantially eliminated for ultimate audio quality at the expense of slightly lower output power. In ALC-2 mode, modest output clipping within commonly acceptable audio quality is allowed for higher output power.

In addition, the ft2128 features a filterless PWM modulator that eliminates the need for an external LC filter, therefore reducing the number of external components, the PCB board space, and the system cost. In this manner, the power efficiency is also improved.

As specifically designed for portable applications, the ft2128 incorporates a shutdown mode to minimize power consumption by holding the CTRL pin to ground. It also includes comprehensive protection features against various operating faults such as short-circuit, over-temperature, or under-voltage for a safe and reliable operation.

AUTOMATIC LEVEL CONTROL (ALC)

The automatic level control is to maintain the audio output signals for a maximum voltage swing without distortion when an excessive input that may cause output clipping is applied. With the ALC function, the ft2128 lowers the voltage gain of the amplifier to an appropriate value such that the clipping at the outputs is eliminated. It also eliminates the clipping of the output signal due to the reduction of the power-supply voltage.

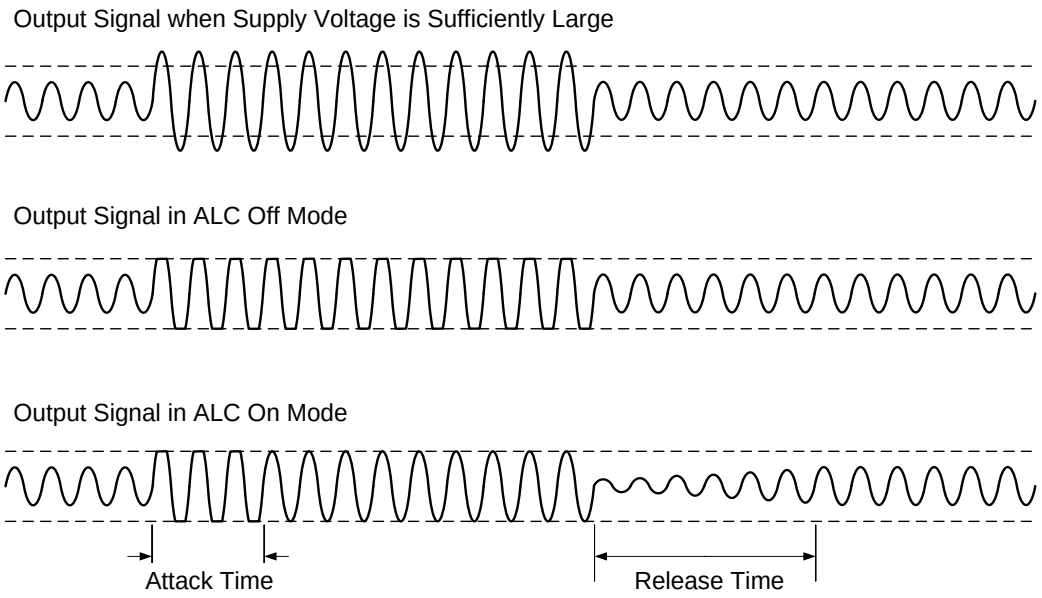


Figure 32: Automatic Level Control Diagram

Table 1 shows the attack time and release time of the ALC mode. The attack time is defined as the time interval required for the gain to fall to its steady-state gain less 3dB approximately, assumed that a sufficiently large input signal is applied. The release time is the time interval required for the amplifier to exit out of the ALC mode of operation.

MODE	ATTACK TIME (ms)	RELEASE TIME (ms)
ALC	64	840

Table 1: ALC Attack Time & Release Time

VOLTAGE GAIN SETTING

The overall voltage gain of the audio amplifier can be externally adjusted by inserting additional input resistors, R_{IN}, in series with the input capacitors. The value of R_{IN} for a given voltage gain can be calculated by Equation 1.

$$A_V = 240 / (R_{IN} + 10) \qquad (1)$$

In Equation 1, A_V is the desired voltage gain of the amplifier and R_{IN} is the internal resistance and expressed in KΩ.

The choice of the overall voltage gain will strongly influence the trade-off between the loudness and the audio quality. The higher the voltage gain is, the louder the listener will experience. However an excessive voltage gain may cause the audio output clipped prematurely for a given range of the input signals. Thus it is crucial to choose an input resistor value resulting in a proper overall voltage gain. The input resistor is chosen based upon various considerations including the supply voltage and the range of input signal levels. Table 2 shows typical resistor values of R_{IN} and the corresponding voltage gains that can be used for various supply voltages and the dynamic range of the input signal levels.

RIN (KΩ)		0	2	5	10	14	20
AV (dB)		27.6	26	24	21.6	20	18
Max. Input Level (V_{RMS}) with ALC in operation	V_{DD}=4.2V	0.50	0.63	0.80	1.0	1.2	1.5
	V_{DD}=5V	0.60	0.75	0.94	1.2	1.5	1.8

Table 2: External Input Resistors Required for Various Voltage Gains

MODE CONTROL

Shutdown and Startup

When the CTRL pin is pulled to ground, the ft2128 is forced into the shutdown mode. In the shutdown mode, all the circuitry is disabled and the supply current is eliminated except leakage current, and the differential outputs are shorted to ground through an internal resistor (2KΩ) individually. Once in the shutdown mode, the CTRL pin must remains low for at least 15ms (T_{SD}), the shutdown settling time, before it can be brought high again. When the CTRL pin is asserted high, the device exits out of the shutdown mode and enters into the ALC mode after a startup time (T_{STUP}) of 64ms.

ALC Mode Control

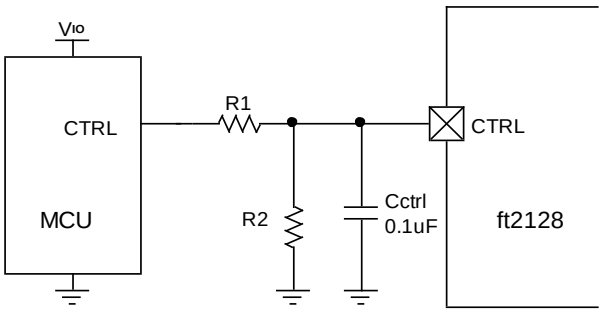
Two ALC operating modes, ALC-1 and ALC-2, are available in ft2128. The ALC-1 mode is intended for the applications where best audio quality is an ultimate design parameter and the output clipping must be substantially eliminated. On the other hand, the ALC-2 mode is for the applications where maximum audio loudness is much desired at the expense of modest output-clipping with THD+N at 4%.

The ALC operation of ft2128 can be configured by either analog (CTRL voltage setting) or digital (a string of digital pulses) scheme. Both schemes are required to interface with a GPIO port from the host via the CTRL pin. The analog scheme configures the ALC operation based upon the voltage at CTRL pin while the digital scheme is based upon the number of low-to-high transitions of digital pulses applied to the CTRL pin.

ALC Mode Control with CTRL Voltage Setting (Analog Scheme)

An example of setting the ALC-1 mode by a host processor or microcontroller is shown in Figure 33. As depicted in the figure, two external resistors (R1, R2 with 1% accuracy) connected to the CTRL pin and GPIO port from the host are used to set the voltage at CTRL pin. It is recommended to add a ceramic capacitor (≥0.1μF) to the CTRL pin to smooth out the mode transition as well as to minimize noise interference.

In Figure 33, "H" indicates a high-level output voltage (V_{IO}) at the host's I/O ports. "L" indicates a low-level output voltage (GND) at the ports. To generate a proper voltage at the CTRL pin for a specific mode of operation, the GPIO port is required to have sufficient pull-down capabilities. Also, the ground (GND) of the host must be at the same potential as that of ft2128. Furthermore, the voltage at CTRL pin is a function of the supply voltage (V_{IO}) applied onto the host. Table 3 defines proper resistor values that can be used for various supply voltages at V_{IO}.



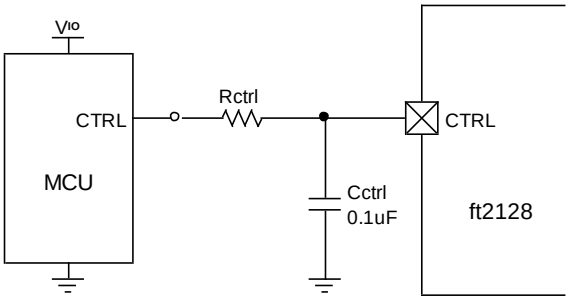
CTRL	MODE
H	ALC-1
L	Shutdown

Figure 33: CTRL Voltage Setting for ALC-1 Operation

V_{IO}	1.8V	2.8V	3.0V	3.3V	4.2V	5.0V
R1	10K	12K	20K	24K	22K	30K
R2	22K	10K	15K	15K	10K	10K

Table 3: Typical Resistors for CTRL Voltage Setting

For applications where ALC-2 operation is desired, the CTRL circuit diagram can be simplified as shown in Figure 34. In this case, one external resistor (Rctrl) and one GPIO port are used to set the voltage at CTRL pin. The value of the resistor is chosen such that the resulting RC time constant (≥1ms) will provide sufficient noise rejection at the CTRL pin.



CTRL	MODE
H	ALC-2
L	Shutdown

Figure 34: CTRL Voltage Setting for ALC-2 Operation

ALC Mode Control with Digital Pulses (Digital Scheme)

To support for a wide range of applications, the ft2128 incorporates digital pulse control to select the ALC operating mode. By applying a string of digital pulses to the CTRL pin, one can select one of the two ALC modes. The detailed timing diagram of the digital pulse control to set the operating mode is shown in Figure 35.

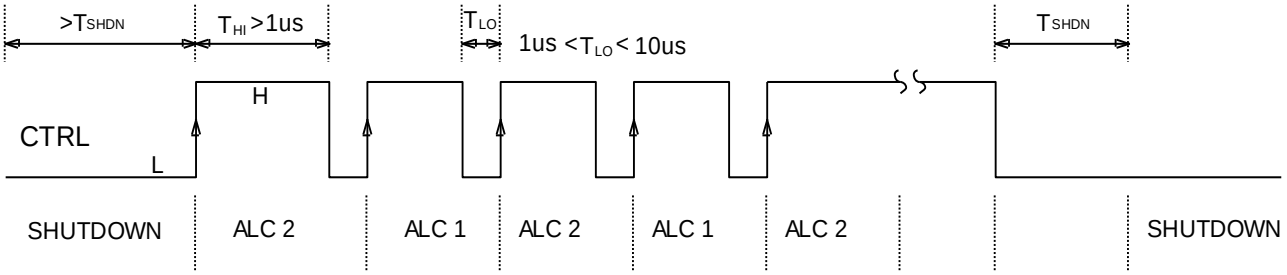


Figure 35: ALC Mode Control with Digital Pulses

Two ALC operating modes, ALC-2 and ALC-1, are configured by the application of a string of pulses onto the CTRL pin. On the first low-to-high transition of the pulses, the device is configured in ALC-2 mode, the default mode. The ALC operating mode can then be toggled in a cyclic manner on each following low-to-high transition of the pulses. Note that each individual high-level or low-level pulse must be longer than a minimum of 1μs to be recognized. Any pulses, high-level or low-level, shorter than 1μs may be ignored. Also, if the CTRL pin is held low for more than 15ms, the device enters into shutdown mode, where all the internal circuitry is de-biased. Once the device is forced into shutdown mode, one or multiple pulses are required for the device to return to its desired mode of operation. For proper operation, do not hold the CTRL pin low for duration between 10μs and 15ms.

CLICK & POP NOISE REDUCTION

The ft2128 incorporates a “click & pop” reduction circuitry to minimize clicks and pops incurred during power-up and power-off, as well as when the device enters into or exists from the shutdown mode. It is however recommended that the CTRL pin be held low during power-up until the supply voltage is stabilized. Similarly, it shall be brought low prior to power-off. In this manner, the click and pop noise can be significantly suppressed.

PROTECTION FEATURES

The ft2128 incorporates various protection functions against possible operating faults for a safe operation. The protection features including Under-Voltage Lockout (UVLO), Short-Circuit Protection (SCP), and Over-Temperature Shutdown (OTSD) are described as follows:

Under Voltage Lockout (UVLO)

The ft2128 incorporates a circuitry to detect a low supply voltage for a safe and reliable operation. When the supply voltage is first applied, the ft2128 will remain inactive until the supply voltage exceeds 2.2V (VUVLU). When the supply voltage is removed and drops below 2.0V (VUVLD), the ft2128 enters into the shutdown mode immediately.

Short-Circuit Protection (SCP)

During operation, the output current flowing through the output stage of the Class-D amplifier is constantly monitored for any over-current and/or short-circuit conditions. Whenever an over-current or short-circuit condition is detected at the differential outputs, either to VDD or VSS or to each other, the amplifier output stage is immediately disabled and the differential outputs are forced into

high-impedance. If this over-current condition persists over a prescribed period, the ft2128 then enters into the shutdown mode and remains in this mode for about 180ms.

Once the shutdown mode times out, the ft2128 will automatically initiate a startup sequence and then check if the short-circuit condition has been removed. If the fault condition is still present, the ft2128 will repeat itself for the process of shutdown followed by a startup sequence, detection, and qualification. It is so-called the hiccup mode of operation. Whenever the fault condition is removed, the ft2128 will automatically restore itself to its normal mode of operation

Over-Temperature Shutdown (OTSD)

When the die temperature exceeds the preset threshold (160°C) for an extended period of 8μs, the device enters into the over-temperature shutdown mode, where two differential outputs are pulled to ground through an internal resistor (2KΩ) individually. The device will resume normal operation once the die temperature returns to a temperature, which is at least 25°C lower than the threshold.

CLASS-D AUDIO AMPLIFIER

As a Class-D audio amplifier, the ft2128 offers much higher efficiency than Class-AB amplifiers. The high efficiency of a Class-D amplifier is due to the switching operation of the output stage. Any power loss associated with the Class-D output stage is mostly due to the I^2R loss of the MOSFET on-resistance and quiescent current overhead.

Fully Differential Amplifier

The ft2128 is a fully differential amplifier with differential inputs and outputs. The fully differential amplifier consists of a differential amplifier and a common-mode amplifier. The differential amplifier ensures that the amplifier outputs a differential voltage on the output that is equal to the differential input times the voltage gain. The common-mode feedback ensures that the common-mode voltage at the output is biased around $V_{DD}/2$ regardless of the common-mode voltage at the input. The fully differential ft2128 can still be used with a single-ended input; however, the ft2128 should be used with differential inputs in a noisy environment, like a wireless handset, to ensure maximum noise rejection.

Low-EMI Filterless Output Stage

Traditional Class-D amplifiers require the use of external LC filters, or shielding, to meet EN55022B electromagnetic-interference (EMI) regulation standards. The ft2128 uses a proprietary edge-rate -controlled (ERC) circuitry to reduce EMI emissions, while maintaining up to 90% efficiency. Above 10MHz, the wideband spectrum looks like noise for EMI purposes.

Filterless Design

Traditional Class-D amplifiers require an output filter to recover the audio signal from the amplifier's output. The filter adds cost, increases the solution size of the amplifier, and can decrease efficiency and THD+N performance. The traditional PWM scheme uses large differential output swings (with its peak-to-peak equal to two times of the supply voltage) and causes large ripple currents. Any parasitic resistance in the filter components results in a loss of power and lowers the efficiency.

The ft2128 does not require an output filter. The device relies on the inherent inductance of the speaker coil and the natural filtering of both the speaker and the human ear to recover the audio component of the square-wave output. Eliminate the output filter results in a smaller, less costly, and more efficient solution.

Because the frequency of its outputs is well beyond the bandwidth of most speakers, voice coil movement due to the square-wave frequency is very small. Although this movement is small, a speaker not designed to handle the additional power can be damaged. For optimum results, use a speaker with a series inductance>10μH. An 8Ω speaker typically exhibits a series inductance in the range from 20μH to 100μH.

How to Reduce EMI

The ft2128 does not require an LC output filter for short connections from the amplifier to the speaker. However, additional EMI suppressions can be made by use of a ferrite bead in conjunction with a capacitor, as shown in Figure 36. Choose a ferrite bead with low DC resistance (DCR) and high impedance (100Ω~330Ω) at high frequencies (>100MHz). The current flowing through the ferrite bead must be also taken into consideration. The effectiveness of ferrites can be greatly aggravated at much lower than the rated current values. Choose a ferrite bead with a rated current value no less than 2A. The capacitor value varies based on the ferrite bead chosen and the actual speaker lead length. Choose a capacitor less than 1nF based on EMI performance.

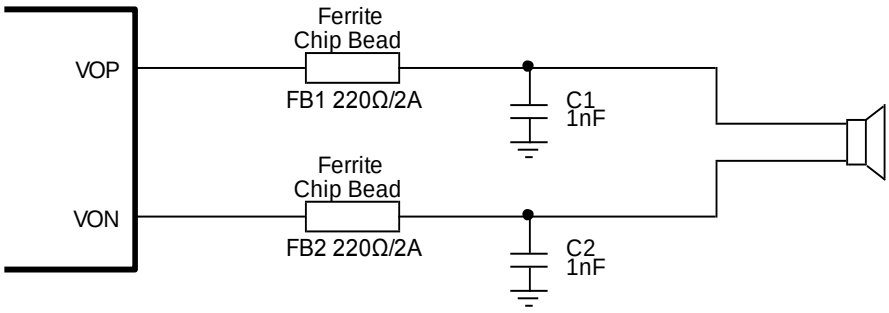


Figure 36: Ferrite Bead Filter to Reduce EMI

RC SNUBBER CIRCUIT

For applications where the power supply is rated more than 4.6V or the load resistance less than 6Ω, it may become necessary to add an RC snubber circuit between the two output pins, VOP and VON, for robustness and reliability. Figure 37 shows a simple RC snubber circuit, which can be used to prevent the device from accelerated deterioration or abrupt destruction due to excessive inductive flybacks that are induced on fast output switching or by an over-current or short-circuit condition.

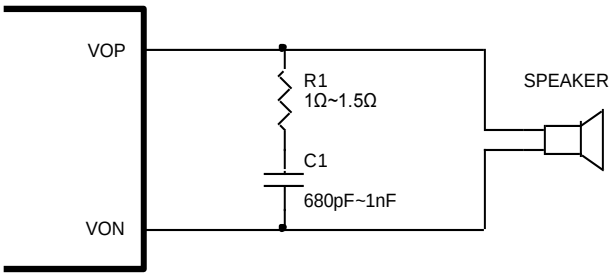


Figure 37: RC Snubber Circuit

Power Supply Decoupling Capacitor (C_S)

The ft2128 is a high-performance Class-D audio amplifier that requires adequate power supply decoupling. Adequate power supply decoupling ensures high efficiency and low THD+N.

Place a low equivalent-series-resistance (ESR) ceramic capacitor (X7R or X5R), typically 1μF, within 2mm of the VDD pin. This choice of capacitor and placement helps degenerate high frequency transients, spikes, or digital hash on the line. Also, placing the decoupling capacitor close to ft2128 is important, as any parasitic resistance or inductance between the ft2128 and the bypass capacitor causes loss of efficiency and degradation of audio quality. In addition to the 1μF ceramic capacitor, place a 47μF or larger capacitor on the VDD supply trace. This large capacitor will act as a charge reservoir, providing energy faster than the board supply, thus helping prevent any droop in the supply voltage.

Input Resistors (R_{IN})

To minimize the number of external components required for the application of ft2128, a set of 10KΩ input

resistors are integrated internally at INP and INN pins respectively. The internal input resistors also bring other benefits such as higher PSRR and lower turn-on pop noise since on-chip resistors can match well. Thus, for typical portable device applications, there is no need for additional input resistors connected to INP or INN pin. However, for applications where additional gain adjustment becomes necessary, a set of external input resistors can be added onto INP and INN pins respectively. The value of the external input resistors must be included for the calculation of the overall voltage gain (as described by Equation 1) as well as the selection of proper input capacitors (as described by Equation 3). As shown in Equation 2, the external input resistors will attenuate the original overall voltage gain by the ratio of $R_{INTERNAL}$ / (R_{IN} + $R_{INTERNAL}$).

$$A_V = A_{V0} \times [R_{INTERNAL} / (R_{IN} + R_{INTERNAL})] \quad (2)$$

where A_{V0} = 24 (27.6dB)
$R_{INTERNAL}$ = 10KΩ

Input Capacitors (C_{IN})

The input DC decoupling capacitors are recommended to bias the audio inputs to an optimum DC level. The input capacitor (C_{IN}), in conjunction with the amplifier input resistance (including both internal 10KΩ and external resistance R_{IN}, if any) forms a highpass filter that removes the DC bias from the audio inputs. The corner frequency, f_C, of the highpass filter is given by Equation 3

$$f_C = 1 / [2 \times \pi \times (R_{IN} + R_{INTERNAL}) \times C_{IN}] \quad (3)$$

where $R_{INTERNAL}$ = 10KΩ

Note that any mismatch in capacitance and resistance between the two differential inputs will cause a mismatch in the corner frequencies. Severe mismatch may also cause degradation of turn-on pop noise, PSRR, and CMRR performance. Choose the resistors and capacitors with a tolerance of ±5% or better.

Choose C_{IN} such that f_C is well below the lowest frequency of interest. Setting it too high affects the amplifiers' low-frequency response. Consider an example where the specification calls for A_V=21.6dB and a flat frequency response down to 20Hz. In this example, R_{IN}=10KΩ and C_{IN} is calculated to be about 0.40μF, thus 0.47μF, as a common choice of capacitance, can be chosen for C_{IN}.

The type of the input capacitor C_{IN} is also important. For best audio quality, use capacitors whose dielectrics have low-voltage coefficients, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, may result in increased distortion at low frequencies. Other factors for consideration when designing the input filter include the constraints of the overall system. Although high-fidelity audio requires a flat response between 20Hz and 20kHz, portable devices may concern primarily about the frequency range of the human voice, which ranges typically from 300Hz to 4kHz. Additionally, the physical size of the speakers used in most portable devices limits the low frequency response. In this case, the frequency components below 150Hz may be filtered out.

VREF Bypass Capacitor (C_{VREF})

A voltage at V_{DD}/2 is internally generated and provided to the VREF pin. A low-ESR ceramic capacitor of 1μF is strongly recommended at the VREF pin to ground. The bypass capacitor (C_{VREF}) significantly improves PSRR and THD+N performance by suppressing power supply and other noise sources at the common-mode bias node.

TYPICAL APPLICATION CIRCUITS

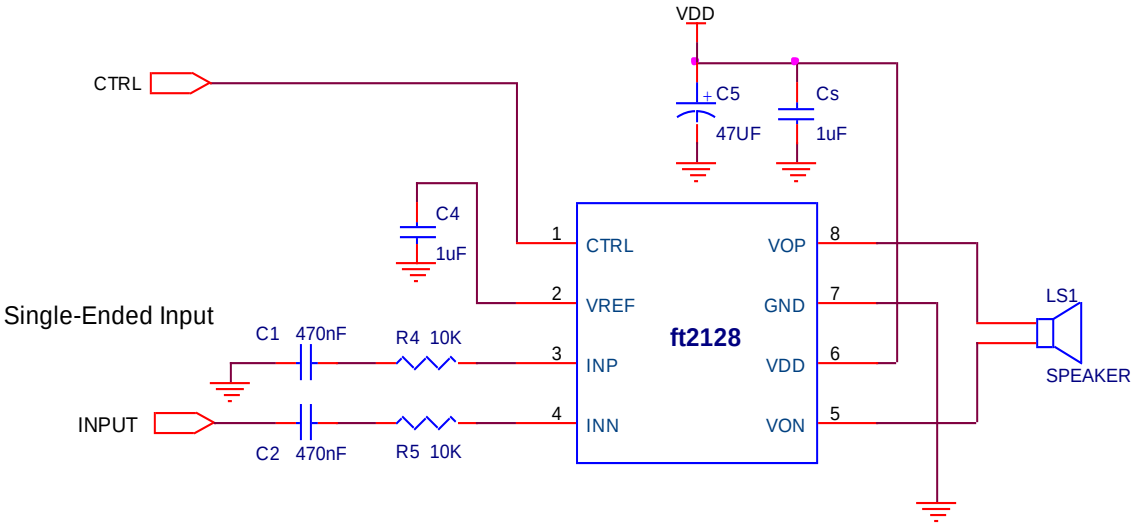


Figure 38: Single-Ended Audio Input (with Digital Pulse Control)

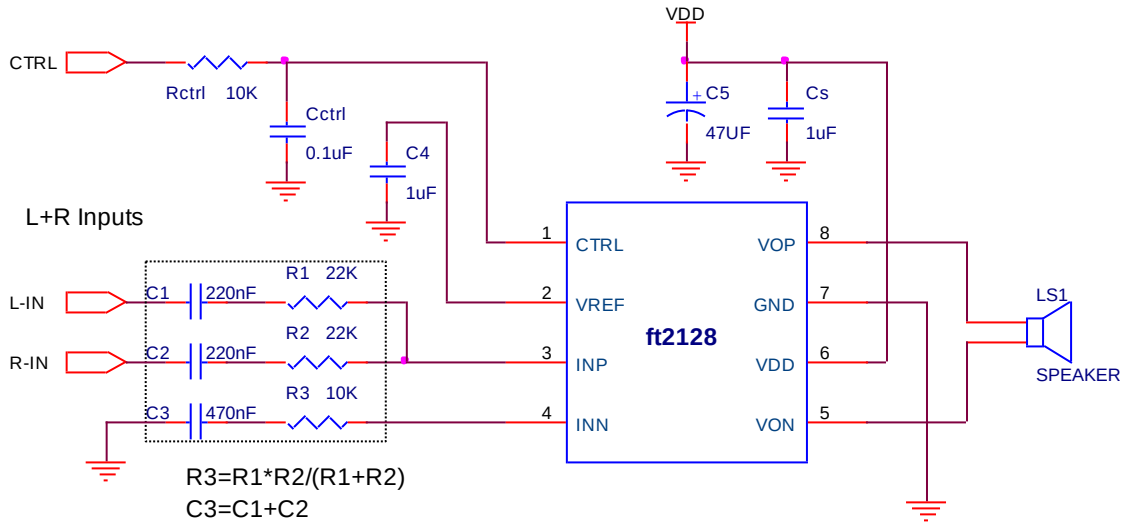


Figure 39: Dual Channel Audio Inputs (for ALC-2 Operation)

TYPICAL APPLICATION CIRCUITS (Cont'd)

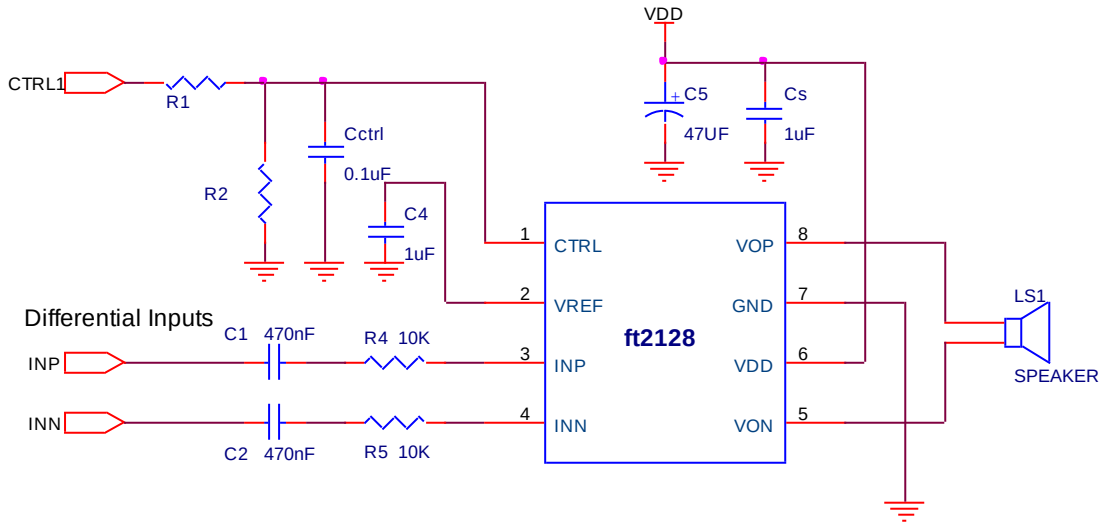


Figure 40: Differential Audio Inputs (for ALC-1 Operation)

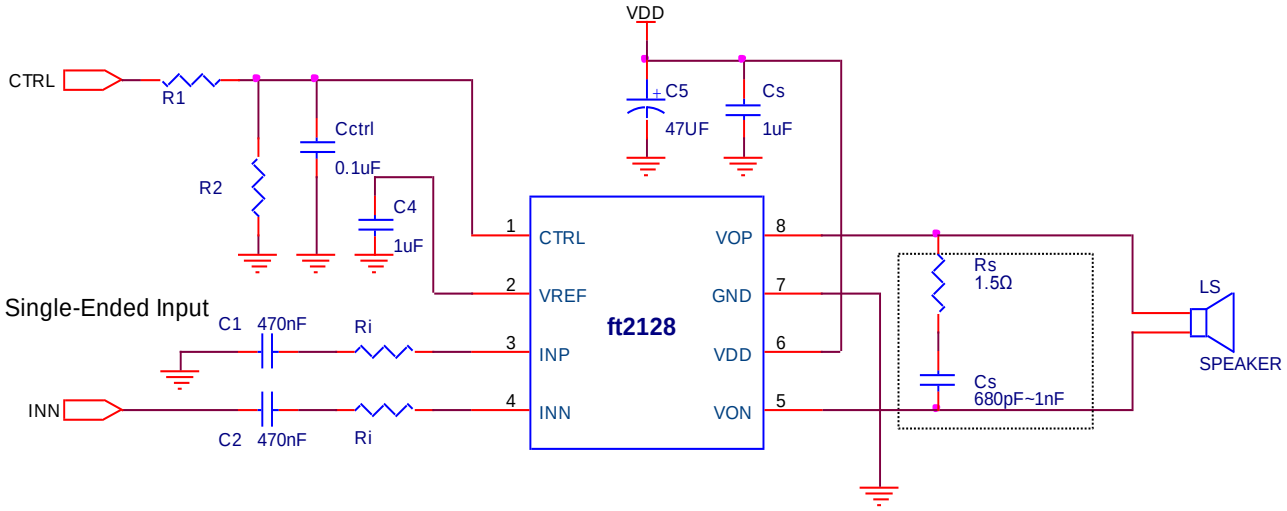
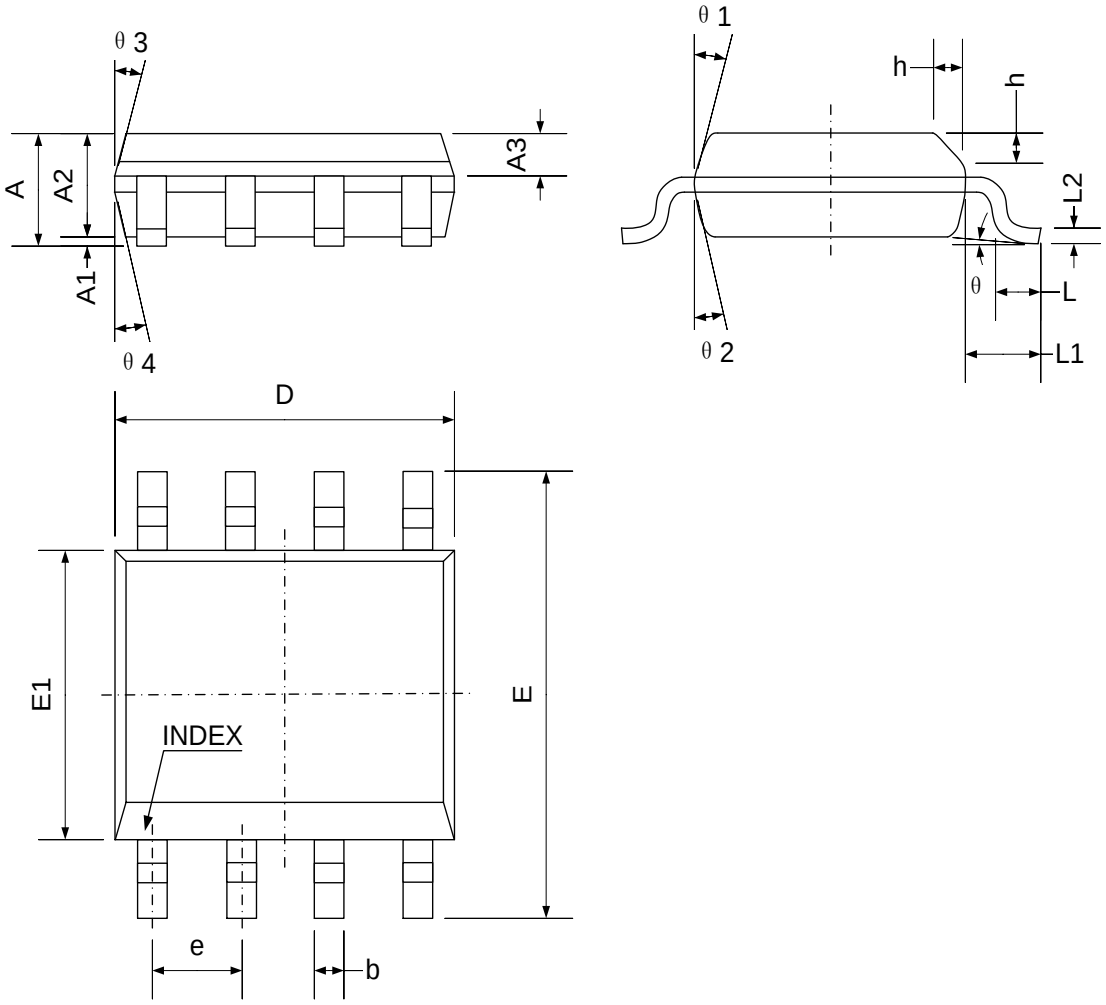


Figure 41: Single-Ended Audio Input (for ALC-1 Operation with a snubber circuit)

Note: It is strongly recommended to add a simple snubber circuit (RC in series) between the two outputs, VOP and VON, for robust reliability in the applications where the power supply is rated more than 4.6V or the load resistance less than 6Ω.

PHYSICAL DIMENSIONS

SOP-8 PACKAGE OUTLINE DIMENSIONS

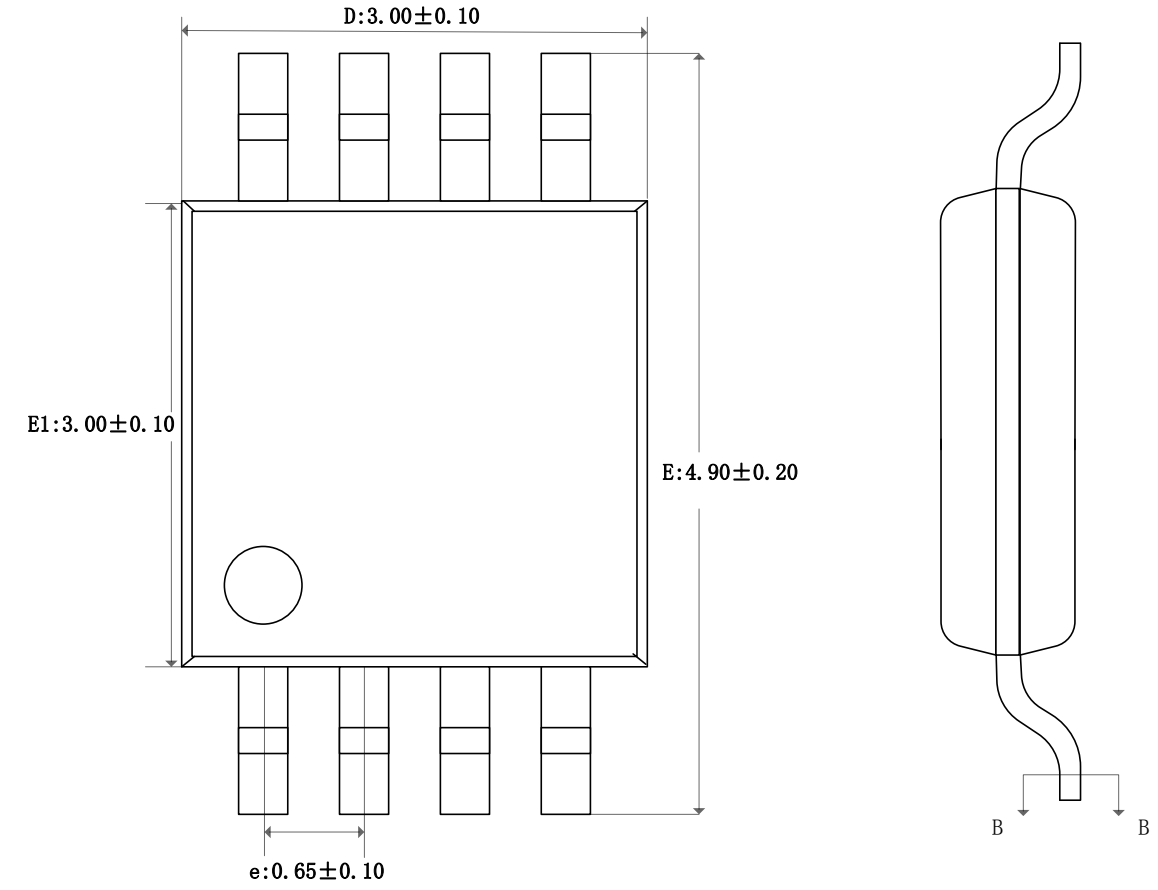


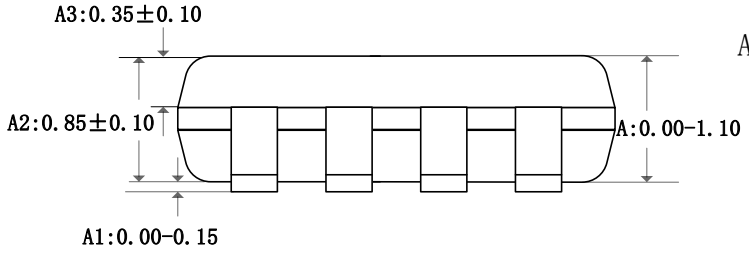
SYMBOL	MIN	NOM	MAX	UNIT
A	1.35	1.55	1.75	mm
A1	0.10	0.15	0.25	mm
A2	1.25	1.40	1.65	mm
A3	0.50	0.60	0.70	mm
b	0.38	-	0.51	mm
c	0.17	-	0.25	mm
D	4.80	4.90	5.00	mm
E	5.80	6.00	6.20	mm
E1	3.80	3.90	4.00	mm
e	1.27 (BSC)			mm
L	0.45	0.60	0.80	mm
L1	1.04REF			mm
L2	0.25BSC			mm
h	0.30	0.40	0.50	mm
θ	0	-	8°	
θ1	15°	17°	19°	
θ2	11°	13°	15°	
θ3	15°	17°	19°	
θ4	11°	13°	15°	

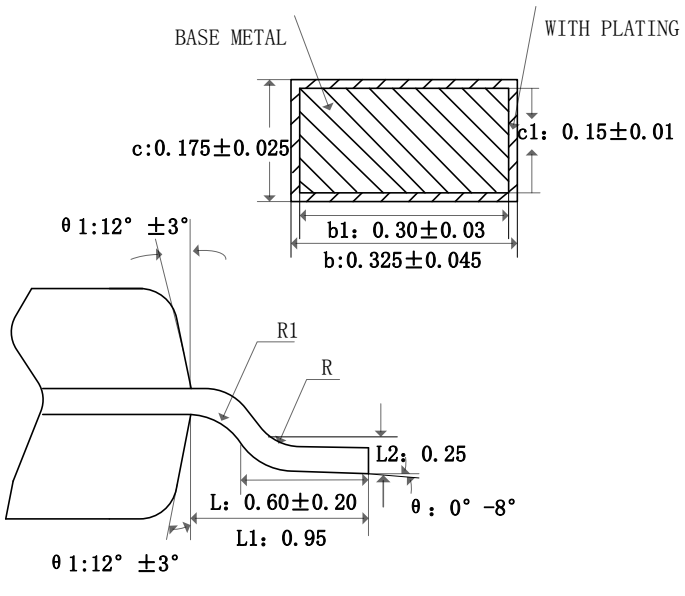
SOP-8 PACKAGE OUTLINE DIMEMSIONS

PHYSICAL DIMENSIONS (Cont'd)

MSOP-8 PACKAGE OUTLINE DIMENSIONS







All dimensions are in millimeters

Symbol	Dimensions in Millimeters	
	Min.	Max.
A	—	1.10
A1	0	0.15
A2	0.75	0.95
A3	0.25	0.39
b	0.28	0.37
b1	0.27	0.33
c	0.15	0.20
c1	0.14	0.16
D	2.90	3.10
E	4.70	5.10
E1	2.90	3.10
e	0.55	0.75
L	0.40	0.80
L1	0.95REF.	
L2	0.25BSC.	
R	0.07	—
R1	0.07	—
θ	0°	8°
θ1	9°	15°

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