ANALOG DEVICES

12-Bit, 10 MSPS A/D Converter

AD9005A

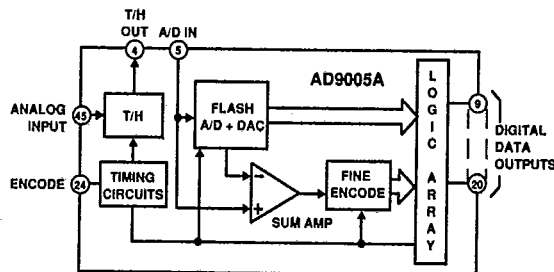## FEATURES
Complete 12-Bit A/D Converter
Includes Track and Hold, Reference, and Timing
Bipolar Analog Input (±1.024 V)
Up to 10 MSPS Sampling Rate
Low Power Dissipation: 3.2 W
Low Harmonic Distortion
MIL-STD-883-Compliant Versions Available

APPLICATIONS
Radar
Digital Receivers
Electro-Optics
Medical Scanners
Signal Intelligence
Spectrum Analyzers

FUNCTIONAL BLOCK DIAGRAM

GENERAL DESCRIPTION

The AD9005A is a complete 12-bit A/D converter which includes on-board track-and-hold amplifier, voltage reference, and timing circuits. Featuring sampling rates from dc to 10 MSPS, the AD9005A uses a subranging converter architecture to achieve high speed and high resolution. Dynamic performance includes a SNR of 64 dB and harmonic distortion of −72 dBc with a 4.3 MHz analog input.

This unit replaces its predecessor, the AD9005. The AD9005A uses a higher level of integration than the earlier design to provide increased performance, better reliability, and reduced cost.

The AD9005ALM guarantees a minimum 76 dBc (@ 2.3 MHz) spurious free dynamic range (SFDR) for applications which have demanding ac performance requirements. All grades are fully tested for dynamic performance.

Critical to the performance of the AD9005A is the use of advanced bipolar integrated circuits, custom designed for this device and manufactured by Analog Devices. The AD9005A is TTL-compatible with offset binary outputs. It is available in a 46-pin hermetic metal DIP in two temperature ranges: 0°C to +70°C commercial range and −55°C to +125°C military range (case temperature).

The AD9005A is available in versions compliant with MIL-STD-883. Refer to the *Analog Devices Military Products Databook* or current AD9005A/883B data sheet for detailed specifications.

AD9005A—SPECIFICATIONS

T-51-10-12

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage ($+V_{CC}$) . . . . +18 V
Negative Supply Voltage ($-V_{EE}$) . . . . −18 V
Positive Supply Voltage ($+V_S$) . . . . +6 V
Negative Supply Voltage ($-V_S$) . . . . −6 V
Analog Input Voltage (Pin 45) . . . . ±3.0 V dc
Digital Input Voltage . . . . −0.5 V to $+V_S$
Digital Output Current . . . . 4 mA

Operating Temperature Range (Case)
    AD9005KM . . . . 0°C to +70°C
    AD9005TM . . . . −55°C to +125°C
Storage Temperature Range . . . . −65°C to +150°C
Junction Temperature[2] . . . . +175°C
Lead Soldering Temperature (10 sec) . . . . +300°C

ELECTRICAL CHARACTERISTICS ($+V_{CC}=+15$ V, $-V_{EE}=-15$ V, $+V_S=+5$ V, $-V_S=-5.2$ V, unless otherwise stated)

Parameter	Temp	Test Level	Commercial 0°C to +70°C AD9005AKM Min	Typ	Max	Commercial 0°C to +70°C AD9005ALM Min	Typ	Max	Military −55°C to +125°C AD9005ATM Min	Typ	Max	Units
RESOLUTION	+25°C	I	12			12			12			Bits
LSB Weight	Full	V		0.5			0.5			0.5		mV
STATIC ACCURACY												
Differential Nonlinearity	+25°C	I	−0.75	±0.5	+0.75	−0.75	±0.5	+0.75	−0.75	±0.5	+0.75	LSB
	Full	VI	−1.0		+1.5	−1.0		+1.5	−1.0		+1.5	LSB
Integral Nonlinearity	+25°C	I		±1.0	±1.25		±1.0	±1.25		±1.0	±1.25	LSB
	Full	IV			±2.25			±2.25			±2.25	LSB
No Missing Codes	Full	VI	GUARANTEED			GUARANTEED			GUARANTEED			
Gain Error	+25°C	I		±0.5	±1.0		±0.5	±1.0		±0.5	±1.0	% FS
	Full	VI			±2.0			±2.0			±2.0	% FS
Offset Error	+25°C	I		±4	±15		±4	±15		±4	±15	mV
	Full	VI			±30			±40			±40	mV
ANALOG INPUT												
Input Voltage Range	Full	V		±1.024			±1.024			±1.024		V p-p
Input Resistance	Full	VI	950	1000	1050	950	1000	1050	950	1000	1050	Ω
Input Capacitance	+25°C	V		5			5			5		pF
Large Signal Input Bandwidth[3]	Full	V		38			38			38		MHz
DYNAMIC CHARACTERISTICS[5]												
Maximum Conversion Rate	Full	I	10			10			10			MSPS
Output Data Delay[6,9] (t_{PD})	+25°C	V		90			90			90		ns
Aperture Delay (t_A)	+25°C	V		5			5			5		ns
Aperture Uncertainty	+25°C	IV		10	20		10	20		10	20	ps rms
Transient Response (to ±1 LSB)[7]	+25°C	IV			120			120			120	ns
Overvoltage Recovery Time[8] (to ±1 LSB)	+25°C	IV			250			250			250	ns
Harmonic Distortion[10,4]												
F_{IN} = 540 kHz	+25°C	IV	−73	−78		−79	−83		−73	−78		dBc
F_{IN} = 2.3 MHz	+25°C	I	−68	−72		−76	−80		−68	−72		dBc
	Full	VI	−67			−75			−66			dBc
F_{IN} = 4.3 MHz	+25°C	I	−66	−72		−68	−75		−66	−72		dBc
	Full	VI	−65			−67			−63			dBc
Signal to Noise Ratio[11,4]												
F_{IN} = 540 kHz	+25°C	IV	65	67		66	68		65	67		dB
F_{IN} = 2.3 MHz	+25°C	I	63	65		65	66		63	65		dB
	Full	VI	63			64			60			dB
F_{IN} = 4.3 MHz	+25°C	I	62	64		63	65		62	64		dB
	Full	VI	61			62			60			dB
Two-Tone Intermodulation Distortion[12]												
F_{IN} = 2.2 MHz + 2.3 MHz	+25°C	V		−75			−76			−75		dBc
ENCODE INPUT[14]												
Logic "1" Voltage	Full	IV	2.0			2.0			2.0			V
Logic "0" Voltage	Full	IV			0.8			0.8			0.8	V
Logic "1" Current	Full	I			150			150			150	μA
Logic "0" Current	Full	I			150			150			150	μA
Input Capacitance	+25°C	V		5			5			5		pF
Encode Pulse Width (High)	+25°C	IV	25			25			25			ns
DIGITAL OUTPUTS												
Logic "1" Voltage (2 mA Source)	Full	I	2.4			2.4			2.4			V
Logic "0" Voltage (4 mA Sink)	Full	I			0.4			0.4			0.4	V
Logic Coding	Full	IV	Offset Binary			Offset Binary			Offset Binary			

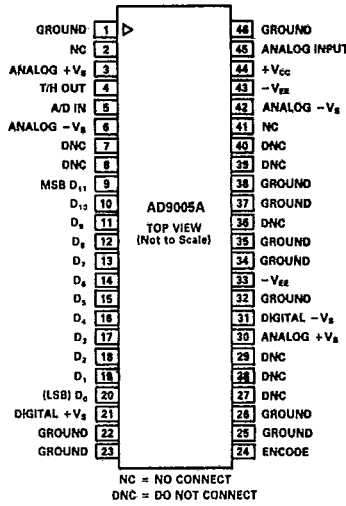| Parameter	Temp	Test Level	Commercial 0°C to +70°C AD9005AKM			Commercial 0°C to +70°C AD9005ALM			Military −55°C to +125°C AD9005ATM			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
POWER SUPPLY												
Supply Voltage +V_CC	Full	VI	+14.25	+15.0	+15.75	+14.25	+15.0	+15.75	+14.25	+15.0	+15.75	V
Supply Current +V_CC	Full	VI		15	25		15	25		15	25	mA
Supply Voltage −V_EE	Full	VI	−14.25	−15.0	−15.75	−14.25	−15.0	−15.75	−14.25	−15.0	−15.75	V
Supply Current −V_EE	Full	VI		30	55		30	55		30	55	mA
Supply Voltage +V_s	Full	VI	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
Supply Current Analog +V_s	Full	VI		180	210		180	210		180	210	mA
Supply Current Digital +V_s	Full	VI		43	60		43	60		43	60	mA
Supply Voltage −V_s	Full	VI	−4.95	−5.2	−5.45	−4.95	−5.2	−5.45	−4.95	−5.2	−5.45	V
Supply Current Analog −V_s	Full	VI		210	250		210	250		210	250	mA
Supply Current Digital −V_s	Full	VI		65	100		65	100		65	100	mA
Nominal Power Dissipation	Full	VI		3.2	4.0		3.2	4.0		3.2	4.0	W
PSRR[13, 15]	+25°C	I		0.01	0.02		0.01	0.02		0.01	0.02	%/%

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. Exposure to absolute rating conditions for extended periods of time may affect device reliability.

[2]Maximum junction temperature should not be allowed to exceed +175°C. Hybrid thermal model:

$$t_{JUNCTION} = t_{AMBIENT} + P_{DISSIPATION} \times (\theta_{CA}) + (T_S - T_C) \ max$$

where $(T_S - T_C)$ max = 10°C

46 Pin metal DIP: θ_{CA} = 14°C/W in still air;

θ_{CA} = 6°C/W with 500 LFPM air flow

[3]Determined by 3 dB reduction in reconstructed output.

[4]Input at 1 dB below full scale.

[5]Measured at 10 MHz encode rate.

[6]Measured from ENCODE in to data out for LSB only.

[7]For full-scale step input; 12-bit accuracy is attained in the specified time.

[8]Recovers to 12-bit accuracy in specified time following 200% full-scale input voltage.

[9]Excludes pipeline delay of two clock cycles (see timing diagram).

[10]Worst case spurious in-band signal relative to input level.

[11]RMS signal to RMS noise, including harmonics.

[12]Worst case spurious in-band signal relative to level of input tones, which are both −7 dB below full scale.

[13]Sensitivity of full-scale gain error with respect to power supply variation within supply Min/Max limits.

[14]ENCODE signal rise and fall times should be less than 5 ns for normal operation. Transition from "0" to "1" initiates conversion.

[15]PSRR is tested over given voltage range.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS
Test Level
I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures.
III – Periodically sample tested only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for military temperature devices. Guaranteed, not tested, for commercial temperature range

AD9005A

AD9005A PIN DESIGNATIONS

```
            GROUND  1  ▷        46  GROUND
               NC   2           45  ANALOG INPUT
         ANALOG +Vs  3          44  +Vcc
            T/H OUT  4          43  -VEE
             A/D IN  5          42  ANALOG -Vs
         ANALOG -Vs  6          41  NC
               DNC   7          40  DNC
               DNC   8          39  DNC
           MSB D11   9          38  GROUND
              D10   10   AD9005A 37  GROUND
               D9   11   TOP VIEW 36  DNC
               D8   12  (Not to Scale) 35  GROUND
               D7   13          34  GROUND
               D6   14          33  -VEE
               D5   15          32  GROUND
               D4   16          31  DIGITAL -Vs
               D3   17          30  ANALOG +Vs
               D2   18          29  DNC
               D1   19          28  DNC
          (LSB) D0  20          27  DNC
        DIGITAL +Vs  21          26  GROUND
            GROUND  22          25  GROUND
            GROUND  23          24  ENCODE
```

NC = NO CONNECT
DNC = DO NOT CONNECT

AD9005A PIN DESCRIPTIONS

Pin	Name	Description
1	GROUND	Circuit ground. All grounds should be connected together near the AD9005A.
2	NC	Not internally connected.
3	ANALOG +V_S	Positive analog supply pin. Nominally +5 V dc.
4	T/H OUT	Output of internal track-and-hold amplifier. Connect to Pin 5 for normal operation.
5	A/D IN	Input to internal A/D encoder. Connect to Pin 4 for normal operation.
6	ANALOG $-V_S$	Negative analog supply pin. Nominally -5.2 V dc.
7, 8	DNC	Do not connect. Internal test point.
9	D_{11} (MSB)	Most significant bit of digital output data.
10-19	D_1-D_{10}	Digital data outputs.
20	D_0 (LSB)	Least significant bit of digital output data.

OUTPUT CODING

ANALOG INPUT	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
$\geq +1.024V$	1	1	1	1	1	1	1	1	1	1	1	1
$\leq -1.024V$	0	0	0	0	0	0	0	0	0	0	0	0

| Pin	Name	Description
21	DIGITAL +V_S	Positive digital supply pin. Nominally +5 V dc.
22, 23	GROUND	Circuit ground. All grounds should be connected together near the AD9005A.
24	ENCODE	Convert command. TTL compatible, rising edge triggered.
25, 26	GROUND	Circuit ground. All grounds should be connected together near the AD9005A.
27-29	DNC	Do not connect. Internal test point.
30	ANALOG +V_S	Positive analog supply pin. Nominally +5 V dc.
31	DIGITAL $-V_S$	Negative digital supply pin. Nominally -5.2 V dc.
32	GROUND	Circuit ground. All grounds should be connected together near the AD9005A.
33	$-V_{EE}$	Negative analog supply pin. Nominally -15 V dc.
34, 35	GROUND	Circuit ground. All grounds should be connected together near the AD9005A.
36	DNC	Do not connect. Internal test point.
37, 38	GROUND	Circuit ground. All grounds should be connected together near the AD9005A.
39, 40	DNC	Do not connect. Internal test point.
41	NC	Not internally connected.
42	ANALOG $-V_S$	Negative analog supply pin. Nominally -5.2 V dc.
43	$-V_{EE}$	Negative analog supply pin. Nominally -15 V dc.
44	$+V_{CC}$	Positive analog supply pin. Nominally +15 V dc.
45	ANALOG INPUT	Analog input. Full scale of ±1.024 V.
46	GROUND	Circuit ground. All grounds should be connected together near the AD9005A.

AD9005A

TIMING DIAGRAM
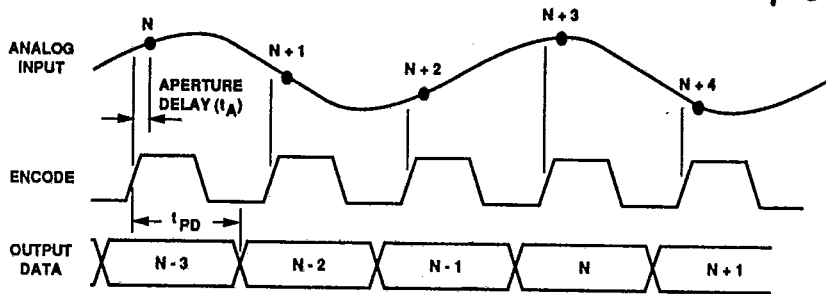
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EQUIVALENT INPUT/OUTPUT CIRCUITS

BURN-IN CIRCUIT

ALL CAPACITORS
IN µF ± 10%
RESISTORS IN
OHMS ± 5%
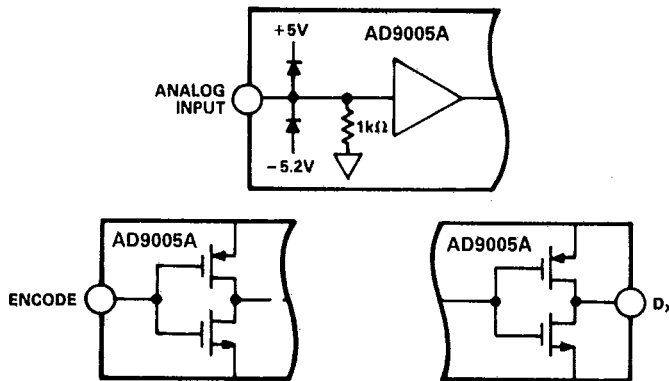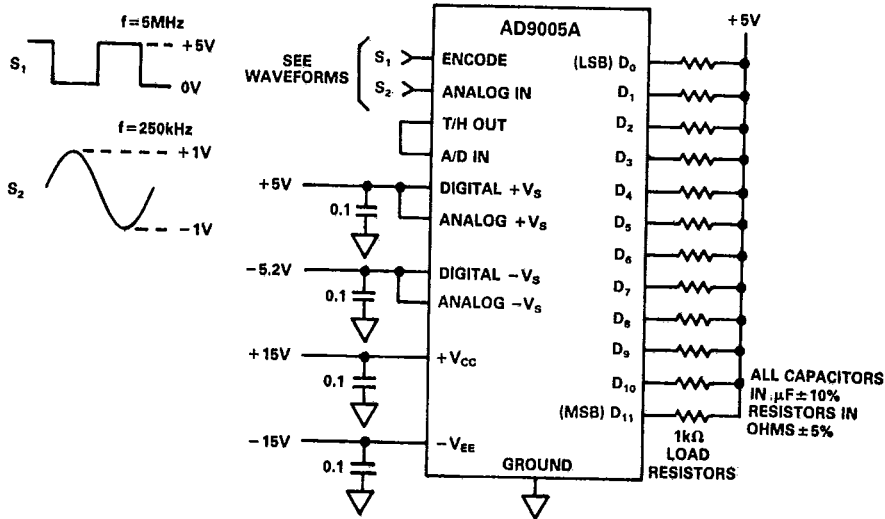
AD9005A

APPLICATIONS INFORMATION

The AD9005A is a complete analog-to-digital converter. The AD9005A uses a subranging A/D architecture enhanced by hybrid technology. This includes an on-board track-and-hold amplifier, on-board references, timing circuitry and output latches.

The analog input of the AD9005A is fed directly into the internal track-and-hold amplifier, thus eliminating the need for external signal conditioning in many applications. This amplifier provides low input capacitance and a bipolar (±1.024 V) input range. Normally reverse-biased Schottky diodes on the input provide overrange protection. If the amplitude, bandwidth or dc voltage level of the analog input signal calls for external signal conditioning, it is advisable to use an amplifier with low harmonic distortion and low noise characteristics. Selecting the amplifier may be difficult because the performance of the AD9005A will probably exceed the performance of most commercially available amplifiers. A notable exception is the AD9617, a wideband, low noise current feedback amplifier. It is important to remember that band limiting the analog input signal can avoid aliasing during the A/D conversion process.

Timing in the AD9005A is critical, and careful measures must be taken to support 12-bit accuracy. One simple way to enhance the performance of the AD9005A is to synchronize the system clock to a crystal oscillator. This will minimize any clock jitter,

a must for maintaining the spectral purity of analog signals near Nyquist limits. Because the conversion cycle begins with the rising edge of the encode signal, a fast, clean rising edge will also help to reduce any clock jitter.

When the ENCODE signal of the AD9005A goes HIGH, the internal track-and-hold enters the hold state; after 65 ns, it returns to track mode. In applications in which the AD9005A is clocked slowly or intermittently (i.e., in burst mode), the encode signal should be returned to a logic LOW state during the idle periods.

The ENCODE signal pulse width should also be adjusted so that it is in the HIGH (hold) state for a minimum of 25 ns. This ensures that the T/H enters the hold mode before the A/D conversion takes place.

The AD9005A has many appealing characteristics for 12-bit A/D converter applications. Its dynamic performance is state-of-the-art in hybrid technology. Typical applications include radar, missile guidance, digital oscilloscopes, waveform analyzers, medical instrumentation, electro-optics, communications and ESM.

TYPICAL AD9005A APPLICATION
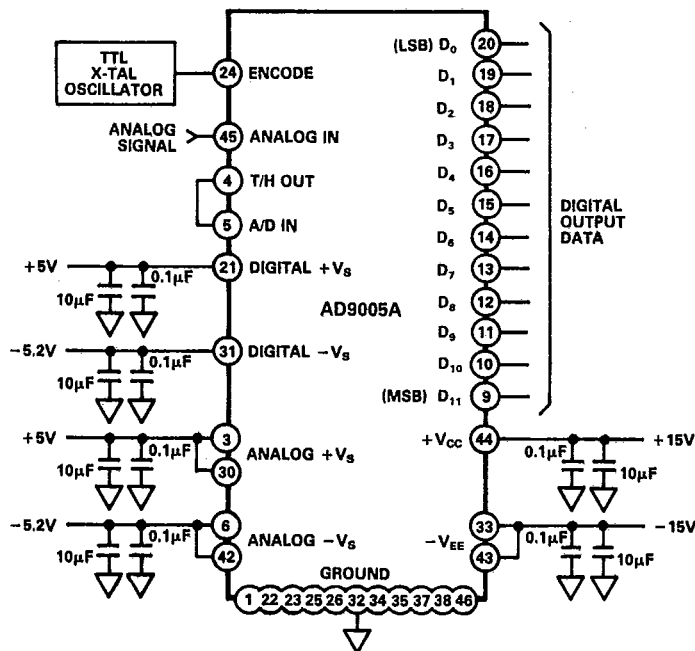
Layout Information

The accuracy of a 12-bit converter, especially one with the dynamic performance level of the AD9005A, requires that designers pay careful attention to printed circuit board layouts. Analog signal paths should be impedance matched, with termination/load resistors at or near package connections. Analog signal paths should also be isolated from digital signal paths. Otherwise digital signals can be capacitively coupled into the analog section of the circuit, degrading the overall performance of the A/D converter.

Digital switching noise on power supplies can also degrade converter performance. Because of this noise (inherent with TTL logic), the digital power supplies of the AD9005A should be separated from the analog power supplies. In addition, each power supply should be capacitively decoupled to ground. To accomplish this, a single large value capacitor with a high resonant frequency (a 10 μF tantalum capacitor for example) should be used on each of the AD9005A's power supplies, at or near the package. In addition, a lower value capacitor with good high frequency characteristics (a 0.1 μF ceramic chip capacitor is recommended) should be connected to each power supply pin connection.

For applications in which only single +5 V and/or −5.2 V supplies are available, a ferrite bead, placed in series between the analog and digital power pins, can be used to isolate the digital noise from the analog circuits.

Noise on the circuit ground is often the limiting factor in A/D converter performance. Perhaps the most critical concerns of circuit layout are the ground connections. To reduce ground noise, a two-sided printed circuit board is recommended, the component side being reserved (as much as possible) for a single, low impedance ground plane. The other side should be used for all (possible) power and signal connections. Each of the ground connections of the AD9005A should be connected to the ground plane, and most of the area under the AD9005A should be part of this ground plane. The metal case of the AD9005A is connected to ground.

Operation of the AD9005A requires that Pin 4, the output of the internal track-and-hold, be connected to Pin 5, the input to the AD9005A's A/D converter circuitry. A suggested layout, showing this connection, is shown below.

A final suggestion regarding circuit layout concerns the use of sockets. Ideally, parts should be soldered into boards in final designs. If sockets must be used, individual pin sockets are recommended to avoid lead inductance and capacitive coupling between adjacent pins. Pin sockets are available from Amp, part #6−330808−0.
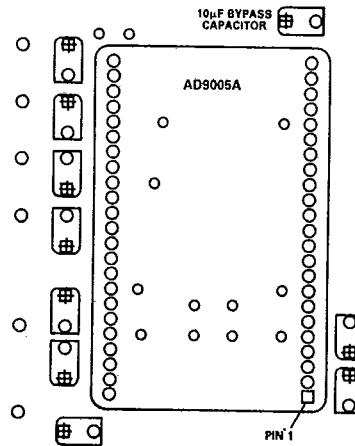
SUGGESTED LAYOUT
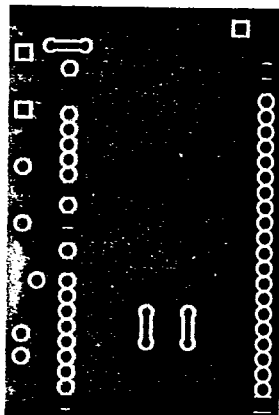
*GND Plane Side
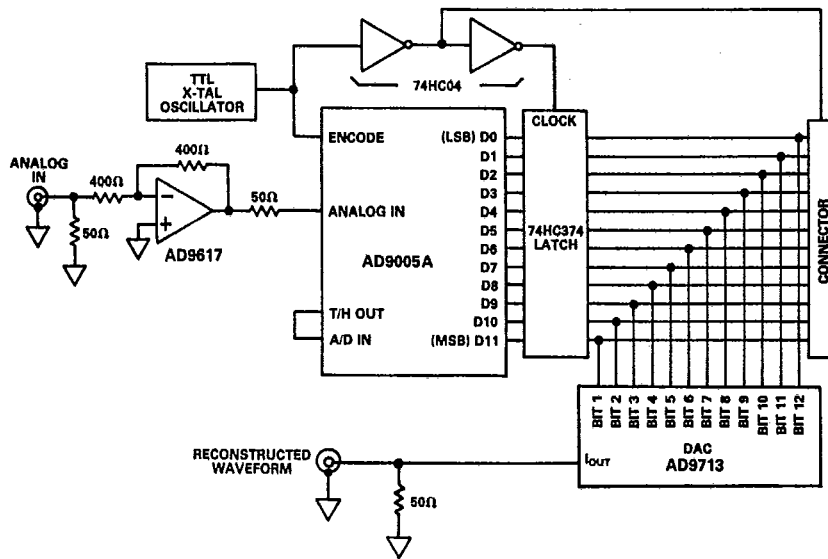(As Viewed from Top)*
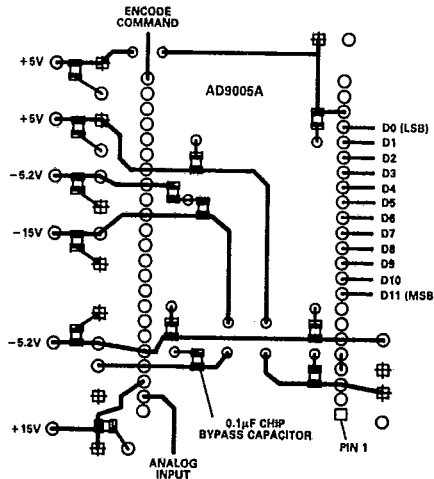
*Solder Side
(As Viewed from Top)*

*Component Mounting
(As Viewed from Top)*

AD9005A

EVALUATION CIRCUIT

ORDERING GUIDE

Model	Temperature Range	Package	Package Option*
AD9005AKM	0°C to +70°C	46-Pin DIP, Commercial Temperature	M-46
AD9005ALM	0°C to +70°C	46-Pin DIP, Commercial Temperature	M-46
AD9005ATM	−55°C to +125°C	46-Pin DIP, Military Temperature	M-46
AD9005A/PCB	0°C to +70°C	AD9005A Evaluation Board	M-46

*M = Hermetic Metal Can DIP.

AD9005A DYNAMIC PERFORMANCE (AT +25°C)
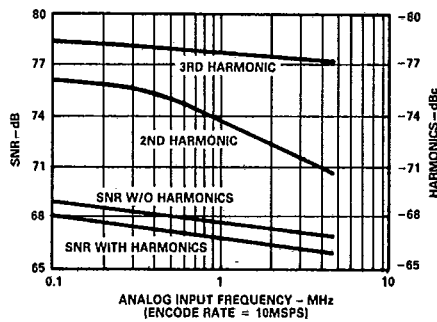
OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).

46-Pin Metal Dual In-Line Can

REV. A