SY6897A

2.5V to 16V Protection Switch with Blocking FET Control

General Description

The eFuse SY6897A is a highly integrated circuit protection and power management solution in a tiny package. The device uses few external components and provides multiple protection modes. It is a robust defense against overload, short circuit, excessive inrush current.

Extremely low power path resistance $R_{DS(ON)}$ helps to reduce power loss during the normal operation. An open drain indicator pin is opened to show the operation status of device. It integrates the over-temperature protection and auto-recovery with hysteresis to protect against over current events.

Current limit level can be set with a single external resistor. Application with particular voltage ramp requirement can set SST pin with a single capacitor to ensure proper output ramp rates. An external NFET can be connected "Back to Back (B2B)" with the SY6897A output and the driven by BFET to prevent current flow from load to source when shutdown.

The SY6897A adopts compacted QFN2x2-12 footprint.

Features

- 2.5V to 16V Input Voltage Range
- Extremely Low Power Path Resistance $R_{DS(ON)}$
  $R_{DS(ON)}$=30mΩ Typical
- Open Drain Indicator Pin for Operation Status
- 1A to 5A Current Limit
- ±10% I_{LIMIT} Accuracy at 3A
- Programmable OUT Slew Rate
- Built-in Thermal Shutdown
- Small Foot Print –QFN (2mm×2mm)

Applications

- Power Bank
- LCD Panel
- HDD and SSD Drives
- Set Top Boxes
- Servers / AUX Supplies
- Fan Control
- PCI/PCIe Cards
- Adapter Powered Devices

Ordering Information

SY6897 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY6897ATLC	QFN2×2-12	----

Typical Applications

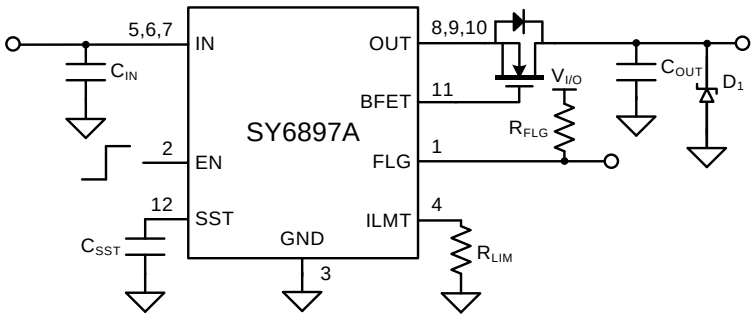
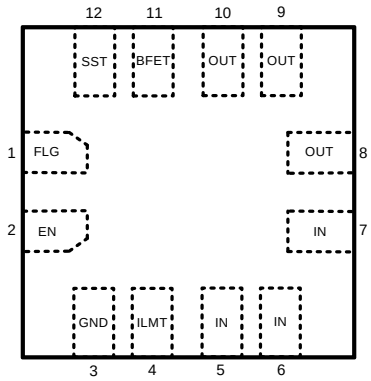


Figure1. Schematic Diagram

Pinout (top view)



(QFN2×2-12)

Top mark: **Yexyz** (Device code: Ye, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
FLG	1	Open drain indicator pin. FLG will be pulled down when over current, short circuit or thermal shutdown occurs.
GND	3	Ground pin.
IN	5,6,7	Input voltage and supply voltage; connect 0.1 μF or greater ceramic capacitor from IN to GND as close to the device as possible
OUT	8,9,10	Power-switch output
BFET	11	Connect this pin to the gate of an external blocking NFET. This pin can be left floating if it is not used.
EN	2	Pull high to enable SY6897A. Do not leave it floating.
SST	12	Connect a capacitor from this pin to GND to control the ramp rate of OUT at device turn-on.
ILMT	4	A resistor from this pin to GND will set the over current limit.

Block Diagram

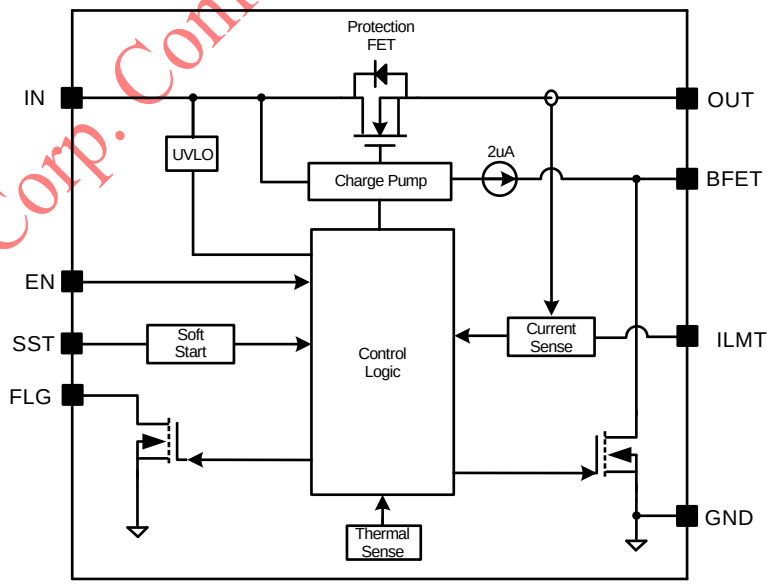


Figure2. Block Diagram

Absolute Maximum Ratings (Note 1)

IN, EN, FLG ---------- -0.3V to 18V
OUT ---------- -0.3V to IN+0.3V
BFET ---------- -0.3V to 26V
ILMT, SST ---------- -0.3V to 3.6V
FLG Continuous Output Sink Current ---------- 25mA
BFET Continuous Output Sink Current ---------- 20mA
Power Dissipation, P_D @ T_A = 25°C---------- 2.7W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 46° C/W
θ_{JC} ----------18° C/W
Junction Temperature Range ---------- -40°C to +150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

IN ---------- 2.5V to 16V
BFET ---------- 0V to IN+6V
EN ---------- 0V to 16V
SST, ILMT ---------- 0V to 3V
OUT Continuous Output Current ---------- 0A to 5A
FLG Continuous Output Sink Current ---------- 0mA to 10mA
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(–40 ≤ T_J ≤ 125°C, V_{IN} = 12 V, V_{EN} = 2 V, R_{ILMT} =1.1kΩ, C_{SST} = OPEN, R_{FLG} =10kΩ. Typical values are at 25°C. All voltages are with respect to GND, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.5		16	V
IN Rising UVLO Threshold Voltage	V_{UVLO}				2.45	V
Hysteresis	$V_{UVLO-HYS}$			100		mV
Shutdown Current	I_{SHDN}	EN=0V		2		μA
Bias Current	I_Q	EN=2V		62		μA
ON Resistance	$R_{DS(ON)}$	T_J = 25°C	24	30	36	mΩ
		T_J = 125°C		45	52	mΩ
OUT Overload Current limit	I_{OC}	R_{ILMT} = 5.5kΩ	0.80	1.00	1.20	A
		R_{ILMT} = 3.65kΩ	1.30	1.50	1.70	A
		R_{ILMT} = 2.75kΩ	1.80	2.00	2.20	A
		R_{ILMT} = 1.85kΩ	2.70	3.00	3.30	A
		R_{ILMT} = 1.1kΩ	4.50	5.00	5.50	A
Soft-start Time Range	t_{SST}	Note 4	0.5		60	ms
Soft-start Time Accuracy			-30%		30%	t_{SST}
Turn-on Delay Time	$t_{d(ON)}$	EN → H to I_{VIN} = 100 mA, 1A resistive load at OUT		200		μs
Turn-off Delay Time	$t_{d(OFF)}$	EN → L to 0.9×OUT		100		μs
Output Discharge Resistor	R_{DIS}	V_{IN}=5V, EN=0, V_{OUT}=0.1V		100		Ω
BFET Charging Current	I_{BFET}	V_{BFET} = V_{OUT}		2		μA
BFET Clamp Voltage	$V_{BFET-MAX}$	V_{BFET} - V_{IN}		6.0		V
BFET Discharging Resistance to GND	$R_{BFET-DIS}$	V_{EN} = 0 V, I_{BFET} = 10mA	15	26	36	Ω
BFET Turn-on Duration	$t_{BFET-ON}$	EN→H to V_{BFET} = 12V, C_{BFET} = 1nF		6.0		ms
		EN→H to V_{BFET} = 12V, C_{BFET} = 10nF		60		ms
BFET Turn-off Duration	$t_{BFET-OFF}$	EN→L to V_{BFET} = 1V, C_{BFET} = 1nF		7.5		μs
		EN→L to V_{BFET} = 1V, C_{BFET} = 10nF		8.5		μs
EN Pin Logic-high Voltage	V_{ENH}		1			V
EN Pin Logic-low Voltage	V_{ENL}				0.4	V
FLG Output Low Voltage	V_{FLGL}	I_{FLG} = 1mA			200	mV
Over Current FLG Deglitch	t_{FLG}			2.6		ms
Thermal Shutdown Threshold	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			20		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a Silergy's test board.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note4. Recommended Current Soft-start Time Program Table

SST cap (nF)	None	10	47	100
SR (V/ms)	6.67	1.74	0.37	0.17

Recommended formula for C_{SS} & Soft-start slew rate calculation:

$$SR_{OUT} = \frac{17\mu}{C_{SST}(nF)}(V/ms)$$

$$t_{SST} = 0.8 \times \frac{VIN}{SR_{OUT}}(ms)$$

For a 12V application, a 100nF SST cap can make the OUT rise time equal to 56ms.

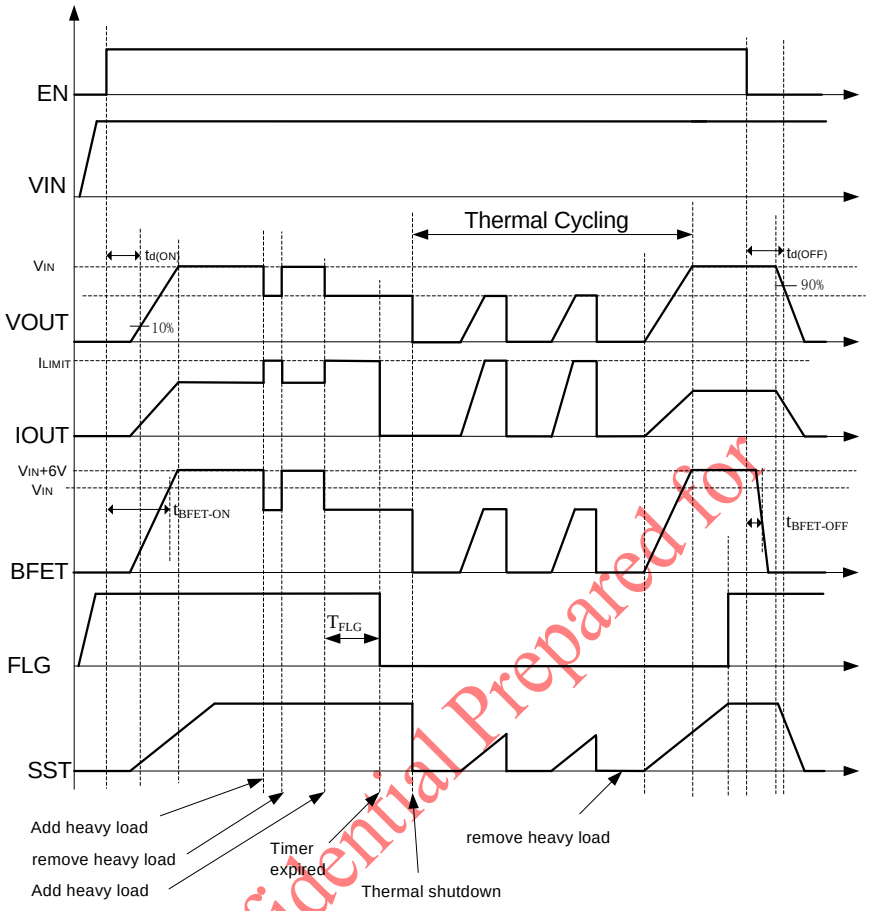
Note5. Recommended Current Limit Program Table

Current Limit Resistance (kΩ)	5.5	2.75	2.2	1.85	1.55	1.4	1.2	1.1
Current Limit (A)	1.0	2.0	2.5	3.0	3.5	4.0	4.5	5.0

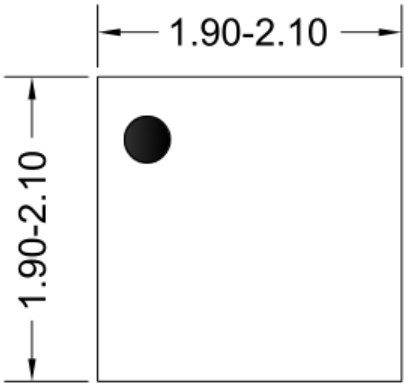
Recommended formula for R_{LIM} & current limit calculation:

$$R_{ILMT} = \frac{5.5K}{I_{LIM}}(\Omega)$$

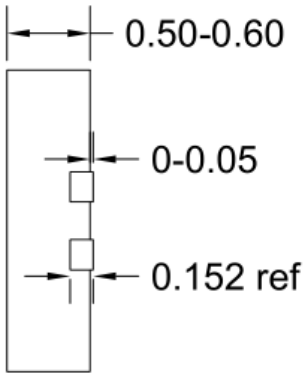
Timing Diagram



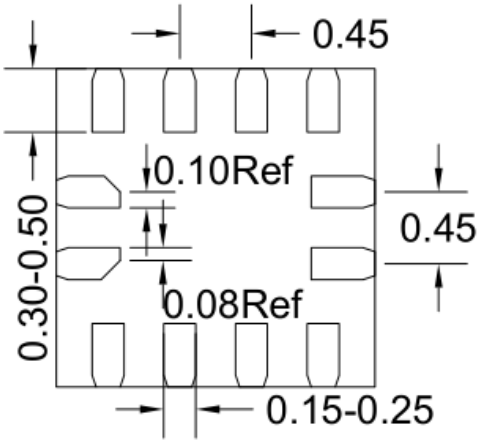
QFN2×2-12 Package Outline Drawing



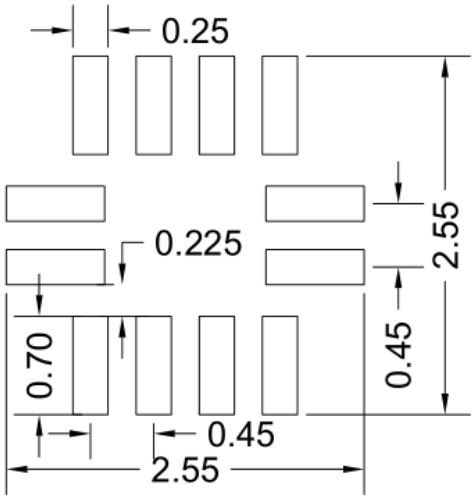
Top view



Side view



Bottom view



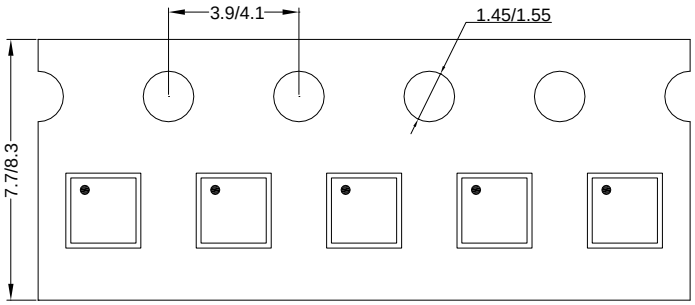
Recommended PCB layout

Notes: 1. All dimension in millimeter and exclude mold flash & metal burr.
2. Recommended PCB layout only for reference.

Taping & Reel Specification

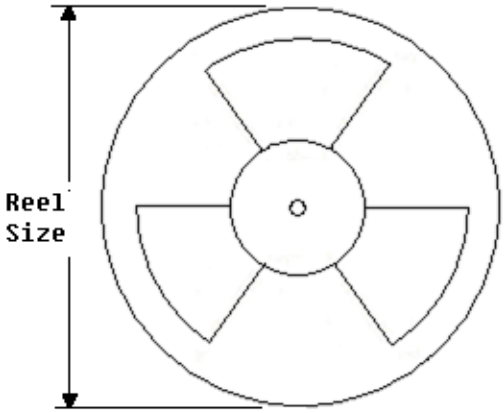
1. Taping orientation

QFN2×2



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN2×2	8	4	7"	400	160	3000

3. Others: NA