3A, ULTRA LOW NOISE, HIGH ACCURACY, LDO VOLTAGE REGULATOR

Description

The DIODES™ AP7179D is a high output current (3A), low-dropout regulator capable of sourcing 3A with 180mV maximum dropout, low-noise (4.4μV_{RMS}), high output voltage accuracy (1%). The device output voltage is pin-programmable from 0.8V to 3.95V using a PCB layout and adjustable from 0.8V to 5.0V using an external resistor divider. The device supports a lower input voltage of 1.1V, which makes it flexible to use and requires a lower component count.

The device's low noise (4.4μV_{RMS}), high PSRR, and high output current capability makes it ideal to power noise-sensitive devices such as high-performance serializers and deserializers (SerDes), analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and RF components.

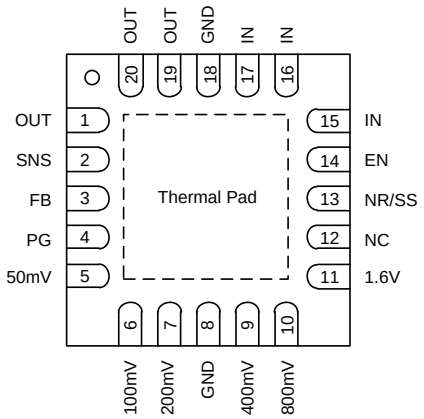
High output accuracy, remote sensing, excellent transient performance, and soft-start capabilities also make the AP7179D ideal to power digital loads such as field-programmable gate arrays (FPGAs), digital signal processors (DSPs), and application-specific integrated circuits (ASICs).

The enable control and a power-good indicator provide easy and accessible power-sequence control. Output noise immunity is enhanced by adding a bypass capacitor on NR/SS pin.

The AP7179D is packaged in the W-QFN3535-20 (Type A1) package.

Pin Assignments

(Top View)



W-QFN3535-20 (Type A1)

Features

- Low V_{IN} and Wide V_{IN} Range: 1.1V to 6.5V
- Low Dropout Voltage: 180mV at 3A
- V_{OUT} Accuracy ±1% Over Line, Load, and Temperature
- Pin-Strapped Output Voltage
  - Output Voltage Range: 0.8V to 3.95V
- Adjustable Output Voltage
  - Output Voltage Range: 0.8V to 5.5V
- Ultra-High PSRR: 40dB at 500kHz
- Output Voltage Noise:
  - 4.4μVRMS at 0.8V Output
  - 7.7μVRMS at 5.0V Output
- Adjustable Soft-Start Output
- Open-Drain Power-Good Indicator Function
- Stable with a 47μF or Larger Ceramic Output Capacitor
- Excellent Load Transient Response
- Enable Control
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Applications

- Portable electronic devices
- Digital loads: SerDes, FPGAs, and DSPs
- Analog circuits applications: VCO, ADC, DAC, and LVDS
- Test and measurement equipment

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

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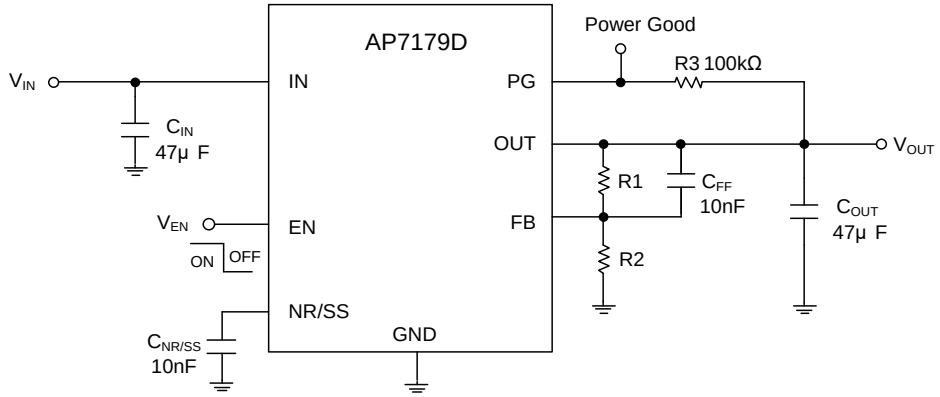
Typical Applications Circuit

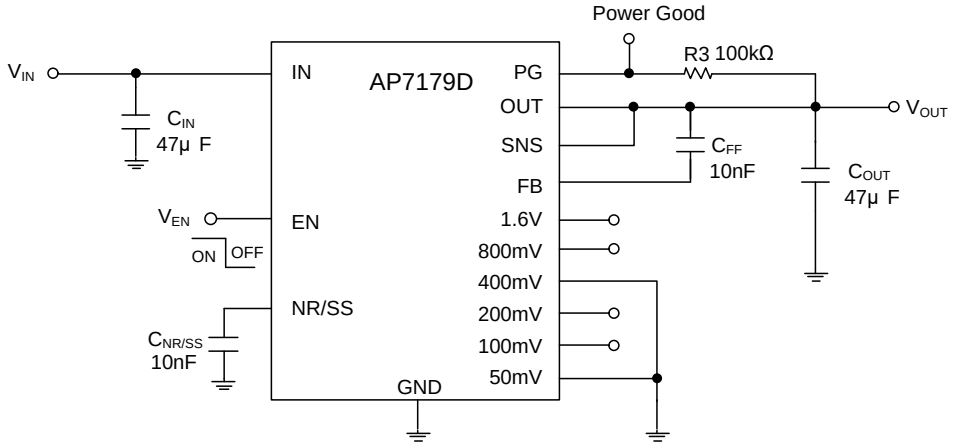


$$V_{OUT} = V_{FB}\left(1 + \frac{R1}{R2}\right)$$

Figure 1. Configuration Circuit for V_{OUT} Adjusted by a Resistive Divider

Table 1. Recommended Feedback-Resistor Values

Output Voltage(V)	External Restive Divider Combinations	
	R1(KΩ)	R2(KΩ)
0.9	12.4	100
1	12.4	49.9
1.2	12.4	24.9
1.5	12.4	14.3
1.8	12.4	10
2.5	12.4	5.9
3.3	11.8	3.74
4.5	11.8	2.55
5	12.4	2.37



$V_{OUT} = V_{REF} + 50mV + 400mV = 0.8V + 50mV + 400mV = 1.25V$

Figure 2. Configuration Circuit for V_{OUT} Adjusted via PCB layout

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Typical Applications Circuit (continued)

Table 2. Programming VOUT Target by Output Voltage Setting Pin

V_{OUT}(V)	50mV	100mV	200mV	400mV	800mV	1.6V	V_{OUT}(V)	50mV	100mV	200mV	400mV	800mV	1.6V
0.80	Open	Open	Open	Open	Open	Open	2.40	Open	Open	Open	Open	Open	GND
0.85	GND	Open	Open	Open	Open	Open	2.45	GND	Open	Open	Open	Open	GND
0.90	Open	GND	Open	Open	Open	Open	2.50	Open	GND	Open	Open	Open	GND
0.95	GND	GND	Open	Open	Open	Open	2.55	GND	GND	Open	Open	Open	GND
1.00	Open	Open	GND	Open	Open	Open	2.60	Open	Open	GND	Open	Open	GND
1.05	GND	Open	GND	Open	Open	Open	2.65	GND	Open	GND	Open	Open	GND
1.10	Open	GND	GND	Open	Open	Open	2.70	Open	GND	GND	Open	Open	GND
1.15	GND	GND	GND	Open	Open	Open	2.75	GND	GND	GND	Open	Open	GND
1.20	Open	Open	Open	GND	Open	Open	2.80	Open	Open	Open	GND	Open	GND
1.25	GND	Open	Open	GND	Open	Open	2.85	GND	Open	Open	GND	Open	GND
1.30	Open	GND	Open	GND	Open	Open	2.90	Open	GND	Open	GND	Open	GND
1.35	GND	GND	Open	GND	Open	Open	2.95	GND	GND	Open	GND	Open	GND
1.40	Open	Open	GND	GND	Open	Open	3.00	Open	Open	GND	GND	Open	GND
1.45	GND	Open	GND	GND	Open	Open	3.05	GND	Open	GND	GND	Open	GND
1.50	Open	GND	GND	GND	Open	Open	3.10	Open	GND	GND	GND	Open	GND
1.55	GND	GND	GND	GND	Open	Open	3.15	GND	GND	GND	GND	Open	GND
1.60	Open	Open	Open	Open	GND	Open	3.20	Open	Open	Open	Open	GND	GND
1.65	GND	Open	Open	Open	GND	Open	3.25	GND	Open	Open	Open	GND	GND
1.70	Open	GND	Open	Open	GND	Open	3.30	Open	GND	Open	Open	GND	GND
1.75	GND	GND	Open	Open	GND	Open	3.35	GND	GND	Open	Open	GND	GND
1.80	Open	Open	GND	Open	GND	Open	3.40	Open	Open	GND	Open	GND	GND
1.85	GND	Open	GND	Open	GND	Open	3.45	GND	Open	GND	Open	GND	GND
1.90	Open	GND	GND	Open	GND	Open	3.50	Open	GND	GND	Open	GND	GND
1.95	GND	GND	GND	Open	GND	Open	3.55	GND	GND	GND	Open	GND	GND
2.00	Open	Open	Open	GND	GND	Open	3.60	Open	Open	Open	GND	GND	GND
2.05	GND	Open	Open	GND	GND	Open	3.65	GND	Open	Open	GND	GND	GND
2.10	Open	GND	Open	GND	GND	Open	3.70	Open	GND	Open	GND	GND	GND
2.15	GND	GND	Open	GND	GND	Open	3.75	GND	GND	Open	GND	GND	GND
2.20	Open	Open	GND	GND	GND	Open	3.80	Open	Open	GND	GND	GND	GND
2.25	GND	Open	GND	GND	GND	Open	3.85	GND	Open	GND	GND	GND	GND
2.30	Open	GND	GND	GND	GND	Open	3.90	Open	GND	GND	GND	GND	GND
2.35	GND	GND	GND	GND	GND	Open	3.95	GND	GND	GND	GND	GND	GND

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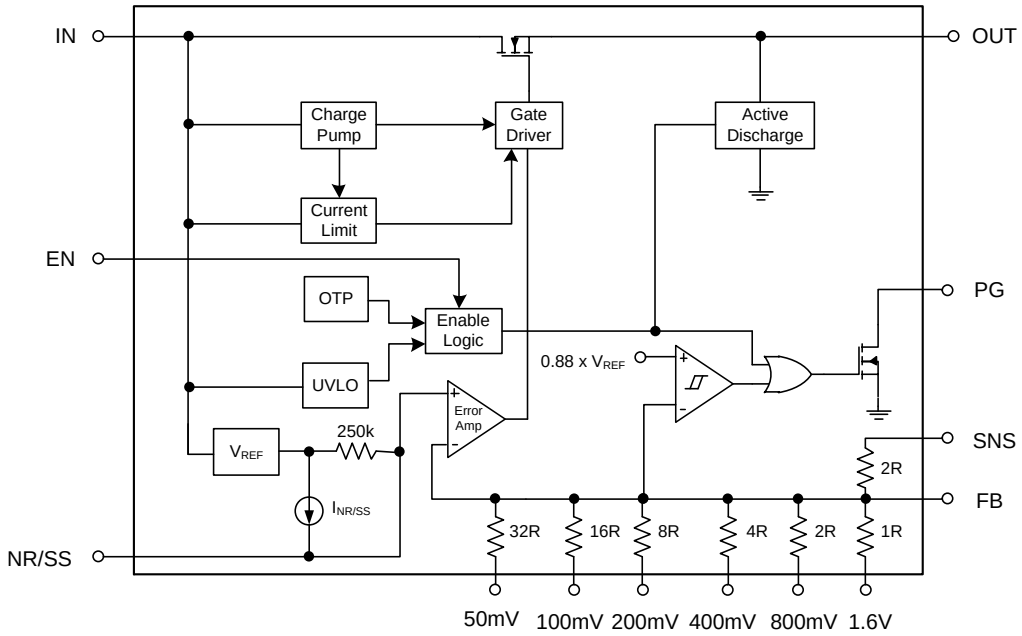
Pin Descriptions

Pin Number	Pin Name	Function
1, 19, 20	OUT	LDO output pin. Connect a 47µF or larger ceramic capacitor (22µF or greater of capacitance) is required for stability and the output capacitor as close to the device as possible to minimize the impedance between OUT pin to load.
2	SNS	Output voltage sense input pin. Connect this pin to OUT only if using the programmed output voltage function (set the output voltage via PCB layout). If the OUT voltage is set by external resistor, leave this pin floating.
3	FB	Feedback voltage pin connected to the error amplifier. This pin is used to set the output voltage by an external resistive divider. The typically reference voltage is 0.8V.
4	PG	Output voltage power good indicator pin. Active-high with open-drain outputs when output voltage reaches 88% of the target. The pin is pulled to ground when the output voltage is lower than threshold, EN pulled down, OCP and OTP.
5, 6, 7, 9, 10, 11	50mV, 100mV, 200mV, 400mV, 800mV, 1.6V	Output voltage setting pins. Connect these pins to ground or leave floating. Connecting theses pins to ground increases the output voltage; multiple pins can be simultaneously connected to GND to select the desired output voltage. Leaves these pins floating (open) when not in use.
8,18, 21 (Exposed Pad)	GND	Ground pin. These pins must be connected to ground. The exposed pad solders to ground with large PCB to enhance the power dissipation.
12	NC	No internal connection. Leave this pin floating doesn't affect the chip functionality.
13	NR/SS	Noise-reduction and soft-start pin. This pin Connect an external capacitor to ground reduce the reference voltage noise and slow down the output voltage rise as a soft-start. A 10nF or larger capacitor connects between NR/SS to ground for low noise applications.
14	EN	Enable pin. Connecting this pin to logic high enables the device or connecting this pin to logic low disables the device. If enable functionality is required; connecting high with EN pin after V_{IN} voltage is established. Connecting EN pin to V_{IN} always, if the enable functionality is not required
15, 16, 17	IN	Input supply voltage pin. Connecting a 47µF or large ceramic capacitor from IN to ground as close as possible to get better noise rejection performance.

Functional Block Diagram



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Feature Descriptions

Operation

The AP7179D operates with single supply input range from 1.1V to 6.5V and is capable of delivering 3A current to output. The device has a high PSRR, and its low noise provides a clean supply to the application.

A low-noise reference and error amplifier are included to reduce device noise. The $C_{NR/SS}$ capacitor filters the noise from the reference and the C_{FF} feed-forward capacitor filters the noise from the error amplifier. The power-supply rejection ratio (PSRR) of the AP7179D minimizes the coupling of input supply noise to the output. The combination of a low noise-floor and high PSRR ensure that the device provides a clean supply to the application.

Enable and Shutdown

The AP7179D provides an EN pin, as an external chip enable control, to enable or disable the device. A V_{EN} below 0.5V turns the regulator off and enters shutdown mode. When the V_{EN} is above 1.1V, it turns the regulator on. When the regulator is shut down, the ground current is reduced to a maximum of 25μA. The enable circuitry has hysteresis (typically 50mV) with relatively slow, ramping analog signals. When the enable function is not desired, the EN must be tied as close as possible to the VIN \ to prevent voltage drops on the VIN line from triggering the enable circuit.

VOUT Programming Pins

The AP7179D's built-in matched feedback resistor network sets the output voltage. The output voltage can be programmed from 0.8V to 3.95V, with 50mV steps by tying programming pins 5 to 11 to the ground. Tying any of the VOUT programming pins to SNS can lower the value of the upper resistor divider and increase programming resolution.

Power Good

The power-good circuit monitors the feedback pin voltage to indicate the status of the output voltage. The open-drain PGOOD pin requires an external pull-up resistor to an external supply, any downstream device can receive power-good as a logic signal for sequencing. A pull-up resistor from 10kΩ to 100kΩ is recommended. Make sure that the external pull-up supply voltage results in a valid logic signal for the receiving device.

After start-up, the PGOOD pin has a high impedance when the feedback voltage exceeds V_{PGOOD_HYS} (typically 88.3% of 0.8V reference voltage level). The PGOOD is pulled to GND when the feedback pin voltage falls below the V_{IT_PGOOD}.

Programmable Soft-Start

Soft-start refers to the ramp-up time of the output voltage during LDO turn-on after EN and V_{UVLO} exceed the respective threshold voltage. The AP7179D activates a quick-start circuit to charge the noise reduction capacitor ($C_{NR/SS}$) and then the output voltage ramps up. The noise reduction capacitor ($C_{NR/SS}$) accomplishes both noise-reduction and the soft-start ramp-time programming during turn-on.

Undervoltage Lockout (UVLO)

The UVLO circuit monitors the input voltage to prevent the device from turning on before the VIN rises above the V_{UVLO} threshold. The UVLO circuit also disables the output of the device when VIN falls below the lockout voltage ($V_{UVLO} - V_{HYS}$). The UVLO circuit responds quickly to glitches on the VIN and will attempt to disable the output of the device if the VIN collapses.

Internal Current Limit (I_{LIM})

The AP7179D continuously monitors the output current to protect the pass transistor against high-load current faults or shorting events. When encountering an abnormal condition, the LDO sources constant current to limit the output within the predefined range. Thermal shutdown can activate during a current-limit event because of the high power dissipation typically found in these conditions. To ensure proper operation of the current limit, minimize the inductances to the input and load. Continuous operation in current limit is not recommended.

By reason of the built-in body diode, the pass transistor conducts current when the output voltage exceeds input voltage. Since the current is not limited here, external current protection should be added if the device may work in a reverse voltage state.

Overtemperature Protection (OTP)

The AP7179D implements thermal shutdown protection. The device is disabled when the junction temperature (T_J) exceeds 160°C (typical). Thermal shutdown hysteresis ensures that the LDO resets again (turns on) when the temperature falls to 140°C (typical). Continuously running the AP7179D into thermal shutdown or above a junction temperature of 125°C reduces long-term reliability.

Output Active Discharge

When the device is disabled, the AP7179D discharges the LDO output (via VOUT pins) through an internal pulldown MOSFET that connects a resistance of several hundred ohms to ground.

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can possibly flow from the output to the input. External current protection should be added if the device may work at a reverse voltage state.

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Absolute Maximum Ratings (Note 4) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Ratings	Unit
ESD HBM	Human Body Mode ESD Protection	2	kV
CDM	Charged Device Model	500	V
V_{IN}	Input Voltage	-0.3 to 7	V
V_{EN}	Input Voltage for EN Pin	-0.3 to 7	V
V_{PG}	Power Good Indictor Voltage	-0.3 to 7	V
V_{OUT}	Output Voltage	-0.3 to V_{IN} + 0.3	V
$V_{NR/SS}$	$V_{NR/SS}$ Pin Voltage	-0.3 to 2	V
V_{FB}	Feedback Pin Voltage	-0.3 to 2	V
T_J	Operating Junction Temperature	150	°C
T_{STG}	Storage Temperature	-55 to +150	°C
θ_{JA}	Thermal Resistance Junction to Ambient (θ_{JA})	65.4	°C/W

Notes: 4. a). Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended period may affect device reliability.

b). Ratings apply to ambient temperature at +25°C. The JEDEC High-K board design used to derive this data was a 3 inch x 3 inch multilayer board with 1oz. internal power and ground planes and 2oz. copper traces on the top and bottom of the board.

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
V_{IN}	Input Voltage	1.1	6.5	V
I_{OUT}	Each Channel Output Current	0	3	A
T_J	Operating Junction Temperature	-40	+125	°C

Electrical Characteristics

Over operating temperature range (T_J = −40°C to 125°C), (1.1V ≤ V_{IN} < 6.5V and V_{IN} ≥ $V_{OUT(TARGET)}$ + 0.3 V, $V_{OUT(TARGET)}$ = 0.8V, V_{OUT} connected to 50Ω to GND, V_{EN} = 1.1 V, C_{IN} = 10µF, COUT = 47µF, $C_{NR/SS}$ = 0nF, C_{FF} = 0nF, and PG pin pulled up to V_{IN} with 100 kΩ, unless otherwise noted. (Note 5)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		1.1	--	6.5	V
Feedback Reference Voltage	V_{FB}		--	0.8	--	V
NR/SS Pin Voltage	$V_{NR/SS}$		--	0.8	---	V
Undervoltage Lock-Out	V_{UVLO}	V_{IN} increasing	--	1.02	1.085	V
	V_{HYS}	Hysteresis	--	150	--	mV
Output Voltage Range		Using voltage setting pins (50mV, 100mV, 200mV, 400mV, 800mV, and 1.6V)	0.8 -1%	--	3.95+ 1%	V
		Using external resistors	0.8 - 1%	--	5 + 1%	V
Output Voltage Accuracy (Note 6)	V_{OUT}	V_{IN} = V_{OUT} + 0.3V, 0.8V ≤ V_{OUT} ≤ 5V, 5mA ≤ I_{OUT} ≤ 3A	-1	--	1	%
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	I_{OUT} = 5mA, 1.4V ≤ V_{IN} ≤ 6.5 V	--	0.05	--	%/V
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	5mA ≤ I_{OUT} ≤ 3A	--	0.08	--	%/A
Dropout Voltage	V_{DROP}	V_{IN} = 1.1V to 6.5V, I_{OUT} = 3A, V_{FB} = 0.8V - 3%	--	110	180	mV
Output Current Limit	I_{LIM}	V_{OUT} = 90% $V_{OUT(TARGET)}$, V_{IN} = $V_{OUT(TARGET)}$ + 0.4V	3.7	4.2	4.7	A

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Electrical Characteristics (continued)

Over operating temperature range (T_J = −40°C to 125°C), (1.1V ≤ V_{IN} < 6.5V and V_{IN} ≥ $V_{OUT(TARGET)}$ + 0.3 V, $V_{OUT(TARGET)}$ = 0.8V, V_{OUT} connected to 50Ω to GND, V_{EN} = 1.1 V, C_{IN} = 10µF, COUT = 47µF, $C_{NR/SS}$ = 0nF, C_{FF} = 0nF, and PG pin pulled up to V_{IN} with 100 kΩ, unless otherwise noted. (Note 5)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Short-circuit Current Limit	I_{SC}	R_{LOAD} = 20 mΩ			1.0		A
Ground Pin Current	I_{GND}	Minimum load, V_{IN} = 6.5V, I_{OUT} = 5mA		--	2.8	4	mA
		Maximum load, V_{IN} = 1.4V, I_{OUT} = 3A		--	4.2	5.5	
		Shutdown, PG = Open, V_{IN} = 6.5V, V_{EN}= 0.5V		--	--	25	µA
EN Pin Current	I_{EN}	V_{IN} = 6.5V, V_{EN} = 0V and 6.5V		-0.1	--	0.7	µA
EN Pin High-Level Input Voltage	V_{EN_H}	Enable device		1.1	--	6.5	V
EN Pin Low-Level Input Voltage	V_{EN_L}	Disable device		0	--	0.5	
PG Pin Threshold	V_{IT_PG}	For the direction PG signal falling with decreasing V_{OUT}		0.82 x V_{OUT}	0.883 x V_{OUT}	0.93 x V_{OUT}	V
PG Pin Hysteresis	V_{PG_HYS}	For PG signal rising		--	0.01 x V_{OUT}	--	V
PG Pin Low- Level Output Voltage	V_{PG_L}	V_{OUT} < V_{IT_PG}, I_{PG} = -1mA (current into device)		--	--	0.4	V
PG Pin Leakage Current	I_{PG_LK}	V_{OUT} > V_{IT_PG} , V_{PG} = 6.5V		--	--	1	µA
NR/SS Pin Charging Current	$I_{NR/SS}$	$V_{NR/SS}$ = GND, V_{IN} = 6.5V		4	6.2	9	µA
FB Pin Leakage Current	I_{FB}	V_{IN} = 6.5V		-100	--	100	nA
Power Supply Rejection Ratio	PSRR	V_{IN} - V_{OUT} = 0.4V, I_{OUT} = 3A, $C_{NR/SS}$ = 100nF, C_{FF} = 10nF, C_{OUT} = 47µF || 10µF || 10µF	f = 10kHz, V_{OUT} = 0.8V	--	42	--	dB
			f = 500kHz, V_{OUT} = 0.8V	--	39	--	
			f = 10kHz, V_{OUT} = 5V	--	40	--	
			f = 500kHz, V_{OUT} = 5V	--	25	--	
Output Noise Voltage	V_n	BW = 10Hz to 100kHz, I_{OUT} = 3A, $C_{NR/SS}$ = 100nF, C_{FF} = 10nF, C_{OUT} = 47µF || 10µF || 10µF	V_{IN} = 1.1V, V_{OUT} = 0.8V	--	4.4	--	μV_{RMS}
			V_{OUT} = 5 V		7.7		
Thermal Shutdown Threshold	T_{SD}	Temperature increasing		--	160	--	°C
		Temperature decreasing		--	140	--	
Thermal Resistance Junction to Case (θ_{JC}) (Note 4)	θ_{JC}			--	3.68	--	°C/W

Notes: 5. $V_{OUT(TARGET)}$ is the expected VOUT value set by the external feedback resistors. The 50Ω load is disconnected when the test conditions specify an IOUT value.
6. External resistor tolerance is not taken into account.

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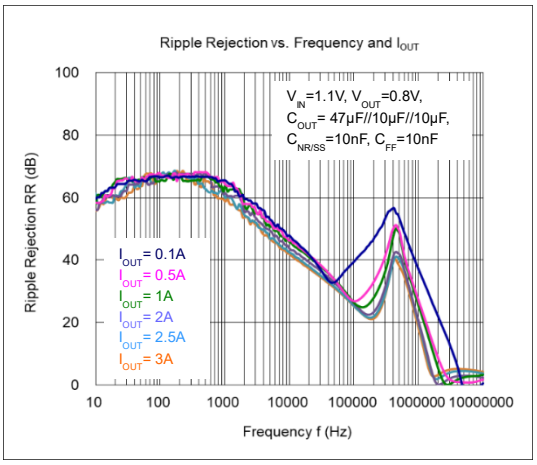
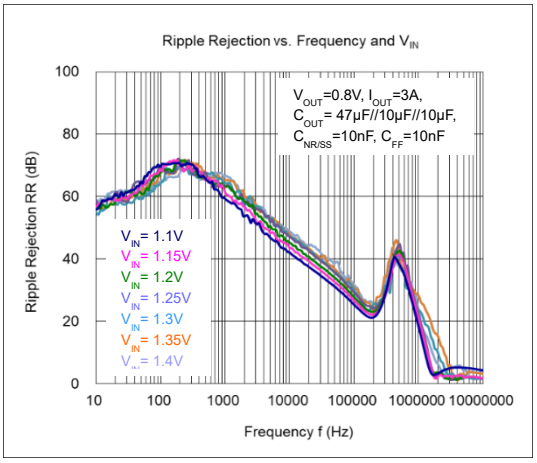
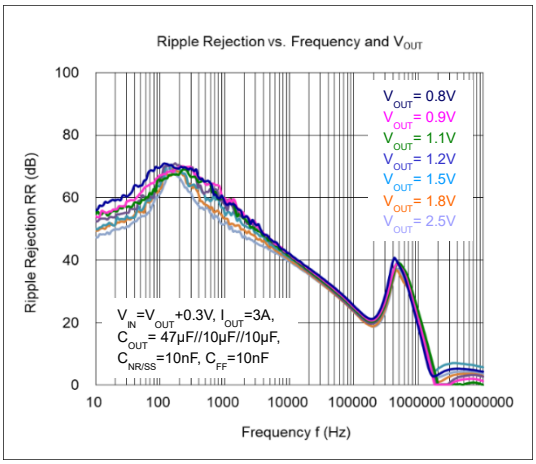
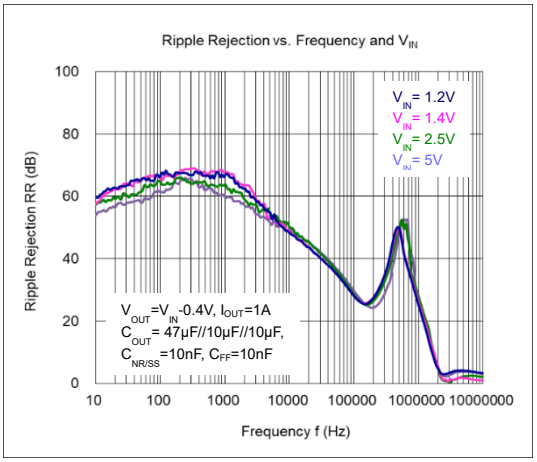
Typical Performance Characteristics

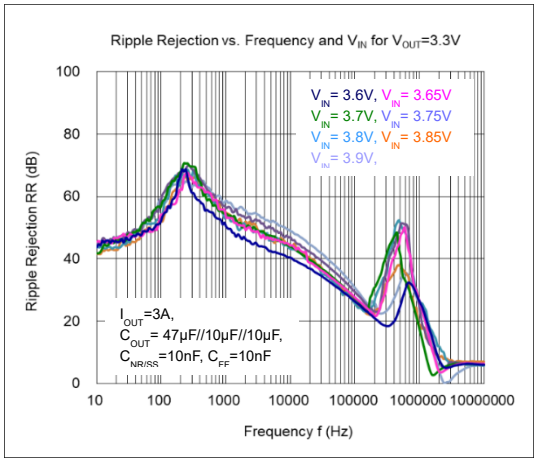
At T_A = 25°C, V_{IN} = 1.1 V or V_{IN} = $V_{OUT(NOM)}$ + 0.3 V (whichever is greater), $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1V, C_{IN} = 10µF, C_{OUT} = 47µF, $C_{NR/SS}$ = 0nF, C_{FF} = 0nF, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted)

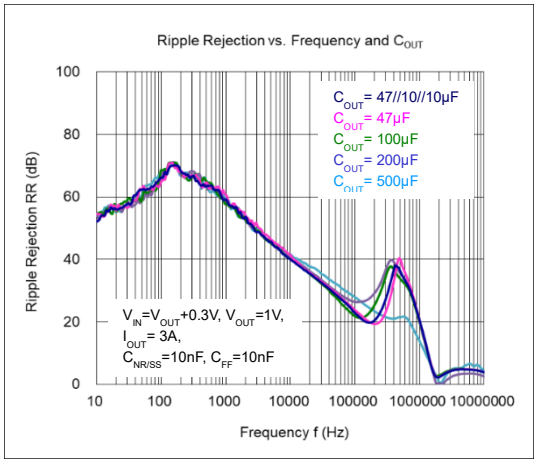












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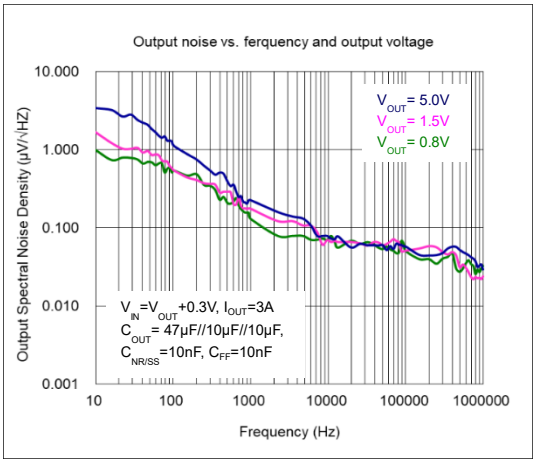
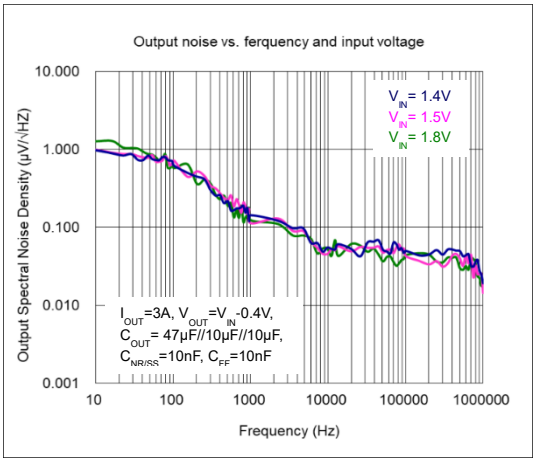
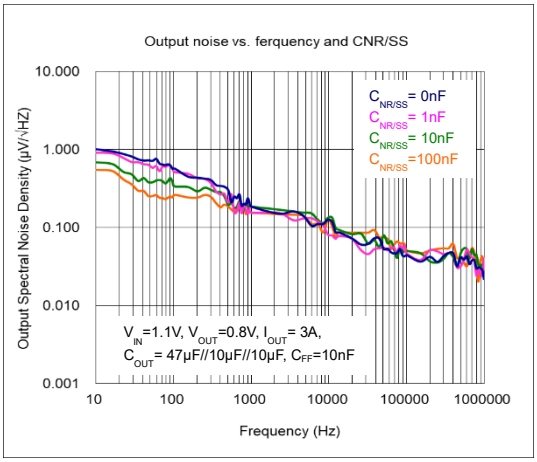
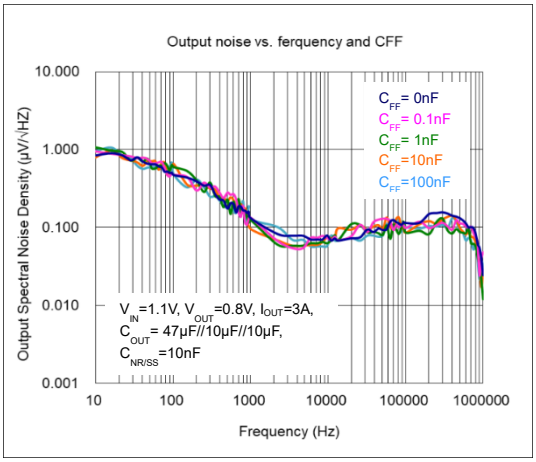
Typical Performance Characteristics (continued)

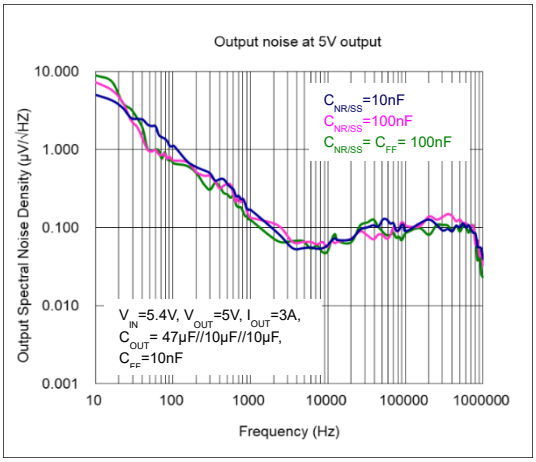
At T_A = 25°C, V_{IN} = 1.1 V or V_{IN} = $V_{OUT(NOM)}$ + 0.3 V (whichever is greater), $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1V, C_{IN} = 10µF, C_{OUT} = 47µF, $C_{NR/SS}$ = 0nF, C_{FF} = 0nF, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted)

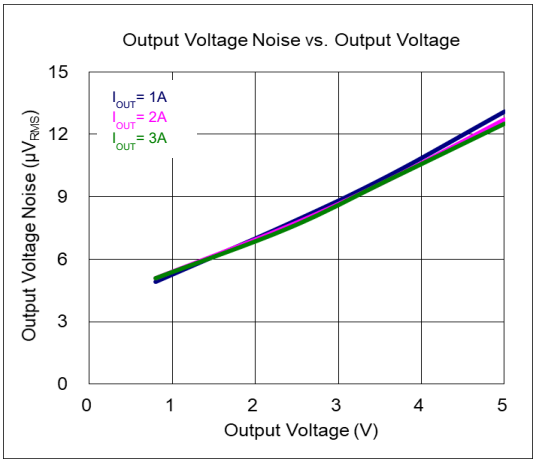












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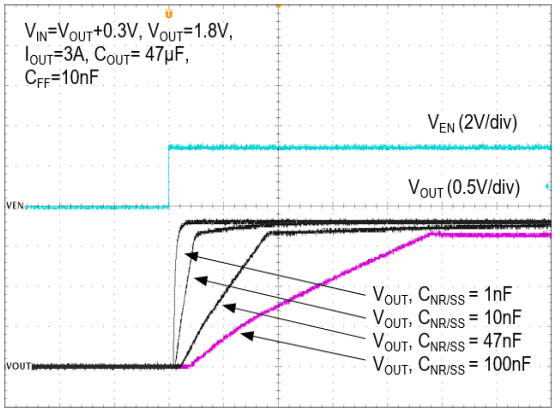
Typical Performance Characteristics (continued)

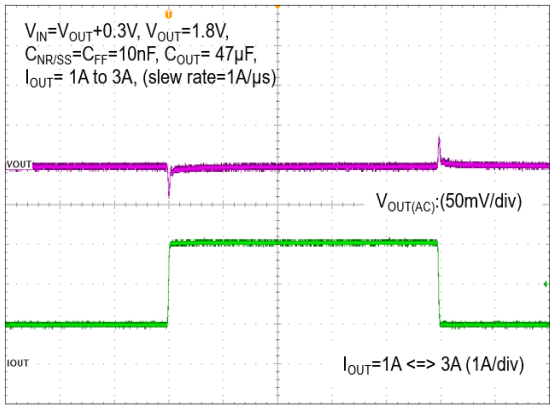
At T_A = 25°C, V_{IN} = 1.1 V or V_{IN} = $V_{OUT(NOM)}$ + 0.3 V (whichever is greater), $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1V, C_{IN} = 10µF, C_{OUT} = 47µF, $C_{NR/SS}$ = 0nF, C_{FF} = 0nF, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted)

Power up response



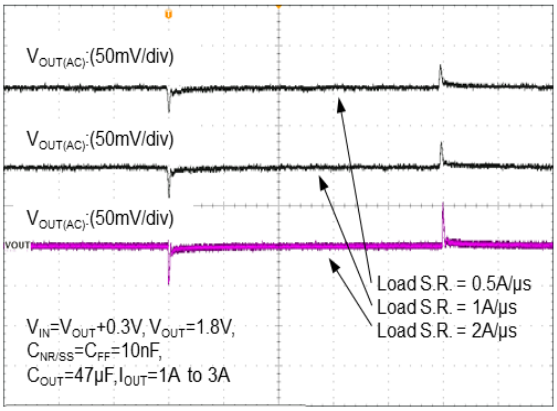
Time (4ms/div)

Load transient response



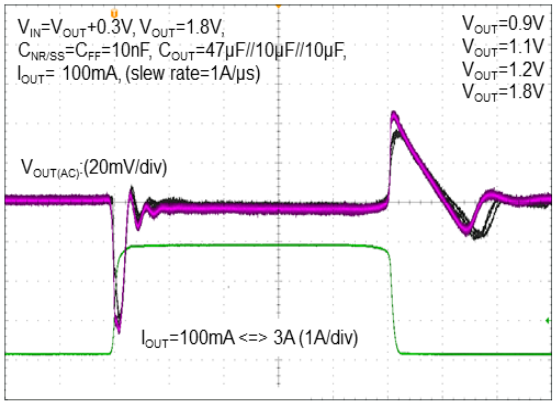
Time (100µs/div)

Load transient response vs. load slew rate



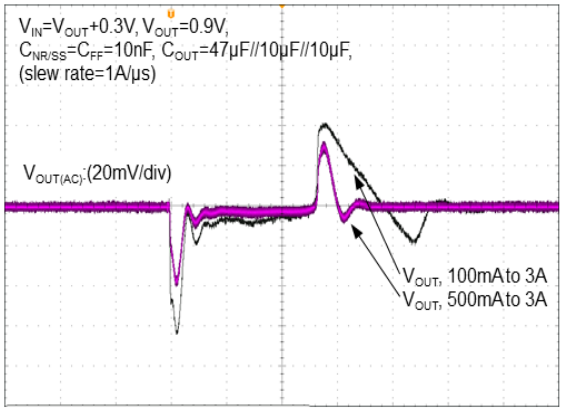
Time (100µs/div)

Load transient response vs. V_{OUT}

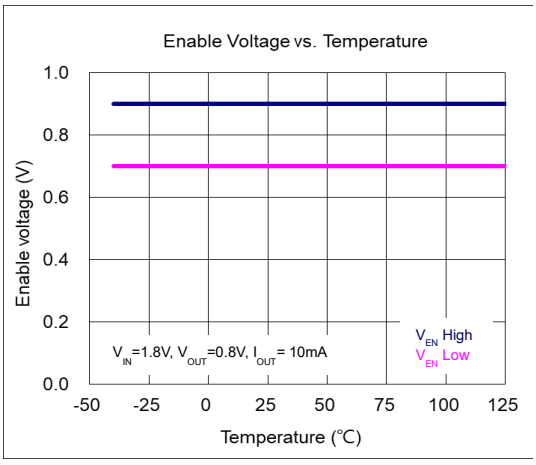


Time (20µs/div)

Load transient response vs. DC load



Time (20µs/div)



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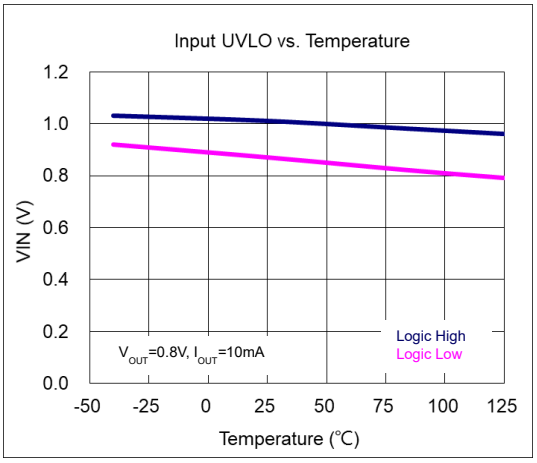
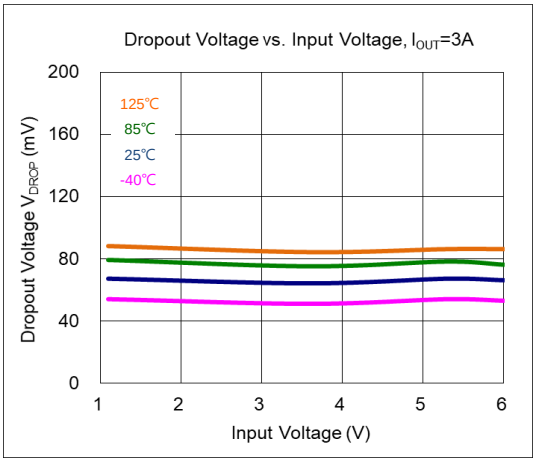
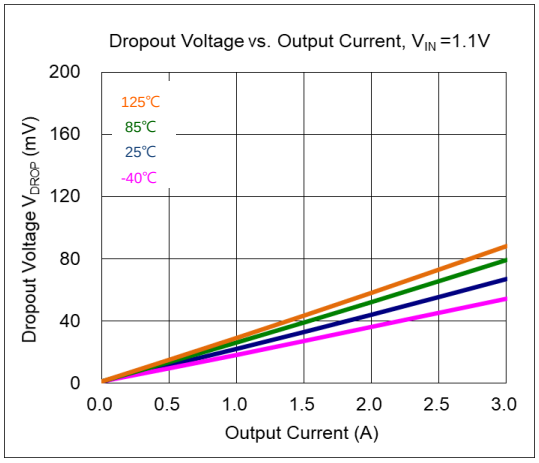
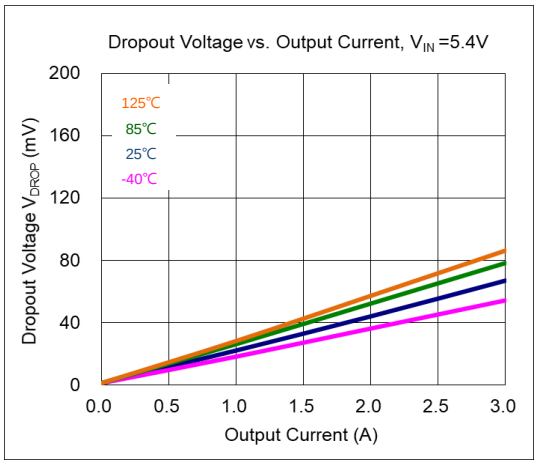
Typical Performance Characteristics (continued)

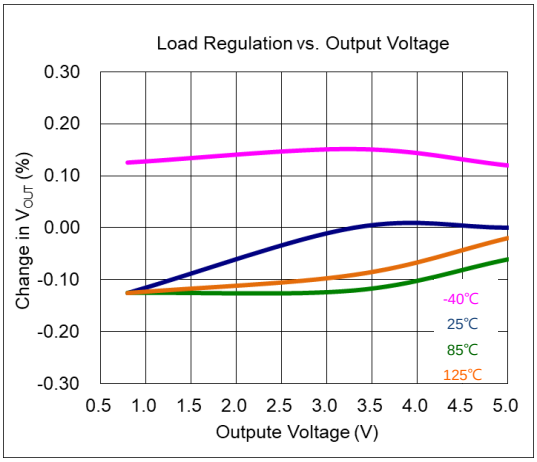
At T_A = 25°C, V_{IN} = 1.1 V or V_{IN} = $V_{OUT(NOM)}$ + 0.3 V (whichever is greater), $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1V, C_{IN} = 10µF, C_{OUT} = 47µF, $C_{NR/SS}$ = 0nF, C_{FF} = 0nF, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted)

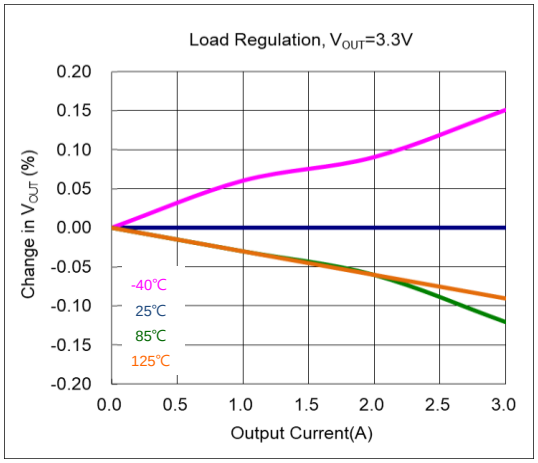












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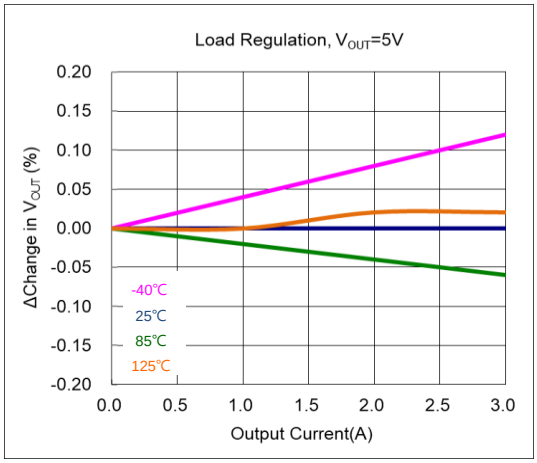
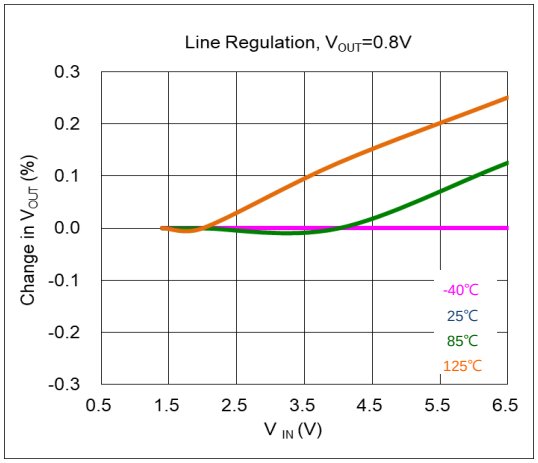
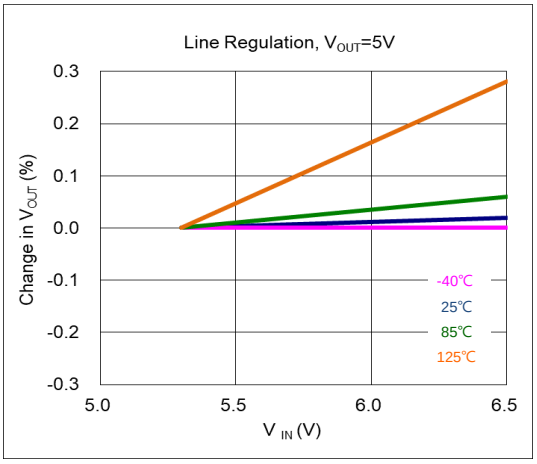
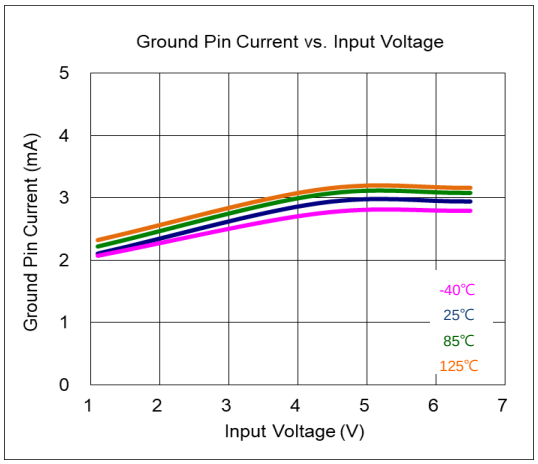
Typical Performance Characteristics (continued)

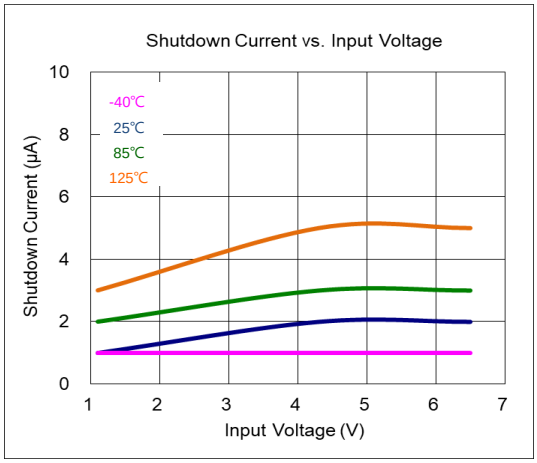
At T_A = 25°C, V_{IN} = 1.1 V or V_{IN} = $V_{OUT(NOM)}$ + 0.3 V (whichever is greater), $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1V, C_{IN} = 10µF, C_{OUT} = 47µF, $C_{NR/SS}$ = 0nF, C_{FF} = 0nF, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted)

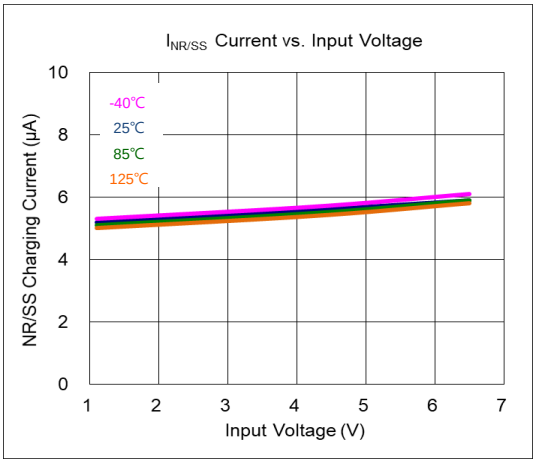












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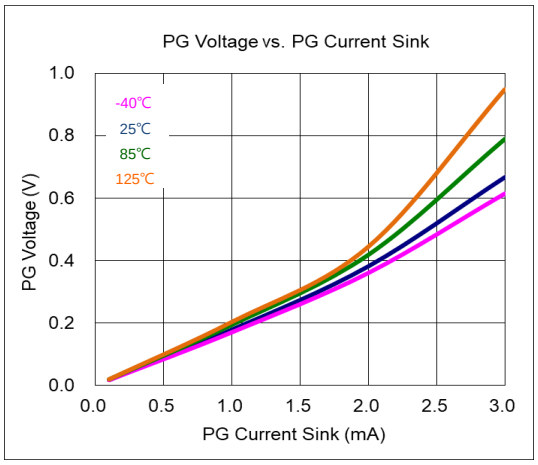
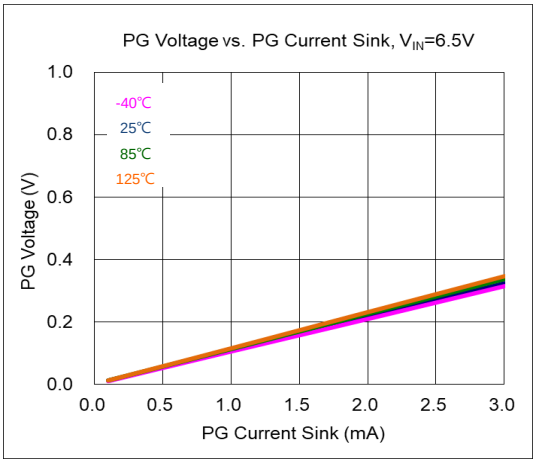
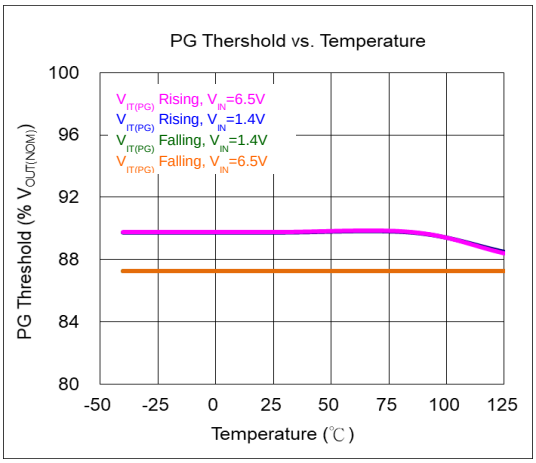
Typical Performance Characteristics (continued)

At T_A = 25°C, V_{IN} = 1.1 V or V_{IN} = $V_{OUT(NOM)}$ + 0.3 V (whichever is greater), $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1V, C_{IN} = 10μF, C_{OUT} = 47μF, $C_{NR/SS}$ = 0nF, C_{FF} = 0nF, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted)







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Application Information

Overview

The AP7179D is a high-current, low-noise, high-accuracy, low-dropout linear regulator with a 3A maximum output current. The device features an input-voltage operating range from 1.1V to 6.5V, and an adjustable output voltage (0.8V to 5.5V via external resistor setting or 0.8V to 3.95V from the PCB layout) to short specific pins and maintain the required output voltage.

Output Voltage Setting

The output voltage of the AP7179D can be set by external resistors or by output voltage setting pins (50mV, 100mV, 200mV, 400mV, 800mV, and 1.6V) to achieve different output targets. Using external resistors, the values of R1 and R2 use the equation below:

$$V_{OUT} = 0.8 \times (1 + \frac{R1}{R2})$$

The application circuit is determined by the values of R1 and R2, seen in Figure 3.

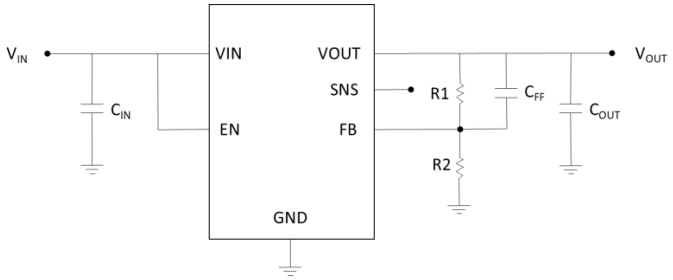
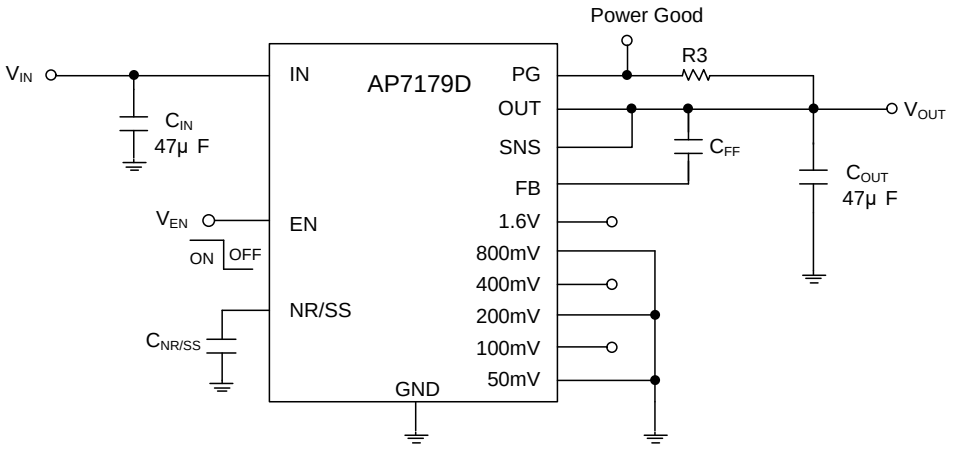


Figure 3. Output voltage set by external resistors

The AP7179D can program the regulated output voltage by shorting pins 5, 6, 7, 8, 9, 10, and 11 to ground without external resistors, while the SNS pin connects with VOUT pin. Pins 5, 6, 7, 9, 10, and 11 are connected with internal resistor pairs, where each pin is either connected to the ground (active) or left open (floating).

Voltage programming is set as the sum of the internal reference voltage (V_{REF} = 0.8V) and the accumulated sum of the respective voltages assigned to each active pin, seen in Figure 4.



$V_{OUT} = V_{REF} + 50mV + 200mV + 800mV = 0.8V + 50mV + 200mV + 800mV = 1.85V$

Figure 4. Output voltage set by programing pins

Table 2 summarizes these voltage values associated with each active pin setting. The output minimum voltage is equal to V_{REF} (0.8V) when all program pins are open. The maximum output can be up to 3.95V after all pins short to ground.

Dropout Voltage

The dropout voltage refers to the minimum voltage difference between the input and output voltage ($V_{DO} = V_{IN} – V_{OUT}$) required for regulation.

For normal operation, the suggested LDO operating range is ($V_{IN} > V_{OUT} + V_{DROP}$) to maintain good transient response and PSRR ability. When VIN drops below the required V_{DO} for the given load current, the device functions as a resistive switch and does not regulate output voltage.

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Application Information (continued)

C_{IN} and C_{OUT} Selection

The AP7179D is designed to support low ESR (equivalent series resistance) ceramic capacitors. The X7R, X5R, and COG-rated ceramic capacitors are recommended due to their good capacitive stability across temperatures. The Y5V-rated capacitor is discouraged because of its large variations in capacitance.

However, ceramic capacitance varies with operating voltage and temperature. Ceramic capacitors are usually recommended to have a voltage derating of 50%. A 47µF or greater ceramic capacitor (or 22µF effective capacitance) for the output is suggested to ensure stability. Input capacitance is selected to minimize transient input droop during load current steps. An input capacitor of at least 47µF is highly recommended for minimal input impedance. If the trace inductance between the AP7179D input supply is high, an available option is to add more input capacitors to restrict ringing and prevent the device from exceeding absolute maximum ratings.

It is generally recommended to use a 47µF 0805-sized ceramic capacitor in parallel with two 10µF 0805-sized ceramic capacitors that meet the minimum effective capacitance at high input-voltage and high output-voltage requirements. Place these capacitors as close as possible to the pins for optimum performance and stability.

Feed-Forward Capacitor (C_{FF})

The AP7179D is designed to be stable without the external feed-forward capacitor (C_{FF}). A 10nF external feed-forward capacitor optimizes the transient, noise, and PSRR performance. A higher capacitance C_{FF} can be also used, but the start-up time is longer and the power-good signal can incorrectly indicate that the output voltage is settled.

Soft-Start and Noise Reduction ($C_{NR/SS}$)

The AP7179D features a programmable, monotonic soft-start time for output rising, which can be achieved via an external capacitor ($C_{NR/SS}$) on the NR/SS pin. Using an external $C_{NR/SS}$ is recommended for general application. Minimizing in-rush current into the output capacitors also helps reduce the noise component from internal reference. The error amplifier of the AP7179D tracks the voltage ramp of the external soft-start capacitor ($C_{NR/SS}$) until the voltage approaches the internal reference 0.8V. The soft-start ramp time can be calculated with Equation 1 and depends on the soft-start charging current ($I_{NR/SS}$), the soft-start capacitance ($C_{NR/SS}$), and the internal reference (V_{REF}).

$$t_{SS} = \frac{(V_{REF} \times C_{NR/SS})}{I_{NR/SS}} \quad (1)$$

For noise-reduction consideration, the $C_{NR/SS}$ in conjunction with an internal noise-reduction resistor forms a low-pass filter (LPF) that filters out noise from the internal bandgap reference, before being gained up via the error amplifier. This reduces the total device noise floor. For low-noise applications, a 10nF to 1µF $C_{NR/SS}$ is recommended.

Input Inrush Current

In-rush current is defined as the current into the LDO at the IN pin during start-up and consists of the sum of the load current and the charging current of the output capacitor. Because the input capacitor must be removed to measure inrush current, this method is not recommended. Generally, the soft-start inrush current can be estimated by Equation 2 below.

$$I_{OUT}(t) = \frac{(C_{OUT} \times dV_{OUT}(t))}{dt} + \left(\frac{V_{OUT}(t)}{R_{LOAD}}\right) \quad (2)$$

Where:

- $V_{OUT}(t)$ is the instantaneous output voltage of the turn-on ramp
- $dV_{OUT}(t) / dt$ is the slope of the V_{OUT} ramp
- R_{LOAD} is the resistive load impedance.

Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) threshold is the minimum input operational voltage range that ensures the device stays disabled and shut down when input voltage collapses. Three input voltage events may occur in the application; assuming $V_{EN} \geq V_{EN\_H}$ in all situations.

(1) Input power starts rising and V_{IN} over the V_{UVLO} rising threshold, the V_{OUT} powers on then reaches the target level and is under-regulated.
(2) Assuming the V_{IN} instant power line is unstable and droops severely, the V_{IN} droop level is not lower than the V_{UVLO} falling threshold, the device maintains normal work status, and the V_{OUT} still under-regulated.
(3) V_{IN} droop level is lower than UVLO falling threshold, the control loop of the device is disabled and does not have regulation ability, the V_{OUT} drops in the meantime.

For general applications, instant power line transient with a long power trace between VIN pin may maintain the V_{IN} level under UVLO threshold, making the output voltage collapse. In this case, use a larger input capacitor to limit the fall-time of the input supply when operating near the minimum V_{IN}.

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Application Information (continued)

Power-Good (PGOOD) Function

Power-Good function monitors the feedback pin voltage and checks if the output voltage is functional or nonfunctional. This feature enables other devices to receive the AP7179D Power-Good signal as a logic signal that can be used for sequence-design application.

The PGOOD pin is an open-drain structure, thus an external pull-up resistor connecting to an external supply is necessary. The pulled-up resistor value between 10kΩ to 100kΩ is recommended for proper operation. The lower limit of 10kΩ results from the maximum pulled-down strength of the power-good transistor, and the upper limit of the 100kΩ results from the maximum leakage current at the power-good node. If the pullup resistor is outside of this range, then the power-good signal may not read a valid digital logic level. The C_{FF} time constant must be greater than the $C_{NR/SS}$ soft-start time constant to ensure proper operation of the PG during start-up.

Reverse Current Protection

If the maximum VOUT exceeds VIN + 0.3V, this may induce reverse current from VOUT to VIN that flows through the body diode of the pass element and cause possible damage. When the output is biased above the input supply voltage level, this makes the VIN < VOUT. An external Schottky diode may be added to prevent the pass element from being damaged by the reverse current, as seen in Figure 5.

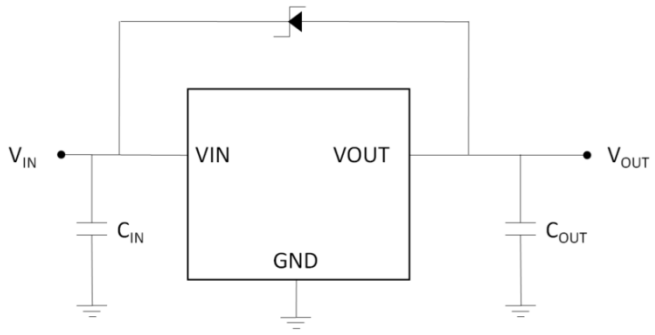

Figure 5. Application circuit for reverse current protection

Thermal Considerations

Thermal protection limits power dissipation in the AP7179D. When power dissipation on the pass element ($P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$) that raises the operating junction temperature exceeds 160°C, the OTP circuit starts the thermal shutdown function and turns the pass element off. The pass element turns on again after the junction temperature drop by 20°C. When the output short circuit occurs, the output voltage will be closed to zero. Overtemperature protection can reduce chip temperature and provide maximum safety to end users when output short circuit occurs.

To avoid permanent damage to the device, the junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the sizing of the thermal plane, and the rate of surrounding airflow. The primary heat conduction path for the package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device.

Power Dissipation

The device power dissipation and proper sizing of the thermal plane connected to the thermal pad is critical to avoid thermal shutdown and ensure reliable operation. Power dissipation of the device depends on input voltage and load conditions, and can be calculated by:

$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$

The maximum power dissipation is handled by the device and depends on the maximum junction to ambient thermal resistance, maximum ambient temperature, and maximum device junction temperature, which can be calculated by the following equation:

$$P_{D(max@T_A)} = \frac{(125℃ - T_A)}{R_{\theta JA}}$$

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Application Information (continued)

Layout Consideration

For best performance of the AP7179D, the recommended PCB layout suggestions are below. All circuit components are placed on the same side of the circuit board and as close as possible to the LDO pins. Place the ground return path connection to the input and output capacitor, with the ground plane connected by a wide copper surface for improved thermal dissipation. It is discouraged to use vias and long power traces for the input and output capacitors connection as this negatively impacts performance. Figure 6 shows an example layout reference that minimizes inductive parasitic, reduces load-current transients, mitigates noise, and maintains good circuit stability.

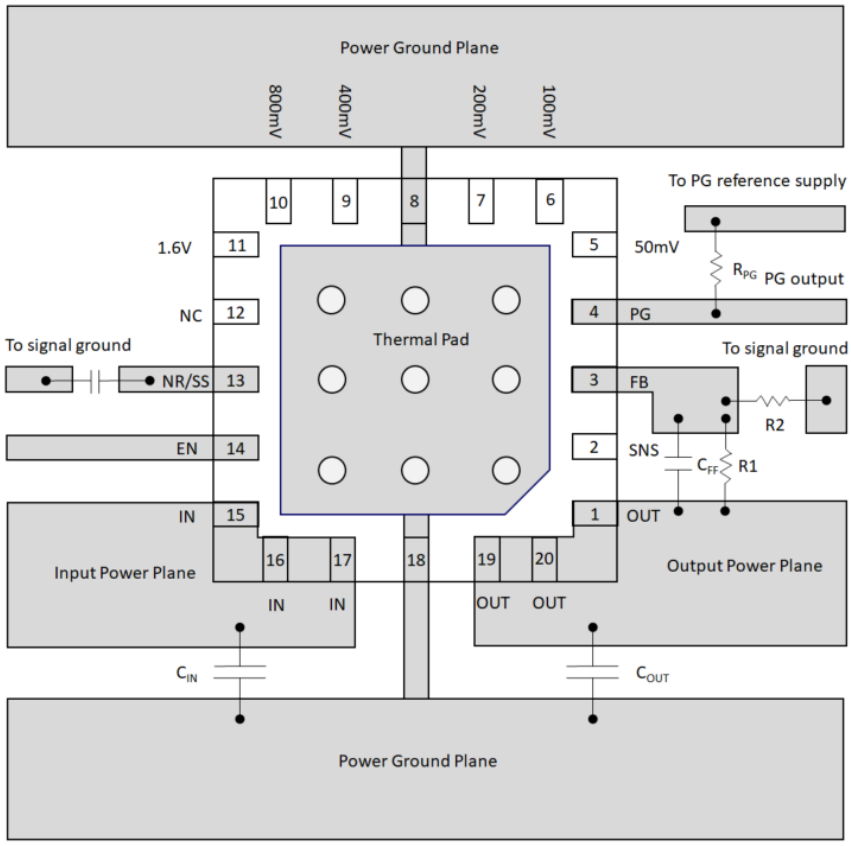

Figure 6. PCB Layout Guide

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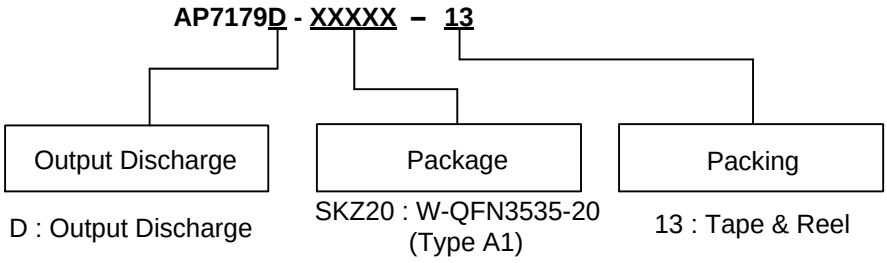
Ordering Information (Note 7)



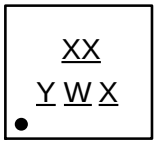
Part Number	Part Number Suffix	Package	Package Code	Packing	
				Qty.	Carrier
AP7179DSKZ20-13	-13	W-QFN3535-20 (Type A1)	SKZ20	5,000	13” Tape & Reel

Note: 7. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information

(1) W-QFN3535-20 (Type A1)

(Top View)



XX : Identification Code
Y : Year : 0~9
W : Week : A~Z : 1~26 week; a~z : 27~52 week; z represents 52 and 53 week
X : Internal Code

Part Number	Package	Identification Code
AP7179DSKZ20-13	W-QFN3535-20 (Type A1)	9D

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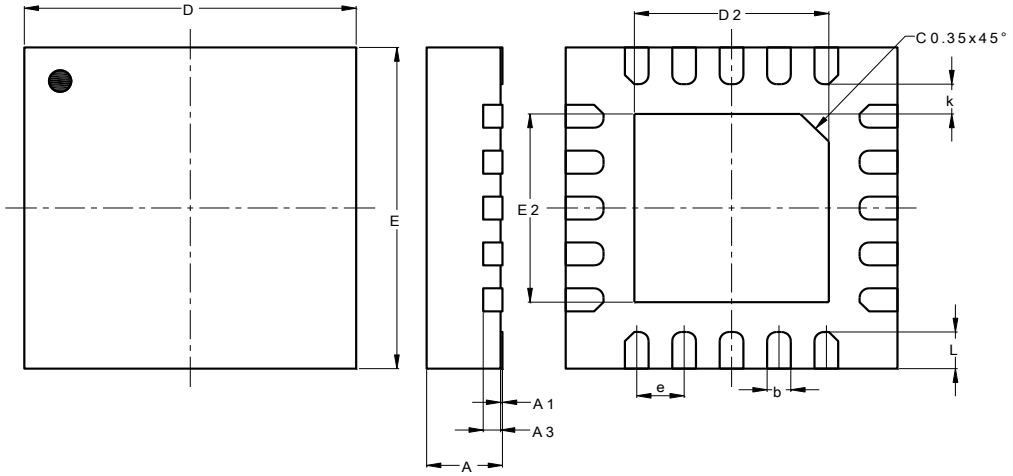
Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-QFN3535-20 (Type A1)



W-QFN3535-20 (Type A1)			
Dim	**Min**	**Max**	**Typ**
A	0.70	0.80	0.75
A1	0.00	0.05	0.02
A3	0.203 REF		
b	0.18	0.30	0.25
D	3.50 BSC		
D2	2.00	2.10	2.05
E	3.50 BSC		
E2	2.00	2.10	2.05
e	0.50 BSC		
k	0.20	--	--
L	0.35	0.45	0.40
All Dimensions in mm			

Suggested Pad Layout

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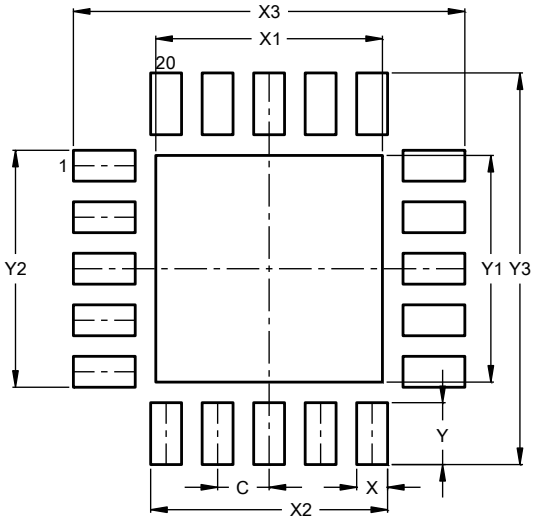
W-QFN3535-20 (Type A1



Dimensions	Value (in mm)
C	0.500
X	0.300
X1	2.200
X2	2.300
X3	3.800
Y	0.600
Y1	2.200
Y2	2.300
Y3	3.800

Mechanical Data

- Moisture Sensitivity: Level 1 Per J-STD-020
- Terminals: Finish - Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.03 grams (Approximate)

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