SY5238

ZVS Flyback SR Controller

General Description

The SY5238 is a Flyback SR controller compatible with QR mode converter to achieve ZVS operation. The primary side PWM converter must work in quasi resonant mode. The SY5238 adopts proprietary operation mode to achieve flyback ZVS turn on, which greatly improves Flyback efficiency and power density. The SY5238 also adopts adaptive gate voltage control for safe operation.

The SY5238 adopts DSEN voltage falling slope rate detecting technology to avoid SR MOSFET false turn on by parasitic ring under DCM or QR mode.

The SY5238 is available in a DFN2*3-8 package.

Features

- Proprietary Operation Mode for Flyback ZVS
- High Efficiency, High Power Density
- Adaptive Gate Voltage Control
- DSEN Falling Slope Rate Detecting to Prevent SR False Trigger
- 130V DSEN Pin to Directly Sense DRAIN Voltage of SR MOS
- Power Saving Mode to Improve Light Load Efficiency
- Dual Power Supply Channel for 3.3V to 21V Output Systems

Applications

- USB PD, Fast Charger
- Adaptor

Typical Applications

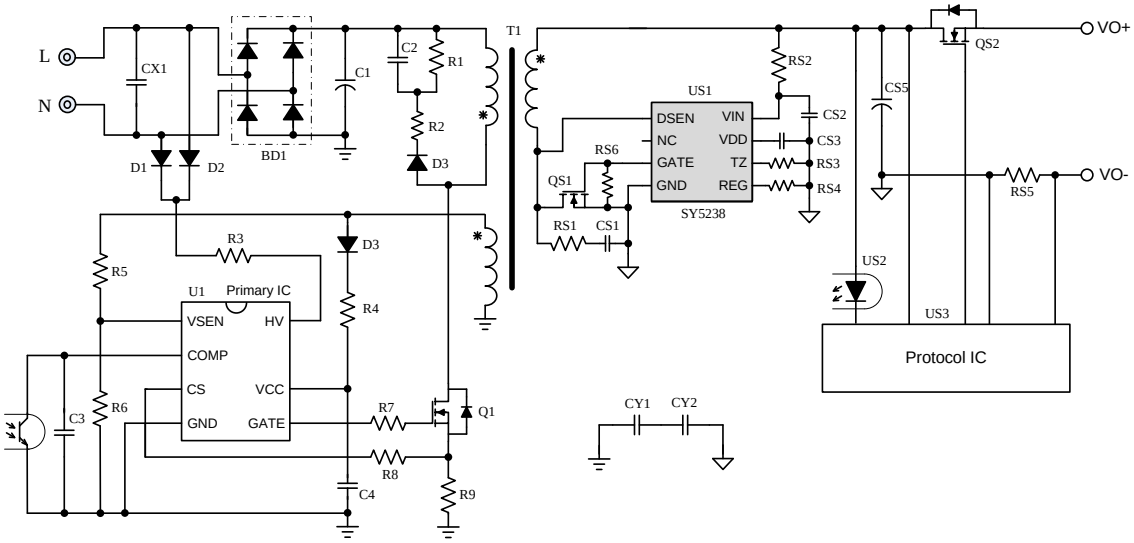


Fig. 1 Typical Application Circuit (SR MOSFET location: Low Side)

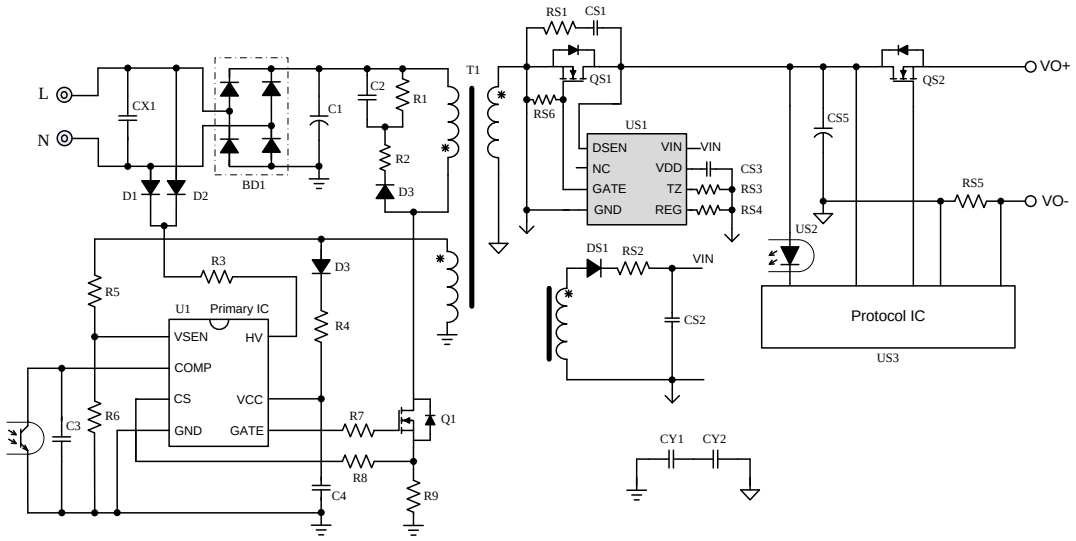


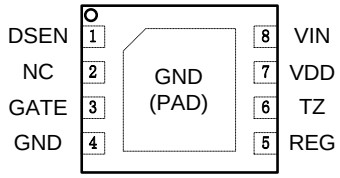
Fig. 2 Typical Application Circuit (SR MOSFET location: High Side)

Ordering Information

SY5238□(□□□)

Package Code

Optional Spec Code



(DFN2*3-8**)**

Pinout (top view)

Ordering Number	Package	Top Mark
SY5238DGD	DFN2*3-8	W7xyz

x=year code, y=week code, z= lot number code

Pinout (top view)

Pin number	Pin Name	Pin Description
1	DSEN	Drain sense input, and used as a self-supply channel
2	NC	Not connected
3	GATE	Gate drive pin
4	GND	Ground pin
5	REG	Connect a resistor between this pin and GND to set the falling slope ref time threshold
6	TZ	Connect a resistor to program ZVS coefficient.
7	VDD	Output of internal LDO, power supply for control unit and GATE drive circuit. Connect a 0.47μF or larger ceramic capacitor between VDD and GND pin
8	VIN	Low voltage power supply input
9	GND	Ground pin

Block Diagram

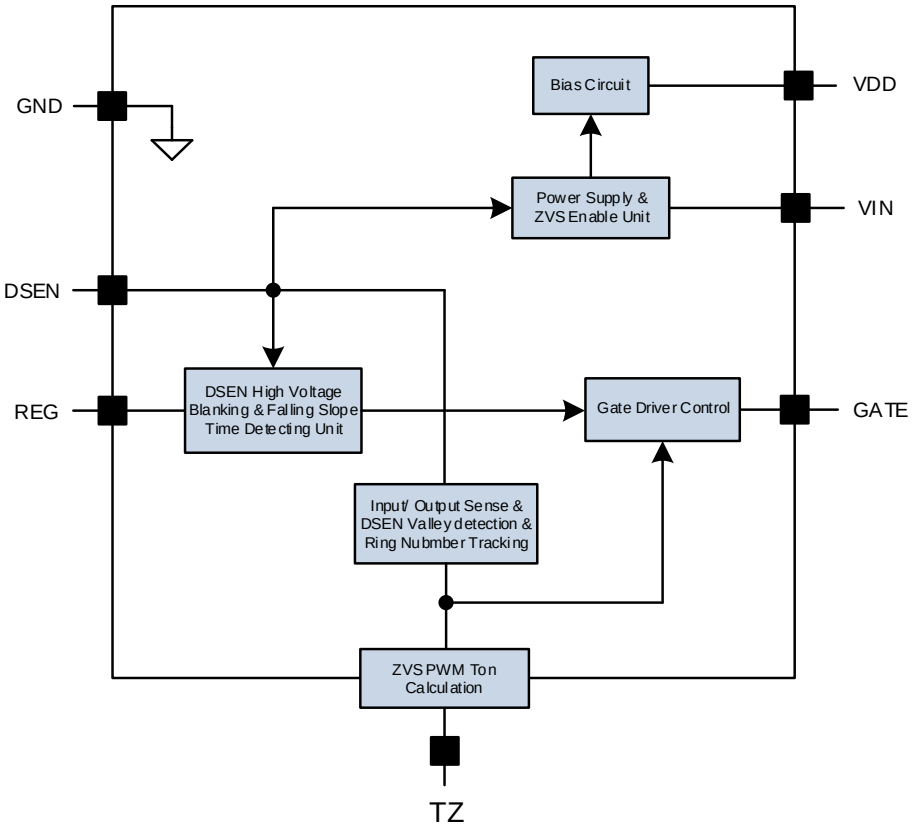


Fig.3 Block Diagram

Absolute Maximum Ratings (Note1)

DSEN ---------- -0.3V ~ 130V
VIN ---------- -0.3V ~ 30V
VDD ---------- -0.3V ~ 15V
GATE ---------- -0.3V ~ VDD+0.3V
TZ, REG ---------- -0.3V ~ 4V
Power Dissipation, @ T_A = 25°C DFN2x3 ---------- 1W
Package Thermal Resistance (Note 2)
DFN2x3, θ_{JA}---------- 46°C/W
DFN2x3, θ_{JC}---------- 28°C/W
Maximum Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Electrical Characteristics

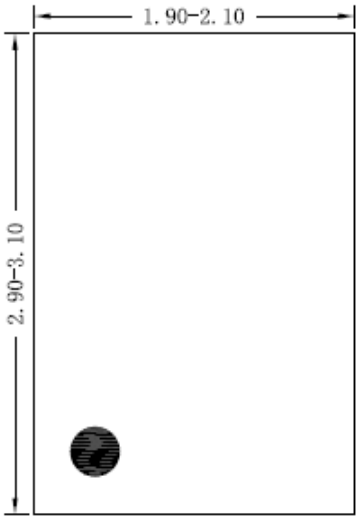
(V_{VIN} = 12V, T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Pin						
VDD ON Threshold	V_{VDD_ON}		3	3.3	3.6	V
UVLO Hysteresis	V_{VDD_HYS}		100	200	300	mV
VDD Regulation Voltage when VIN Pin is Active to Supply IC	$V_{VDD\_REG\_VIN}$		8.3	9.1	9.95	V
VDD Regulation Voltage when DSEN Pin is Active to Supply IC	$V_{VDD\_REG\_DSEN}$		4.2	4.6	5	V
Operating Current (Note3)	I_{VDD_OP}	V_{DD}=9V, C_{GATE}=2.2nF, F_{SW}=200kHz		5.35	6.4	mA
		V_{DD}=5V, C_{GATE}=2.2nF, F_{SW}=200kHz		3.5	4.2	mA
Maximum VDD Pin Capacitor Charging Current	$I_{VDD\_CHARGE\_MAX}$	VIN pin is active to charge VDD capacitor	25	35		mA
		DSEN pin is active to charge VDD capacitor	40	50		mA
Quiescent Current	I_Q	Under Sleep Mode	250	320	400	μA
VIN Pin						
Threshold of Switching to VIN Supply Channel	V_{VIN_VINSPY}	V_{VIN} is rising	4.5	4.8	5.1	V
Threshold of Switching to DSEN Supply Channel	$V_{VIN\_DSENSPY}$	V_{VIN} is falling	4.4	4.7	5	V
REG Pin						
Resistor to Program Drain Falling Slope to Enable SR(Note3)	R_{REG}	R_{REG}=50k	60	80	100	ns
		R_{REG}=300k	115	155	195	ns
TZ Pin						
ZVS Time Program Coefficient	k_{TZ}			4.5		10^{-9}
DSEN Pin						
Operating Voltage Range	V_{DS_OP}				110	V
Ratio of PVS to DSEN	$K_{\_PVS\_RATIO}$			50		
PVS Initial Enable Threshold	$V_{PVS\_INITIAL\_EN}$			150		mV
Turn on Threshold	V_{ON_TH}		-115	-85	-55	mV
V_{DS} Regulation Voltage	V_{DS_REG}		-52	-35	-20	mV
Turn off Threshold	V_{OFF_TH}		-4	10	26	mV
Force Turn off Threshold	$V_{DS\_FORCE\_TH}$		35	48	61	mV
Force Turn off Debounce Time(Note3)	T_{DBC_FORCE}		50	76	100	ns
Enter Sleep Mode Time Threshold	T_{SLP_TH}		50	67	80	μs
GATE Pin						
GATE Pin Clamped Current before VDD ON(Note3)	I_{CLP}	Vgs=1V	160	200		mA

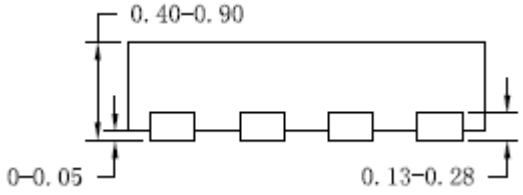
Max. Source Current (Note3)	I_{SOURCE_MAX}	C_{LOAD}=2.2nF, Vgs from 1V to 6V	0.375	0.5		A
Max. Sink Current (Note3)	I_{SINK_MAX}	C_{LOAD}=2.2nF, Vgs from 6V to 1V	1.5	2		A
Minimum ON Time	T_{ON_MIN}		550	700	850	ns
Minimum OFF Time	T_{OFF_MIN}		400	530	660	ns
Turn on Delay Time (Note3)	T_{ON_DLY}	C_{GATE}=2.2nF		35	50	ns
Turn off Delay Time (Note3)	T_{OFF_DLY}	C_{GATE}=2.2nF		10	20	ns
OTP						
Thermal Shutdown Temperature (Note3)	T_{SD}			150		°C
Hysteresis to Resume Operating (Note3)	T_{OTP_HYS}			20		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause perm anent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.
Note 3: Guarantee by design.

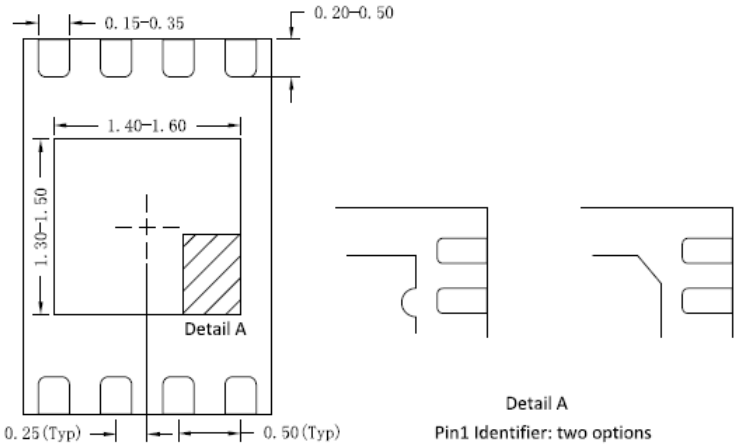
DFN2x3-8 Package Outline



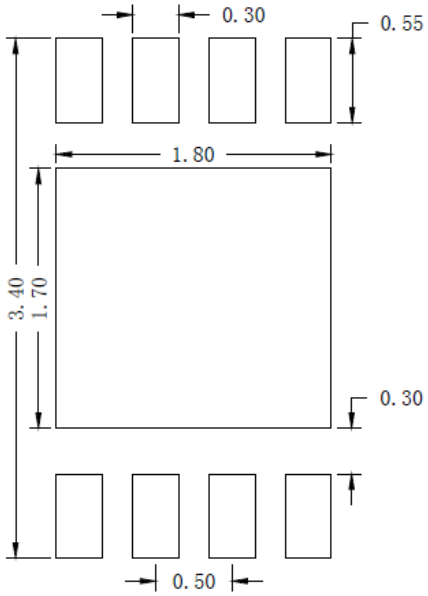
Top View



Side View



Bottom View



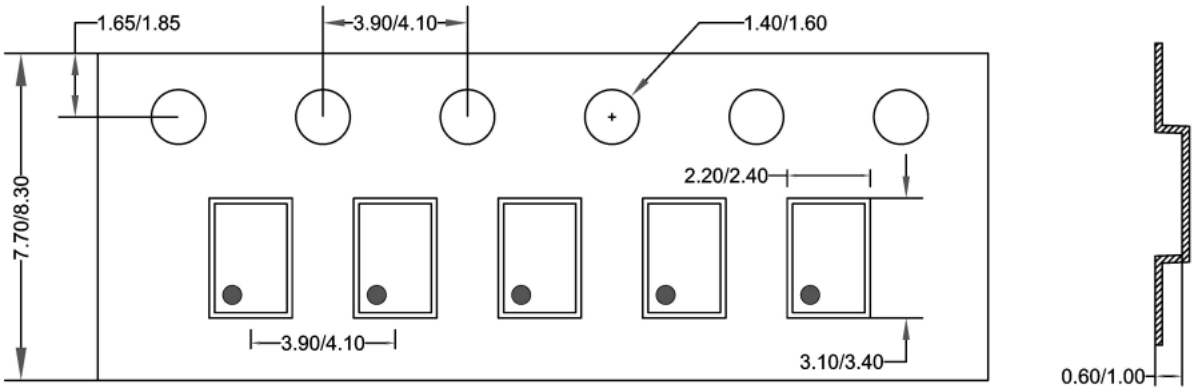
Recommended PCB layout
(Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Taping & Reel Specification

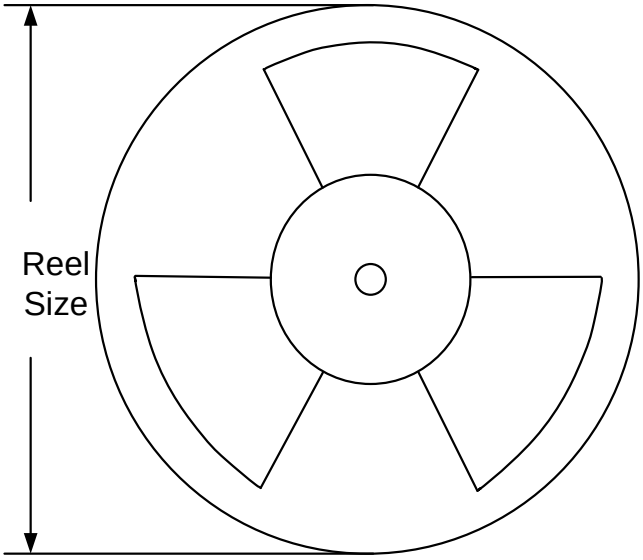
1. Taping Orientation

DFN2x3-8



Feeding Direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
DFN2x3-8	8	4	7"	280	160	3000