DATA SHEET

SKY67021-396LF: 0.4 to 1.2 GHz High-Linearity, Active-Bias Low-Noise Amplifier

Applications

GSM, CDMA, WCDMA, TD-SCDMA cellular infrastructure

Ultra low-noise systems

Balanced, single-ended low-noise amplifier designs

Features

Extended operating temperature range: –40 °C to +100 °C

Low noise figure: 0.6 dB @ 0.9 GHz

Excellent IIP3 performance: +22.5 dBm @ 0.9 GHz

Gain: 17.5 dB @ 0.9 GHz

Adjustable supply current

Integrated enable circuitry

Temperature and process-stable active bias

Miniature DFN (8-pin, 2 x 2 mm) package (MSL1 @ 260 °C per JEDEC J-STD-020)

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04–0074.

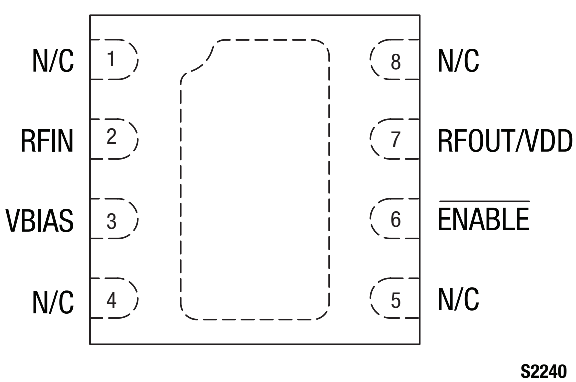

Figure 2. SKY67021-396LF Pinout (Top View)

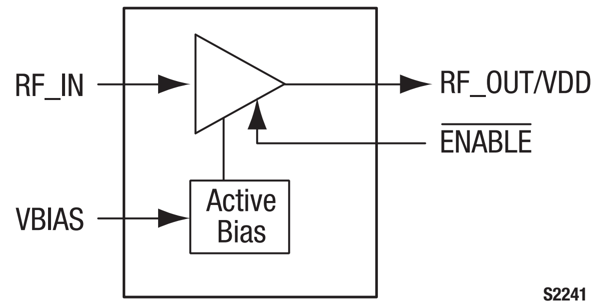

Figure 1. SKY67021-396LF Block Diagram

Description

The SKY67021-396LF is GaAs, pHEMT low-noise amplifier (LNA) with an active bias and high-linearity performance. The advanced GaAs pHEMT enhancement mode process provides good return loss, low noise, and high-linearity performance.

The internal active bias circuitry provides stable performance over temperature and process variation. The device offers the ability to externally adjust supply current and gain. Supply voltage is applied to the RFOUT/VDD pin through an RF choke inductor. Pin 3 (VBIAS) should be connected to RFOUT/VDD through an external resistor to control the supply current. The RFIN and RFOUT/VDD pins should be DC blocked to ensure proper operation.

The SKY67021-396LF operates in the frequency range of 0.4 to 1.2 GHz. For higher frequency operation, the pin-compatible SKY67022-396LF or SKY67023-396LF should be used.

The LNA is manufactured in a compact, 2 x 2 mm, 8-pin Dual Flat No-Lead (DFN) package. A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

Table 1. SKY67021-396LF Signal Descriptions

Pin	Name	Description	Pin	Name	Description
1	N/C	No connection. May be connected to ground with no change in performance.	5	N/C	No connection. May be connected to ground with no change in performance.
2	RFIN	RF input. DC blocking capacitor required.	6	$\overline{\text{ENABLE}}$	Enable pin. Active "low" (0 V) = amplifier on state.
3	VBIAS	Bias for 1st stage amplifier. External resistor sets current consumption.	7	RFOUT/VDD	RF output. Apply VDD through RF choke inductor. DC blocking capacitor required.
4	N/C	No connection. May be connected to ground with no change in performance.	8	N/C	No connection. May be connected to ground with no change in performance.

Table 2. SKY67021-396LF Absolute Maximum Ratings[1]

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply voltage	V_{DD}		5.0	5.5	V
Supply current	I_{DD}			150	mA
RF input power	P_{IN}			+20	dBm
Channel temperature	T_{CH}			+150	°C
Thermal resistance[2]	Θ_{JC}		56.4		°C/W
Storage temperature	T_{STG}	–65	+25	+150	°C
Operating temperature	T_A	–55	+25	+100	°C
Electrostatic discharge:	ESD				
Charged Device Model (CDM), Class 4		1000			V
Human Body Model (HBM), Class 1A		250			V
Machine Model (MM), Class A		30			V

1 Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

2 Thermal resistance = 56.4 °C/W @ 5 V bias.

ESD HANDLING*: Although this device is designed to be as robust as possible, electrostatic discharge (ESD) can damage this device. This device must be protected at all times from ESD when handling or transporting. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD handling precautions should be used at all times.*

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY67021-396LF are provided in Table 2. Electrical specifications are provided in Table 3.

Typical performance characteristics of the SKY67021-396LF are illustrated in Figures 3 through 28.

Table 5 provides noise source pull information versus frequency.

Table 3. SKY67021-396LF Electrical Specifications[1,2]
(V_{DD} = 5 V, I_{DD} = 100 mA, T_A = +25 °C, P_{IN} = –20 dBm, Characteristic Impedance [Z_O] = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
RF Specifications						
Noise figure[3]	NF	@ 0.9 GHz		0.60	0.75	dB
Small signal gain	$\lvert S_{21}\rvert$	@ 0.9 GHz	16.5	17.5	18.5	dB
Input return loss	$\lvert S_{11}\rvert$	@ 0.9 GHz	11.0	12.5		dB
Output return loss	$\lvert S_{22}\rvert$	@ 0.9 GHz	8.0	9.5		dB
Reverse isolation	$\lvert S_{12}\rvert$	@ 0.9 GHz	27	29		dB
Third order input intercept point	IIP3	@ 0.9 GHz, Δf = 1 MHz, P_{IN} = –20 dBm/tone	+20.8	+22.5		dBm
Third order output intercept point	OIP3	@ 0.9 GHz, Δf = 1 MHz, P_{IN} = –20 dBm/tone	+38.3	+40.0		dBm
1 dB input compression point	IP1dB	@ 0.9 GHz	+3.4	+5.2		dBm
1 dB output compression point	OP1dB	@ 0.9 GHz	+20.0	+21.7		dBm
Stability[4]	μ, μ1	Up to 18 GHz, –40 °C to +85 °C		> 1		–
DC Specifications						
Supply voltage	V_{DD}			5.0		V
Quiescent supply current	I_{DD}	Set with external resistor	85	100	115	mA
Amplifier enable off current (logic "high")	I_{EN}		700	900	1100	μA
Enable voltage:	V_{ENABLE}					
Gain mode				0	0.2	V
Power-down mode				1.5	5.5	V
Enable rise time	T_R	@ 0.9 GHz		250	500	ns
Enable fall time	T_F	@ 0.9 GHz		250	500	ns

1 Performance is guaranteed only under the conditions listed in this Table.
2 Circuit topology optimized for balanced configuration with best IIP3 and NF performance.
3 Loss from the input SMA connector and Evaluation Board up to component M1 has not been de-embedded from the NF measurement.
4 Applies to typical application circuit and components shown in Figure 31.

Table 4. SKY67021-396LF Electrical Specifications[1,2]

(VDD = 5 V, IDD = 100 mA, TA = +25 °C, f = 415 MHz, PIN = –20 dBm, Characteristic Impedance [ZO] = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Noise figure[3]	NF	Pin = -20 dBm, CW		0.65		dB
Small signal gain	|S21|	Pin = -20 dBm, CW		23		dB
Input return loss	|S11|	Pin = -20 dBm, CW		15		dB
Output return loss	|S22|	Pin = -20 dBm, CW		9		dB
Reverse isolation	|S12|	Pin = -20 dBm, CW		32		dB
Third order input intercept point	IIP3	Pin = -20 dBm, 1 MHz Tone		10		dBm
Third order output intercept point	OIP3	Pin = -20 dBm, 1 MHz Tone		33		dBm
1 dB input compression point	IP1dB	CW		-1		dBm
1 dB output compression point	OP1dB	CW		21		dBm

1 Not tested in production. Verified by design.

2 Circuit topology optimized for balanced configuration with best IIP3 and NF performance.

3 Loss from the input SMA connector and Evaluation Board up to component M1 has not been de-embedded from the NF measurement.

Typical Performance Characteristics

(VDD = 5 V, Idd = 100 mA, TA = +25 °C, PIN = –20 dBm, Characteristic Impedance [Zo] = 50 Ω, Unless Otherwise Noted)

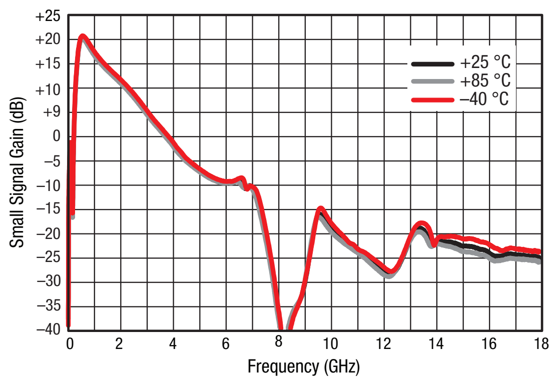

Figure 3. Broadband Gain Response vs Frequency Over Temperature

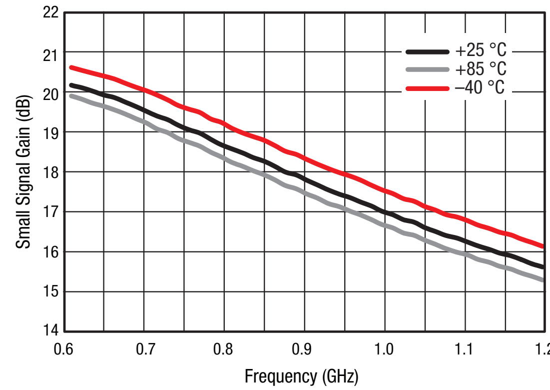

Figure 4. Narrowband Gain Response vs Frequency Over Temperature

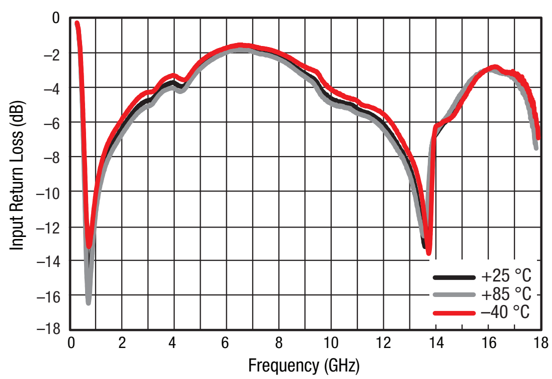

Figure 5. Broadband Input Return Loss vs Frequency Over Temperature

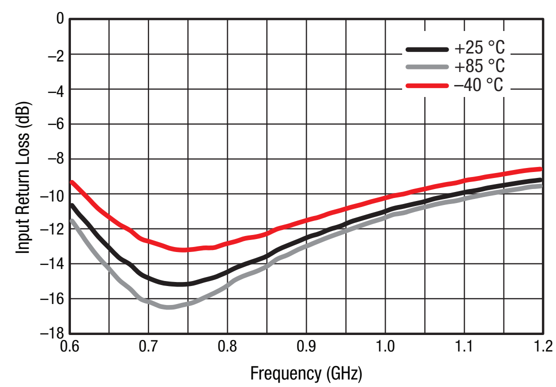

Figure 6. Narrowband Input Return Loss vs Frequency Over Temperature

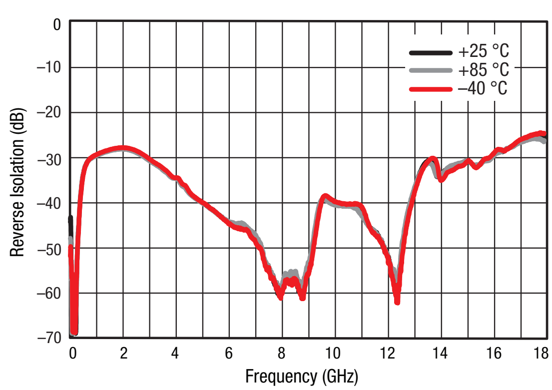

Figure 7. Broadband Reverse Isolation vs Frequency Over Temperature

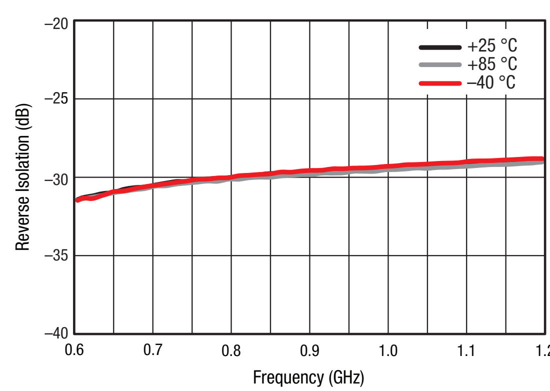

Figure 8. Narrowband Reverse Isolation vs Frequency Over Temperature

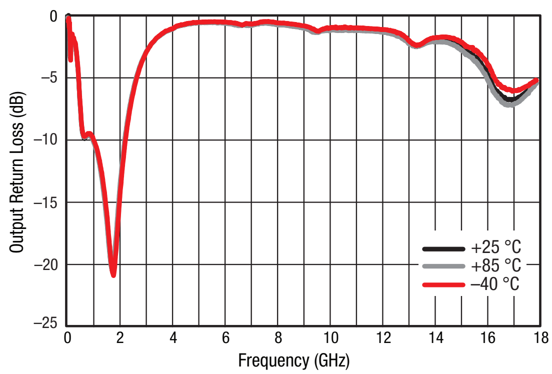

Figure 9. Broadband Output Return Loss vs Frequency Over Temperature

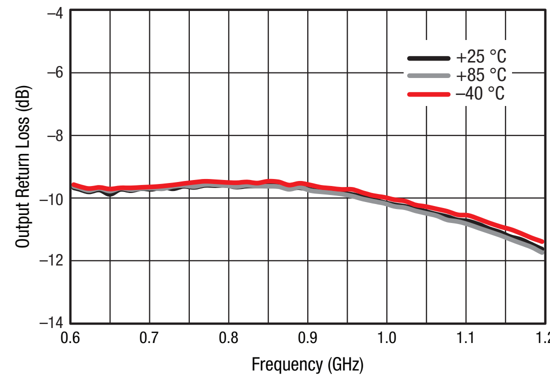

Figure 10. Narrowband Output Return Loss vs Frequency Over Temperature

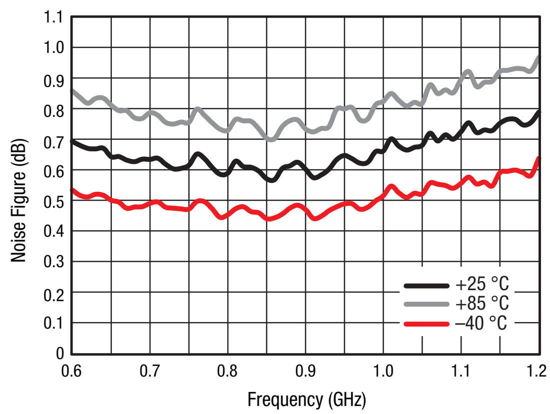

Figure 11. Noise Figure vs Frequency Over Temperature

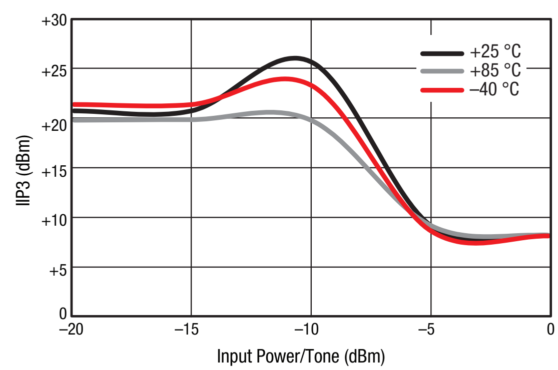

Figure 12. IIP3 vs Input Power Over Temperature @ 600 MHz (P_{IN} = –20 dBm, Tone Spacing = 1 MHz)

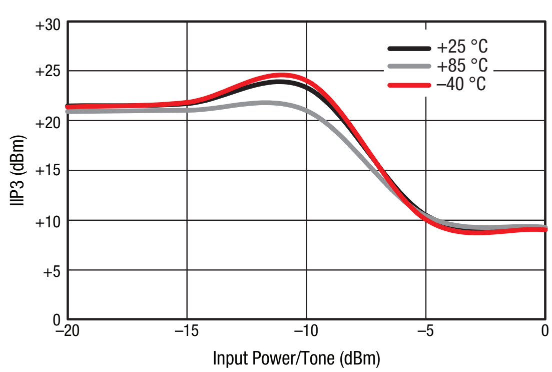

Figure 13. IIP3 vs Input Power Over Temperature @ 700 MHz (P_{IN} = –20 dBm, Tone Spacing = 1 MHz)

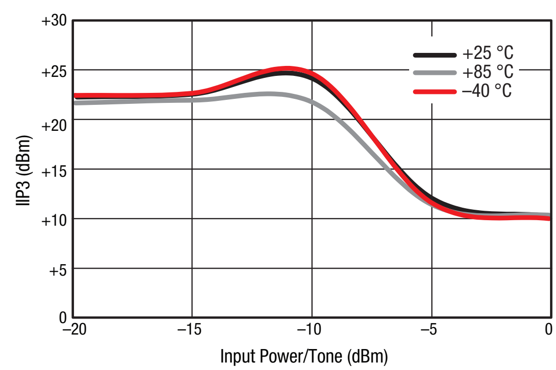

Figure 14. IIP3 vs Input Power Over Temperature @ 800 MHz (P_{IN} = –20 dBm, Tone Spacing = 1 MHz)

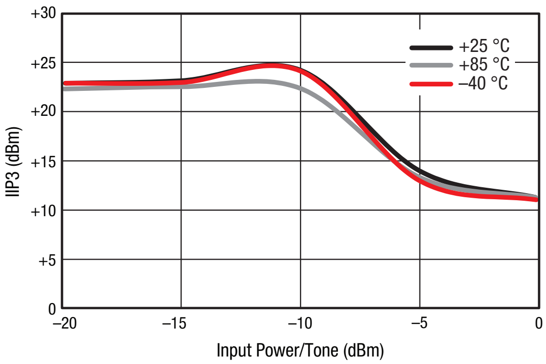

Figure 15. IIP3 vs Input Power Over Temperature @ 900 MHz (PIN = –20 dBm, Tone Spacing = 1 MHz)

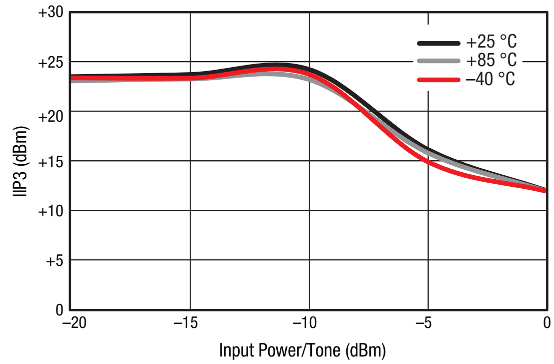

Figure 16. IIP3 vs Input Power Over Temperature @ 1000 MHz (PIN = –20 dBm, Tone Spacing = 1 MHz)

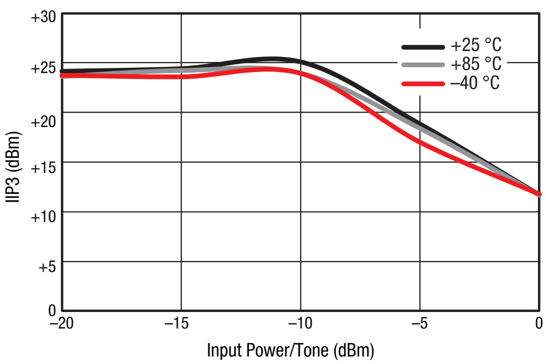

Figure 17. IIP3 vs Input Power Over Temperature @ 1200 MHz (PIN = –20 dBm, Tone Spacing = 1 MHz)

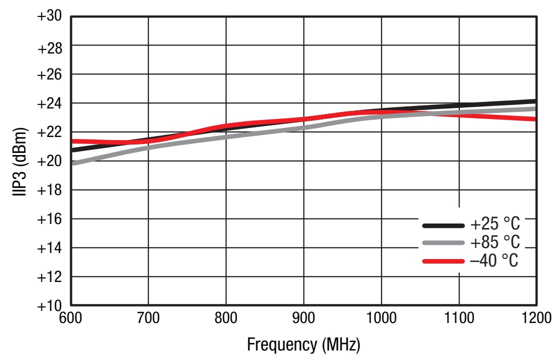

Figure 18. IIP3 vs Frequency Over Temperature (PIN = –20 dBm, Tone Spacing = 1 MHz)

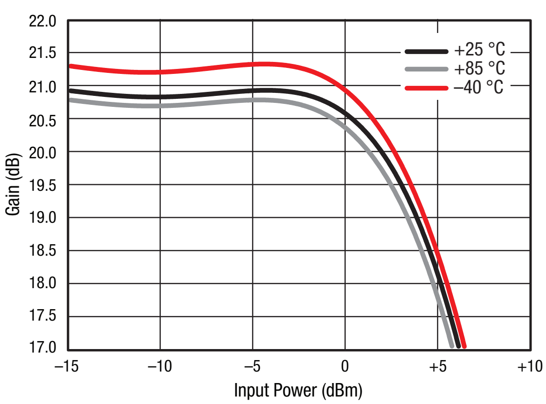

Figure 19. Gain vs Input Power Over Temperature @ 600 MHz

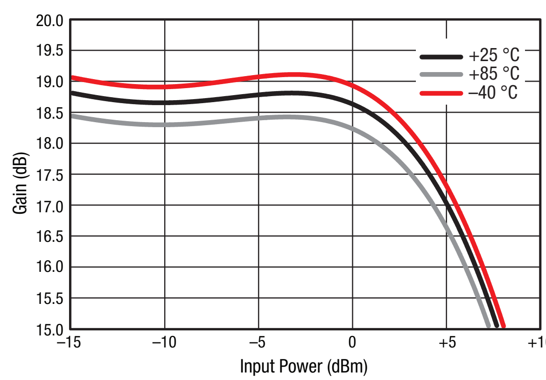

Figure 20. Gain vs Input Power Over Temperature @ 700 MHz

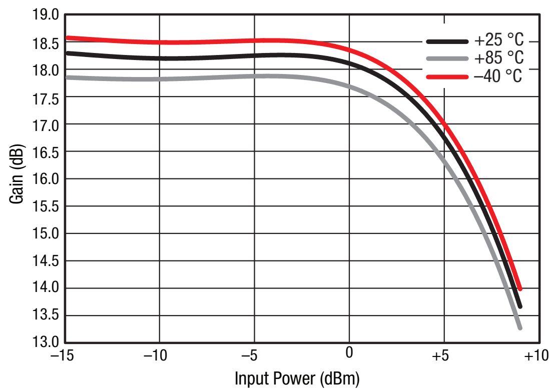

Figure 21. Gain vs Input Power Over Temperature @ 800 MHz

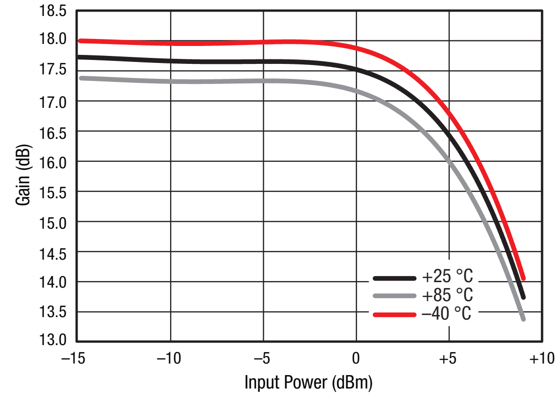

Figure 22. Gain vs Input Power Over Temperature @ 900 MHz

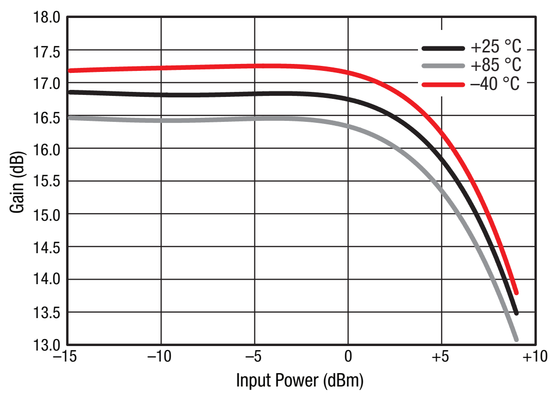

Figure 23. Gain vs Input Power Over Temperature @ 1000 MHz

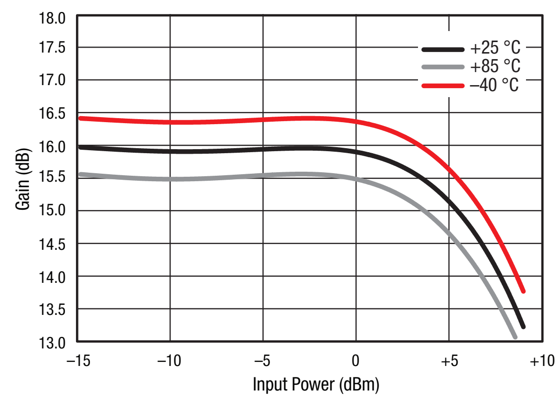

Figure 24. Gain vs Input Power Over Temperature @ 1200 MHz

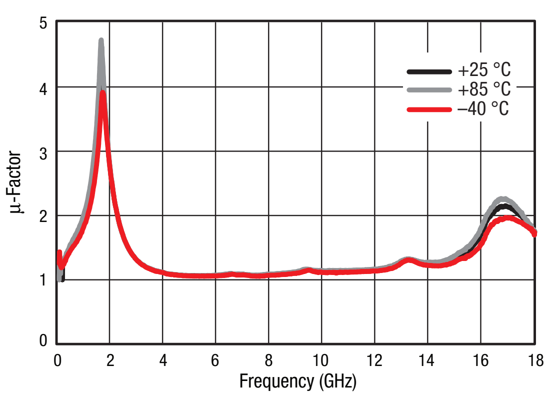

Figure 25. Stability Factor (µ) vs Frequency Over Temperature

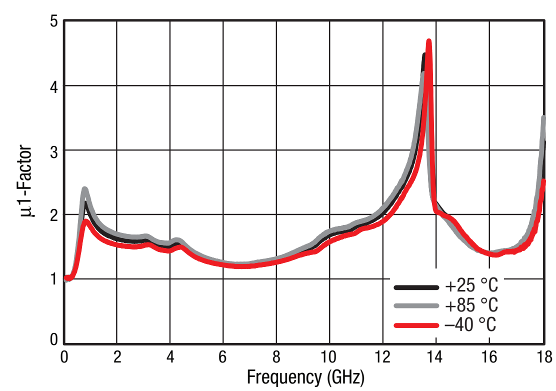

Figure 26. Stability Factor (µ1) vs Frequency Over Temperature

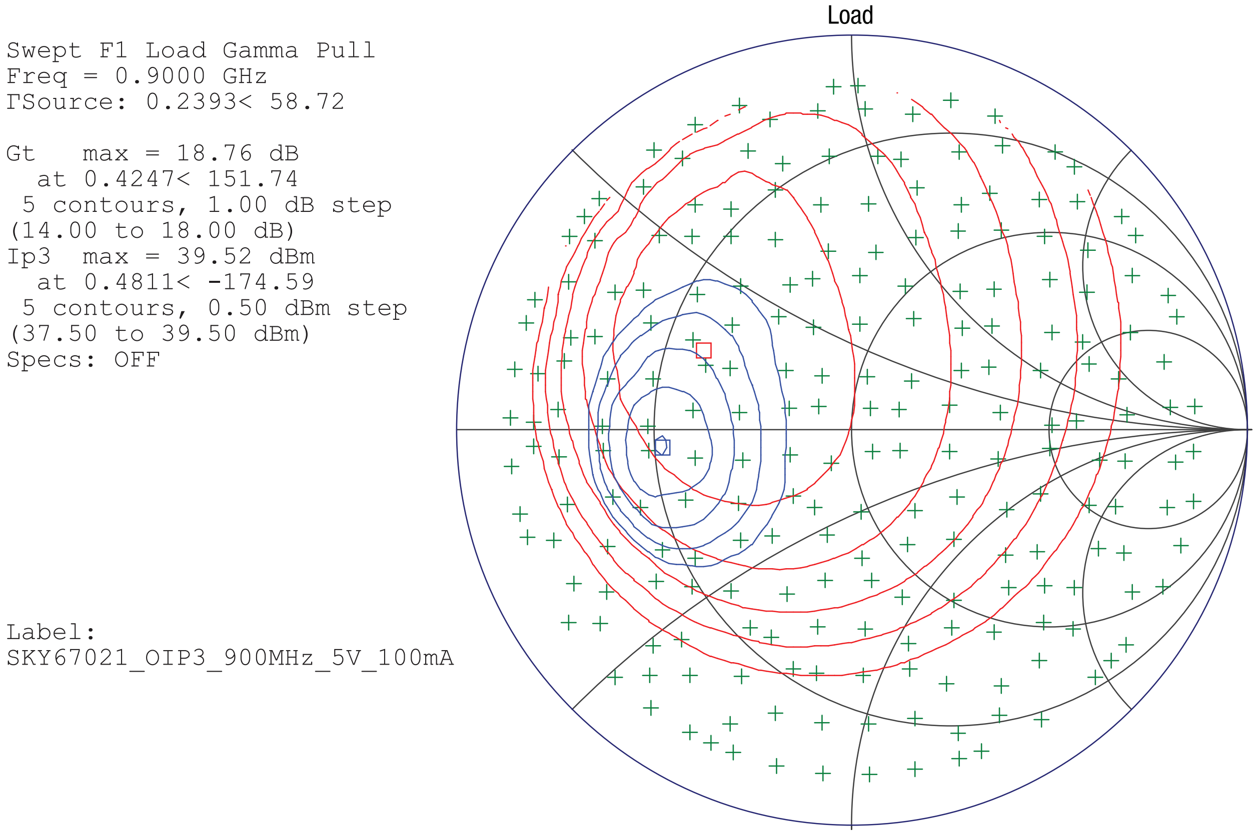

Figure 27. Load Pull, @ 5 V, 900 MHz, 100 mA

Table 5. Noise Parameters vs Frequency @ 5.0 V and 100 mA

Frequency (GHz)	Minimum Noise Figure (F_{MIN}) (dB)	Noise Resistance (R_N) (Ω)	Γopt		Associated Gain (dB)	Maximum Gain (G_{MAX}) (dB)
			Magnitude	Phase		
0.80	0.5571	0.0600	0.1286	129.21	18.8608	19.7254
0.84	0.3977	0.1264	0.1201	72.63	18.8469	19.3559
0.89	0.543	0.0414	0.1575	111.37	18.1270	18.9171
1.20	0.7077	0.0667	0.1636	107.57	15.8561	16.6599
1.42	0.8033	0.0777	0.1466	110.34	14.5550	15.4004
1.52	0.8732	0.0767	0.1751	130.29	13.8350	14.8953
1.76	1.0127	0.1047	0.1240	122.01	12.8532	13.8256
1.84	1.1337	0.1062	0.1113	147.04	12.3242	13.5113
1.92	1.1686	0.1132	0.1137	134.44	12.1251	13.2098
1.98	1.232	0.1021	0.1260	163.51	11.6427	12.9939
2.00	1.3361	0.2648	0.1212	74.78	12.1585	12.9206
2.38	1.5989	0.1143	0.1302	158.37	10.4524	11.7369
2.52	1.6619	0.1667	0.1109	156.50	10.1114	11.3724
2.60	1.7366	0.1817	0.0974	156.70	9.9104	11.1835
2.70	1.6845	0.1032	0.1529	–165.66	9.2704	10.9525
3.00	2.1342	0.1874	0.0978	171.43	8.9475	10.3251
3.60	2.6314	0.2626	0.0816	172.61	6.9070	8.3274
4.00	2.9366	0.3237	0.1187	–160.48	7.3181	8.8760
5.00	3.7549	0.4659	0.2157	–156.72	6.3847	8.3182
6.00	4.5836	0.4105	0.3645	–149.11	5.9685	8.3084
7.00	5.4265	0.7168	0.3627	–157.54	5.3432	8.5428

Evaluation Board Description

The SKY67021-396LF Evaluation Board is used to test the performance of the SKY67021-396LF LNA. An assembly drawing for the Evaluation Board is shown in Figure 28. The layer detail is provided in Figure 29. An Evaluation Board schematic diagram is provided in Figure 30. Tables 6 and 7 provide the Bill of Materials (BOM) for Evaluation Board components.

Package Dimensions

The PCB layout footprint for the SKY67021-396LF is provided in Figure 31. Typical part markings are shown in Figure 32. Package dimensions are shown in Figure 33, and tape and reel dimensions are provided in Figure 34.

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY67021-396LF is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

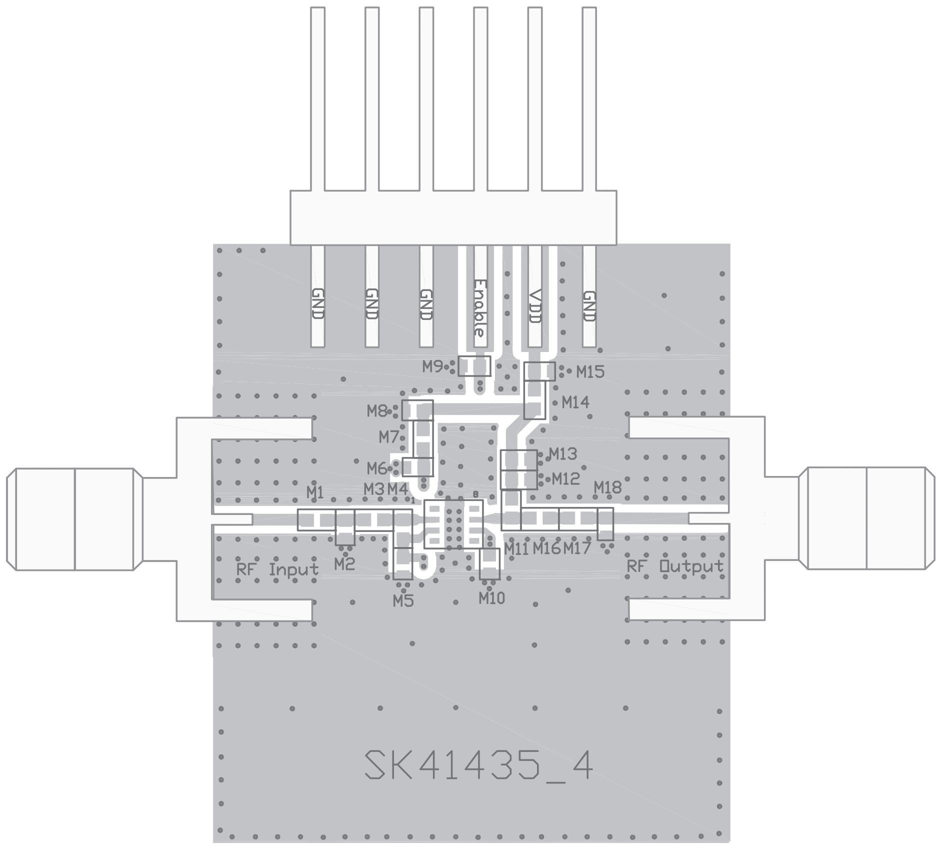

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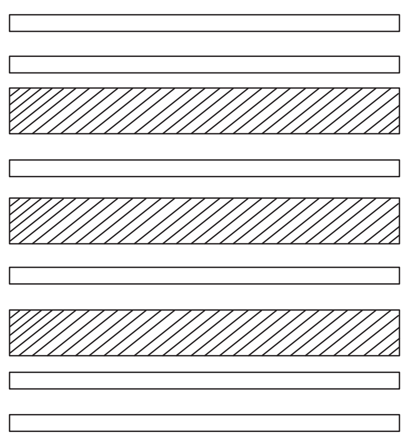
Figure 28. SKY67021-396LF Evaluation Board Assembly Diagram

Cross Section



Name	Thickness (mm)	Material
MSK-NS		
TRA-NS	0.03556	Cu foil
Laminate	0.254 ± 0.152	Rogers 4350B
TRA-2	0.0178	Cu foil
Laminate	0.889 nom.	FR4 Prepreg (Note 1)
TRA-3	0.0178	Cu foil
Laminate	0.254 ± 0.152	FR4 Core
TRA-FS	0.0178	Cu foil
MSK-PS		

Note 1: Adjust this thickness to meet total thickness goal.

General Notes:
Material: Rogers R04350, $\varepsilon_r = 3.66$
Layer 1 thickness: 0.254 mm
Overall board thickness: 1.575 mm
50 Ω transmission line width: 0.522 mm
Coplanar ground spacing: 0.394 mm
Via diameter: 0.254 mm

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Figure 29. Layer Detail Physical Characteristics

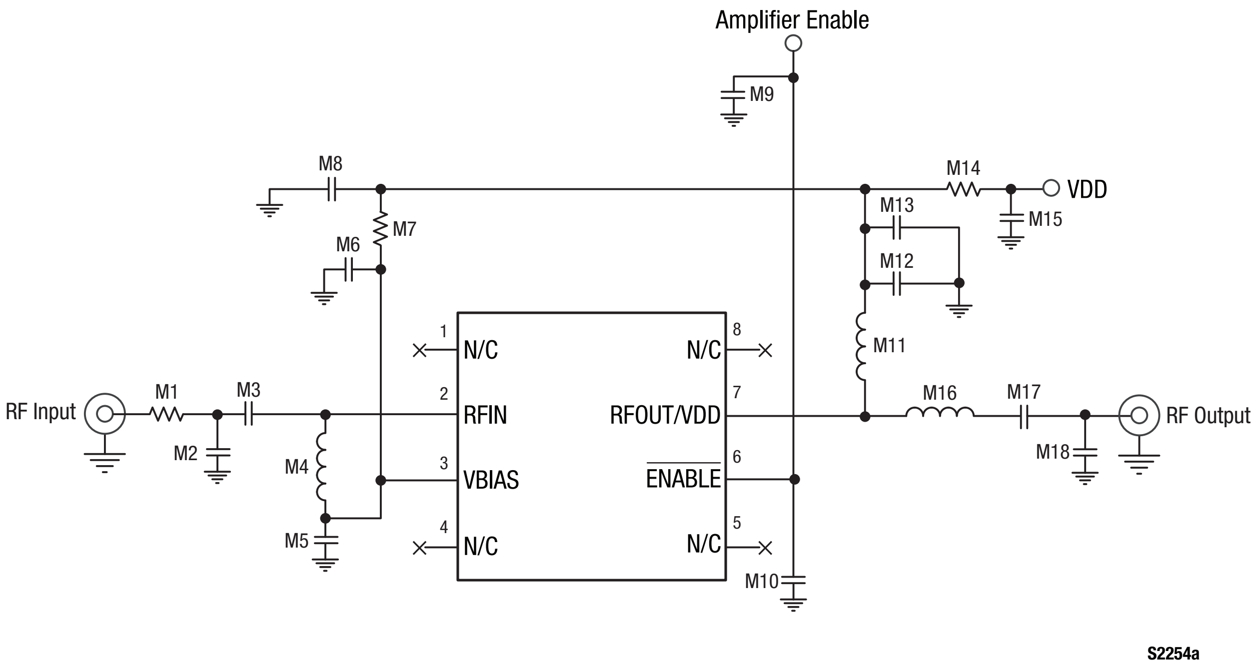


Figure 30. SKY67021-396LF Evaluation Board Schematic

Table 6. SKY67021-396LF Evaluation Board Bill of Materials (600 MHz to 1200 MHz)

Component	Type	Size	Value (5 V @ 100 mA)	Manufacturer	Mfr Part Number
M1	Resistor	0402	0 Ω	Panasonic	ERJ-2GEOROOX
M2	DNI	0402	–	–	–
M3	Capacitor	0402	6 pF	Murata	GJM1555C1H6R0CB01
M4	Inductor	0402	12 nH	Coilcraft	0402HP-12NX_GLU
M5	Capacitor	0402	68 pF	Murata	GRM1555C1H680JZ01
M6	DNI	0402	–	–	–
M7	Resistor	0402	3.6 kΩ	Panasonic	ERJ-2GEJ362X
M8	Capacitor	0402	0.1 μF	Murata	GRM155R71A104KA01
M9	Capacitor	0402	1000 pF	Murata	GRM1555C1H102JA01
M10	DNI	0402	–	–	–
M11	Inductor	0402	27 nH	Murata	LQG15HN27NJ02D
M12	Capacitor	0402	10 pF	Murata	GRM1555C1H100JZ01D
M13	Capacitor	0402	1000 pF	Murata	GRM1555C1H102JA01
M14	Resistor	0402	0 Ω	Panasonic	ERJ-2GEOROOX
M15	DNI	0402	–	–	–
M16	Inductor	0402	4.3 nH	Murata	LQG15HN4N3S02D
M17	Capacitor	0402	82 pF	Murata	GRM1555C1H820JA01
M18	DNI	0402	–	–	–

Table 7. SKY67021-396LF Evaluation Board Bill of Materials (415 MHz)

Component	Type	Size	Value	Manufacturer	Mfr Part Number
M1	Resistor	402	0 Ω	Panasonic	ERJ-2GE0R00X
M2	DNI	402	–	–	–
M3	Capacitor	402	6 pF	Murata	GJM1555C1H6R0CB01
M4	Inductor	402	24 nH	Coilcraft	0402HP-24NX_GLU
M5	Capacitor	402	68 pF	Murata	GRM1555C1H680JZ01
M6	DNI	402	–	–	–
M7	Resistor	402	3.6 kΩ	Panasonic	ERJ-2GEJ362X
M8	Capacitor	402	0.1 uF	Murata	GRM155R71A104KA01
M9	Capacitor	402	1000 pF	Murata	GRM1555C1H102JA01
M10	DNI	402	–	–	–
M11	Inductor	402	39 nH	Murata	LQG15HS39NJ02D
M12	Capacitor	402	10 pF	Murata	GRM1555C1H100JZ01D
M13	Capacitor	402	1000 pF	Murata	GRM1555C1H102JA01
M14	Resistor	402	0 Ω	Panasonic	ERJ-2GE0R00X
M15	DNI	402	–	–	–
M16	Inductor	402	4.3 nH	Murata	LQG15HN4N3S02D
M17	Capacitor	402	82 pF	Murata	GRM1555C1H820JA01
M18	DNI	402	–	–	–

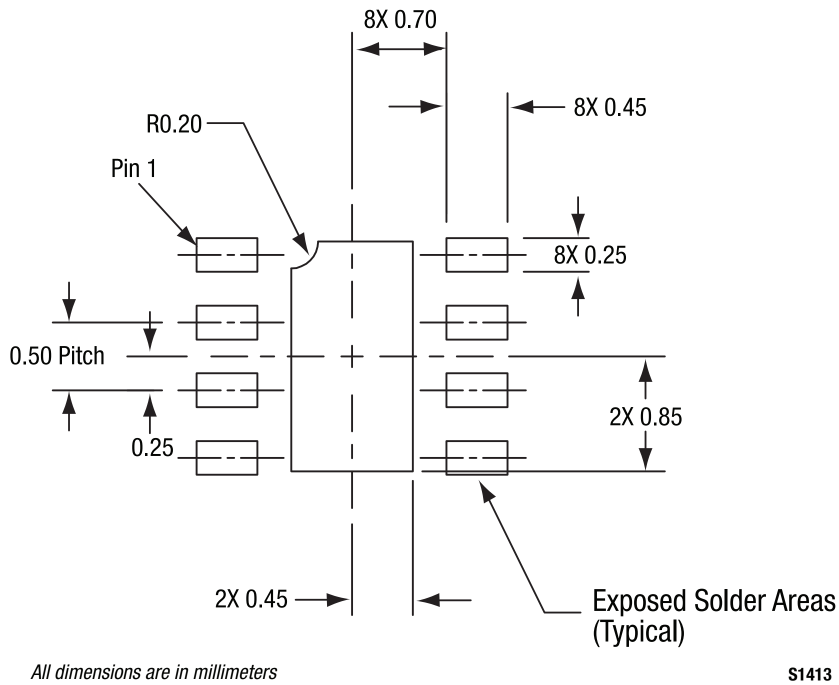


Figure 31. SKY67021-396LF PCB Layout Footprint (Top View)

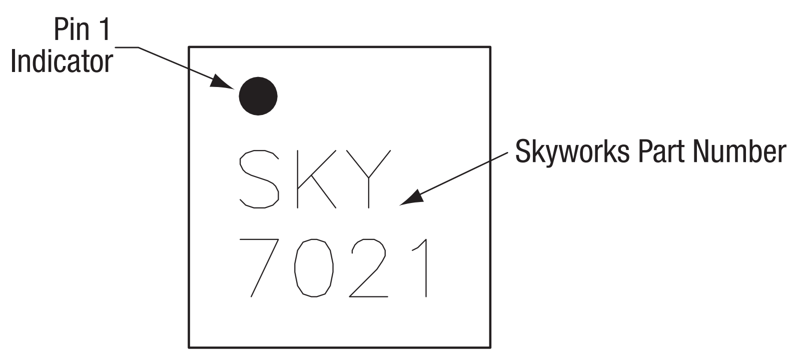
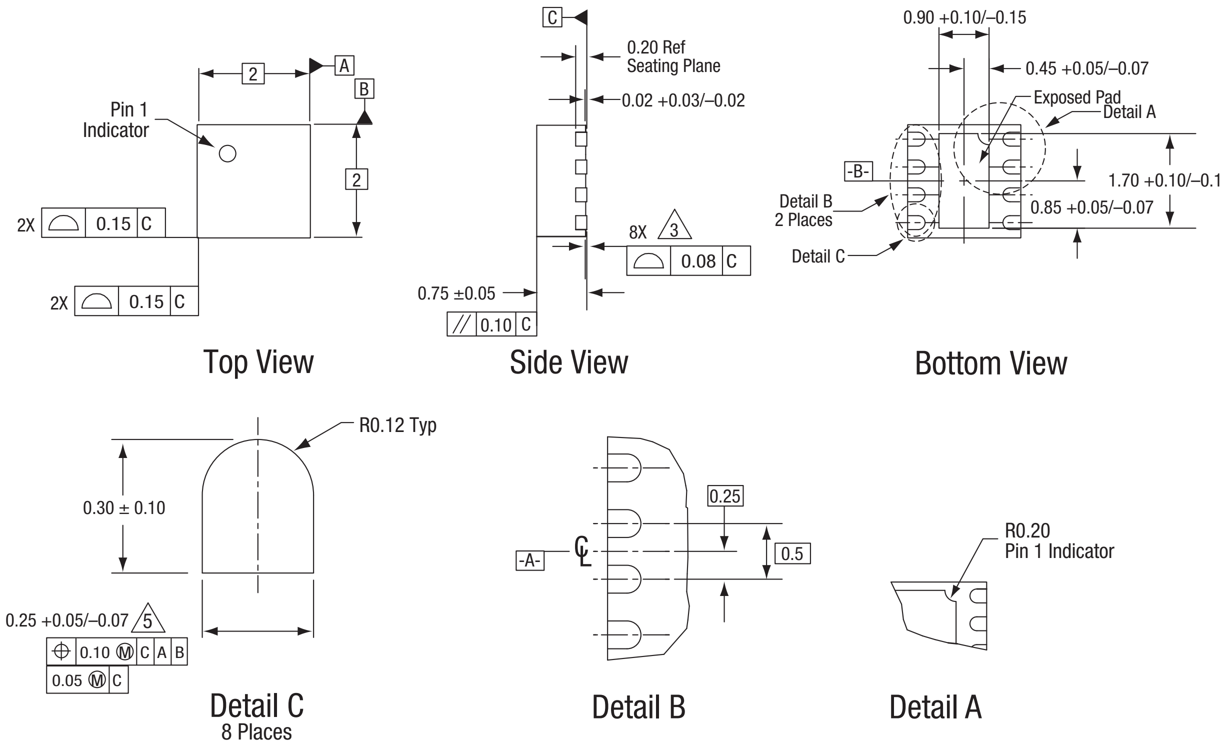


Figure 32. Typical Part Markings (Top View)



Notes:

1. *All measurements are in millimeters.*
2. *Dimensions and tolerances according to ASME Y14.5M-1994.*
3. *Coplanarity applies to the exposed heat sink ground pad as well as the terminals.*
4. *Plating requirement per source control drawing (SCD) 2504.*
5. *Dimension applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.*

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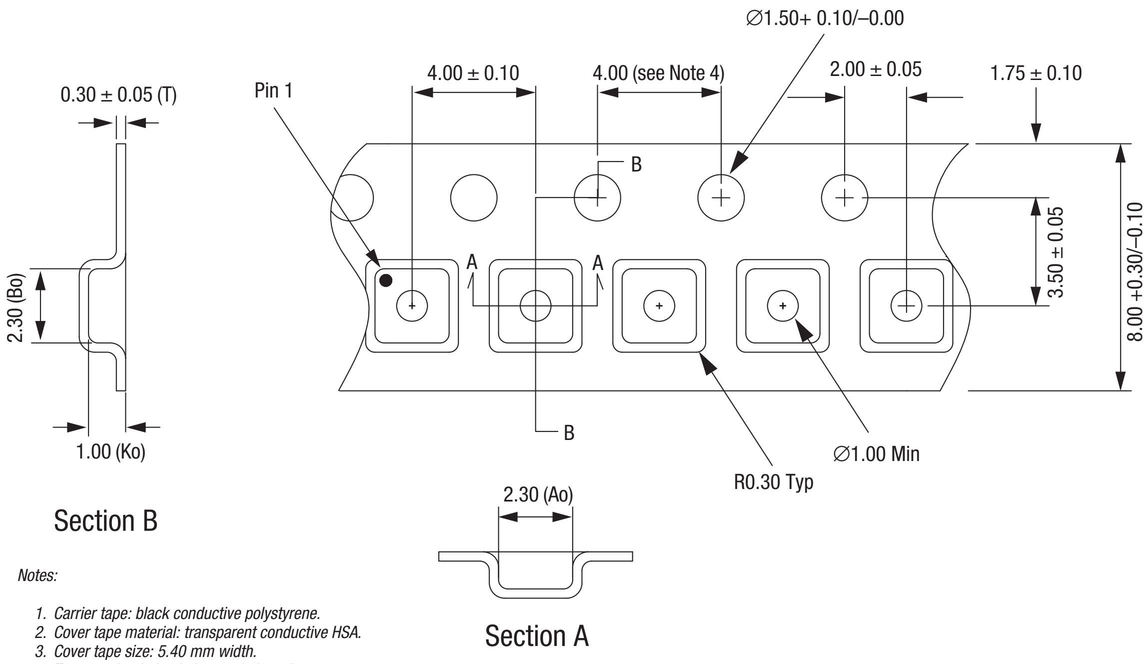
Figure 33. SKY67021-396LF Package Dimensions



Notes:

1. *Carrier tape: black conductive polystyrene.*
2. *Cover tape material: transparent conductive HSA.*
3. *Cover tape size: 5.40 mm width.*
4. *Ten sprocket hole pitch cumulative tolerance = ±0.20 mm.*
5. *ESD surface resistivity is ≤1 x 10^8 Ohms/square per EIA, JEDEC tape and reel specification.*
6. *Ao and Bo measurement point to be 0.30 mm from bottom pocket.*
7. *All measurements are in millimeters.*

Figure 34. SKY67021-396LF Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Number
SKY67021-396LF LNA	SKY67021-396LF	SKY67021-396LF-EVB