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# Silicon Carbide (SiC) Module – 8 mohm SiC M3S MOSFET, 1200 V, 2-PACK Half Bridge Topology, F1 Package

## Product Preview

## NXH008P120M3F1PTG, NXH008P120M3F1PG

The NXH008P120M3F1 is a power module containing 8 mΩ / 1200 V SiC MOSFET half-bridge and a thermistor in an F1 package.

### Features

- 8 mΩ / 1200 V M3S SiC MOSFET Half-Bridge
- Thermistor
- Options with Pre-Applied Thermal Interface Material (TIM) and without Pre-Applied TIM
- Press-Fit Pins
- These Devices are Pb-Free, Halide Free and are RoHS Compliant

### Typical Applications

- Solar Inverter
- Uninterruptible Power Supplies
- Electric Vehicle Charging Stations
- Industrial Power

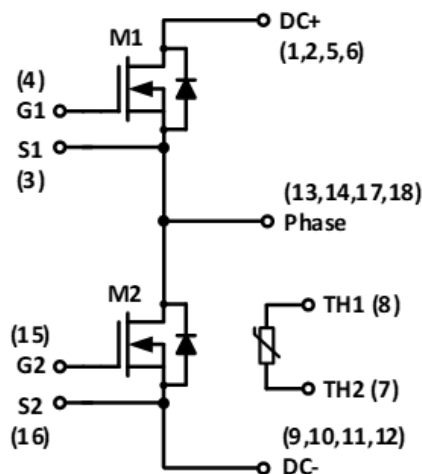
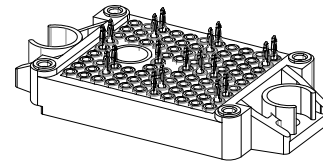


Figure 1. NXH008P120M3F1 Schematic Diagram

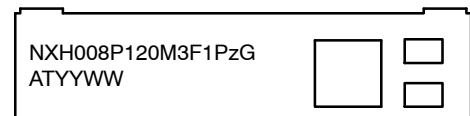
This document contains information on a product under development. onsemi reserves the right to change or discontinue this product without notice.

### PACKAGE PICTURE



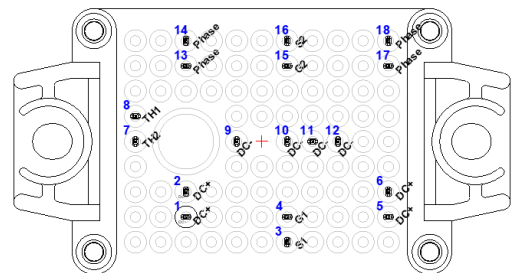
PIM18 33.8x42.5 (PRESS FIT)  
CASE 180BW

### MARKING DIAGRAM



NXH008P120M3F1PzG = Specific Device Code  
z = T (with TIM), blank (without TIM)  
AT = Assembly & Test Site Code  
YYWW = Year and Work Week Code

### PIN CONNECTIONS



See Pin Function Description for pin names

### ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

## NXH008P120M3F1PTG, NXH008P120M3F1PG

### PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	DC+	DC Positive Bus connection
2	DC+	DC Positive Bus connection
3	S1	M1 Kelvin Source (High side switch)
4	G1	M1 Gate (High side switch)
5	DC+	DC Positive Bus connection
6	DC+	DC Positive Bus connection
7	TH2	Thermistor Connection 2
8	TH1	Thermistor Connection 1
9	DC-	DC Negative Bus connection
10	DC-	DC Negative Bus connection
11	DC-	DC Negative Bus connection
12	DC-	DC Negative Bus connection
13	PHASE	Center point of half bridge
14	PHASE	Center point of half bridge
15	G2	M2 Gate (Low side switch)
16	S2	M2 Kelvin Source (Low side switch)
17	PHASE	Center point of half bridge
18	PHASE	Center point of half bridge

# NXH008P120M3F1PTG, NXH008P120M3F1PG

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
<b>SiC MOSFET</b>			
Drain–Source Voltage	$V_{DS}$	1200	V
Gate–Source Voltage	$V_{GS}$	+22/–10	V
Continuous Drain Current @ $T_c = 80^\circ\text{C}$ ( $T_J = 175^\circ\text{C}$ )	$I_D$	145	A
Pulsed Drain Current ( $T_J = 150^\circ\text{C}$ )	$I_{Dpulse}$	436	A
Maximum Power Dissipation ( $T_J = 175^\circ\text{C}$ )	$P_{tot}$	382	W
Minimum Operating Junction Temperature	$T_{JMIN}$	–40	$^\circ\text{C}$
Maximum Operating Junction Temperature	$T_{JMAX}$	175	$^\circ\text{C}$

## THERMAL PROPERTIES

Storage Temperature Range	$T_{stg}$	–40 to 150	$^\circ\text{C}$
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## INSULATION PROPERTIES

Isolation Test Voltage, $t = 1\text{ s}$ , 60 Hz	$V_{is}$	4800	$V_{RMS}$
Creepage Distance		12.7	mm
CTI		600	
Substrate Ceramic Material		$\text{Al}_2\text{O}_3$	
Substrate Ceramic Material Thickness		0.32	mm

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.

## RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Module Operating Junction Temperature	$T_J$	–40	150	$^\circ\text{C}$

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
<b>SiC MOSFET CHARACTERISTICS</b>						
Zero Gate Voltage Drain Current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 1200\text{ V}$ , $T_J = 25^\circ\text{C}$	$I_{DSS}$	–	–	400	$\mu\text{A}$
Drain–Source On Resistance	$V_{GS} = 18\text{ V}$ , $I_D = 120\text{ A}$ , $T_J = 25^\circ\text{C}$	$R_{DS(ON)}$	–	7.7	10.9	$\text{m}\Omega$
	$V_{GS} = 18\text{ V}$ , $I_D = 120\text{ A}$ , $T_J = 125^\circ\text{C}$		–	12.6	–	
	$V_{GS} = 18\text{ V}$ , $I_D = 120\text{ A}$ , $T_J = 150^\circ\text{C}$		–	14.4	–	
	$V_{GS} = 18\text{ V}$ , $I_D = 120\text{ A}$ , $T_J = 175^\circ\text{C}$		–	18.1	–	
Gate–Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 60\text{ mA}$	$V_{GS(TH)}$	2.04	2.4	4.4	V
Internal Gate Resistance		$R_{GINT}$	–	0.8	–	$\Omega$
Gate Leakage Current	$V_{GS} = -10\text{ V} / 22\text{ V}$ , $V_{DS} = 0\text{ V}$	$I_{GSS}$	–4	–	4	$\mu\text{A}$
Input Capacitance	$V_{DS} = 800\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$	$C_{ISS}$	–	8334	–	$\text{pF}$
Reverse Transfer Capacitance		$C_{RSS}$	–	37	–	
Output Capacitance		$C_{OSS}$	–	472	–	
Total Gate Charge	$V_{DS} = 800\text{ V}$ , $V_{GS} = -3/18\text{ V}$ , $I_D = 120\text{ A}$	$Q_{G(TOTAL)}$	–	419	–	$\text{nC}$
Gate–Source Charge		$Q_{GS}$	–	61	–	$\text{nC}$
Gate–Drain Charge		$Q_{GD}$	–	96	–	$\text{nC}$

# NXH008P120M3F1PTG, NXH008P120M3F1PG

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted) (continued)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
<b>SiC MOSFET CHARACTERISTICS</b>						
Turn-on Delay Time	T <sub>J</sub> = 25°C V <sub>DS</sub> = 800 V, I <sub>D</sub> = 120 A V <sub>GS</sub> = -3 V / 18 V, R <sub>G</sub> = 2 Ω	t <sub>d(on)</sub>	—	17	—	ns
Rise Time		t <sub>r</sub>	—	17	—	
Turn-off Delay Time		t <sub>d(off)</sub>	—	97	—	
Fall Time		t <sub>f</sub>	—	12	—	
Turn-on Switching Loss per Pulse		E <sub>ON</sub>	—	1760	—	μJ
Turn-off Switching Loss per Pulse		E <sub>OFF</sub>	—	588	—	
Turn-on Delay Time	T <sub>J</sub> = 150°C V <sub>DS</sub> = 800 V, I <sub>D</sub> = 120 A V <sub>GS</sub> = -3 V / 18 V, R <sub>G</sub> = 2 Ω	t <sub>d(on)</sub>	—	15	—	ns
Rise Time		t <sub>r</sub>	—	15	—	
Turn-off Delay Time		t <sub>d(off)</sub>	—	110	—	
Fall Time		t <sub>f</sub>	—	13	—	
Turn-on Switching Loss per Pulse		E <sub>ON</sub>	—	2155	—	μJ
Turn-off Switching Loss per Pulse		E <sub>OFF</sub>	—	745	—	
Diode Forward Voltage	V <sub>GS</sub> = -3 V, I <sub>SD</sub> = 120 A, T <sub>J</sub> = 25°C	V <sub>SD</sub>	—	4.67	6.2	V
	V <sub>GS</sub> = -3 V, I <sub>SD</sub> = 120 A, T <sub>J</sub> = 125°C		—	4.45	—	
	V <sub>GS</sub> = -3 V, I <sub>SD</sub> = 120 A, T <sub>J</sub> = 150°C		—	4.4	—	
Thermal Resistance – Chip-to-Case	M1, M2	R <sub>thJC</sub>	—	0.249	—	°C/W
Thermal Resistance – Chip-to-Heatsink	Thermal grease, Thickness = 2 Mil +2%, A = 2.8 W/mK	R <sub>thJH</sub>	—	0.466	—	°C/W

## THERMISTOR CHARACTERISTICS

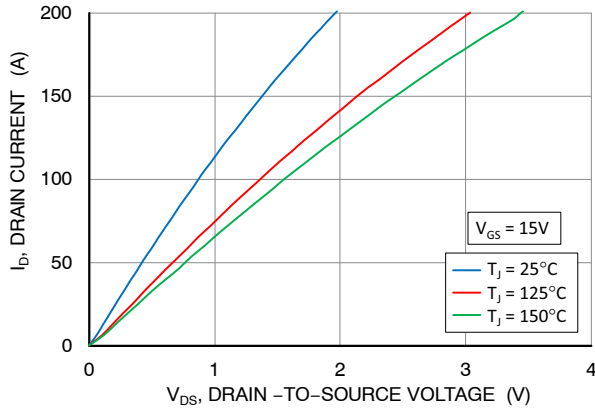
Nominal Resistance	T = 25°C	R <sub>25</sub>	—	5	—	kΩ
	T = 100°C	R <sub>100</sub>	—	493	—	Ω
	T = 150°C	R <sub>150</sub>	—	159.5	—	Ω
Deviation of R <sub>100</sub>	T = 100°C	ΔR/R	-5	—	5	%
Power Dissipation – Recommended Limit	0.15 mA, Non-self-heating Effect	P <sub>D</sub>	—	0.1	—	mW
Power Dissipation – Absolute Maximum	5 mA	P <sub>D</sub>	—	34.2	—	mW
Power Dissipation Constant			—	1.4	—	mW/K
B-value	B (25/50), tolerance ±2%		—	3375	—	K
B-value	B (25/100), tolerance ±2%		—	3436	—	K

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

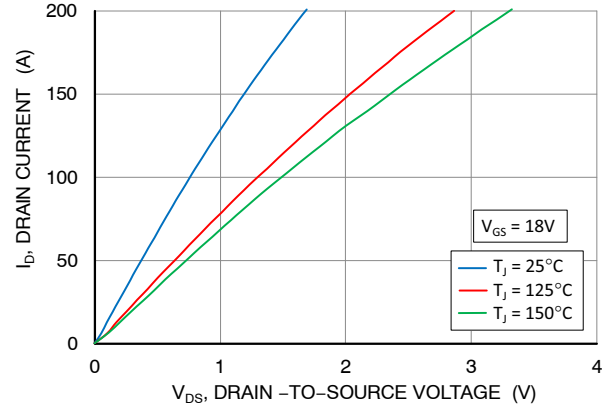
## ORDERING INFORMATION

Orderable Part Number	Marking	Package	Shipping
NXH008P120M3F1PTG	NXH008P120M3F1PTG	F1HALFBR: Case 180BW Press-fit Pins with pre-applied thermal interface material (TIM) (Pb-Free / Halide Free)	28 Units / Blister Tray
NXH008P120M3F1PG	NXH008P120M3F1PG	F1HALFBR: Case 180BW Press-fit Pins (Pb-Free / Halide Free)	28 Units / Blister Tray

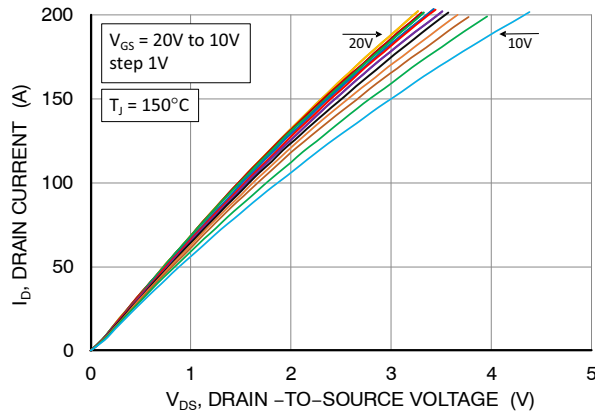
**TYPICAL CHARACTERISTIC**  
(M1/M2 SiC MOSFET CHARACTERISTIC)



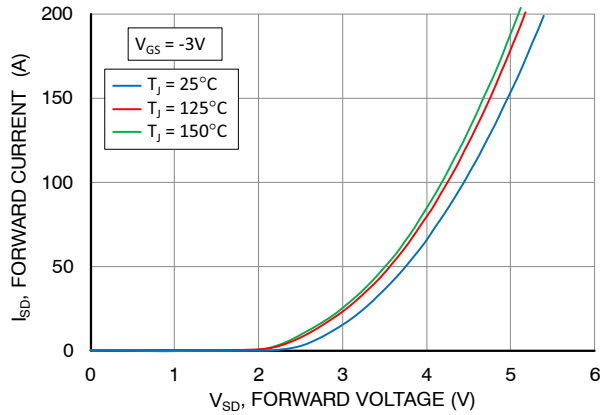
**Figure 2. MOSFET Typical Output Characteristic  $V_{GS} = 15\text{ V}$**



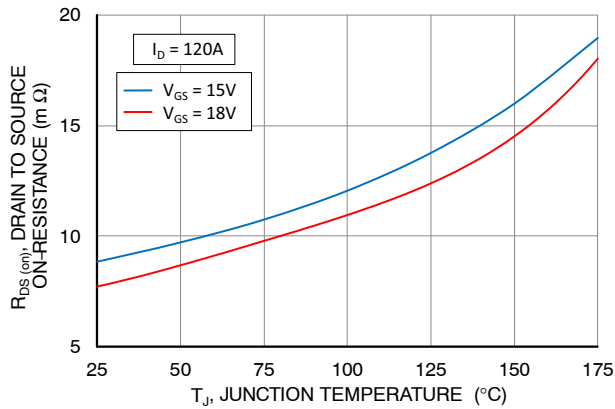
**Figure 3. MOSFET Typical Output Characteristic  $V_{GS} = 18\text{ V}$**



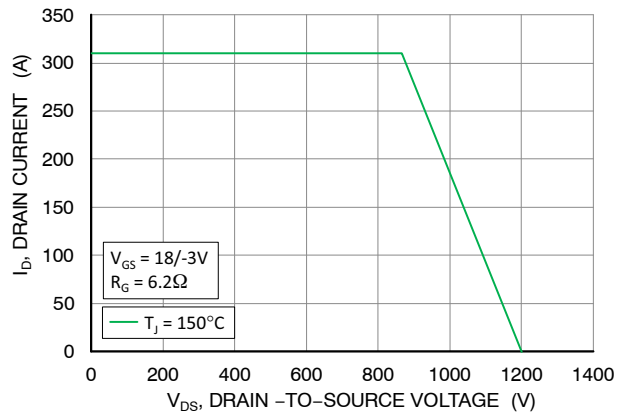
**Figure 4. MOSFET Typical Output Characteristic  $V_{GS} = \text{Var.}$**



**Figure 5. Body Diode Forward Characteristic**

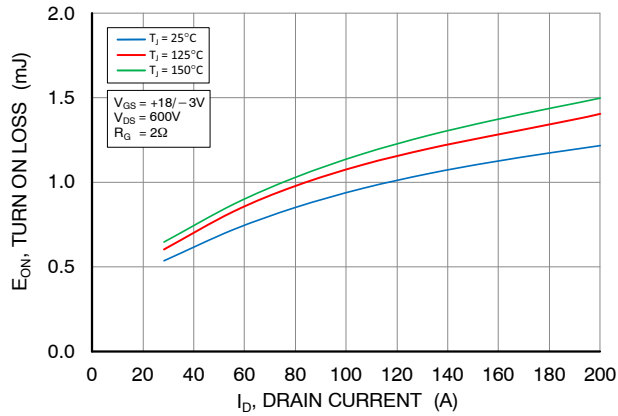


**Figure 6.  $R_{DS(on)}$  Drain-to-Source ON Resistance vs. Junction Temperature**

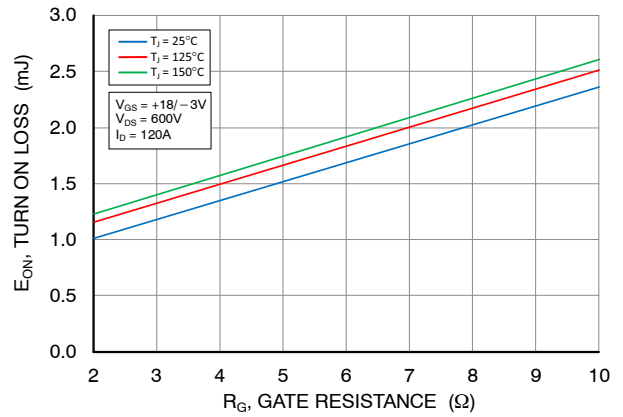


**Figure 7. Reverse Bias Safe Operating Area (RBSOA)**

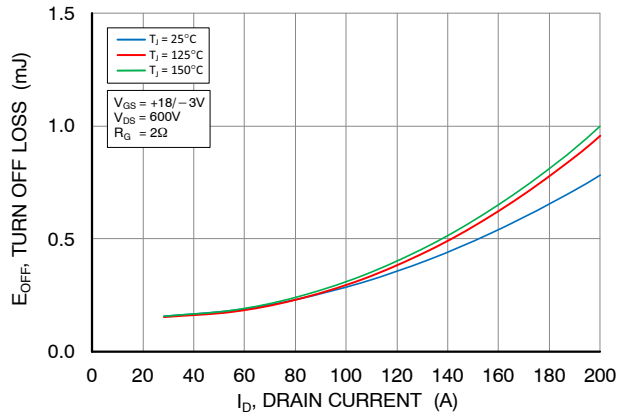
**TYPICAL CHARACTERISTICS**  
M1/M2 SIC MOSFET CHARACTERISTIC



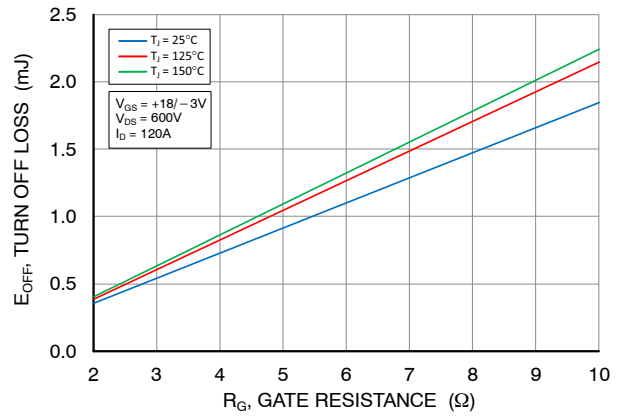
**Figure 8. Switching on Loss vs. Drain Current  $V_{DS} = 600$  V**



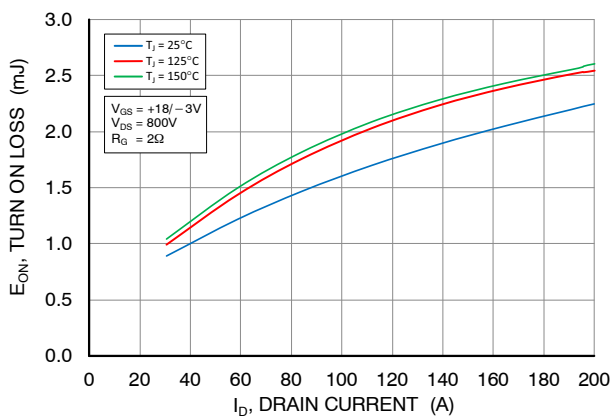
**Figure 9. Switching on Loss vs. Gate Resistance  $V_{DS} = 600$  V**



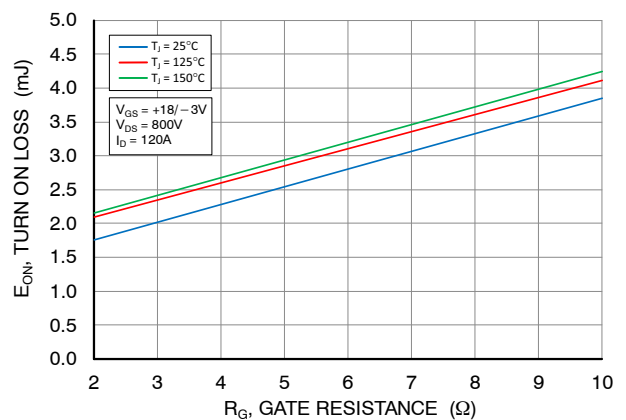
**Figure 10. Switching off Loss vs. Drain Current  $V_{DS} = 600$  V**



**Figure 11. Switching off Loss vs. Gate Resistance  $V_{DS} = 600$  V**



**Figure 12. Switching on Loss vs. Drain Current  $V_{DS} = 800$  V**



**Figure 13. Switching on Loss vs. Gate Resistance  $V_{DS} = 800$  V**

TYPICAL CHARACTERISTICS  
M1/M2 SIC MOSFET CHARACTERISTIC

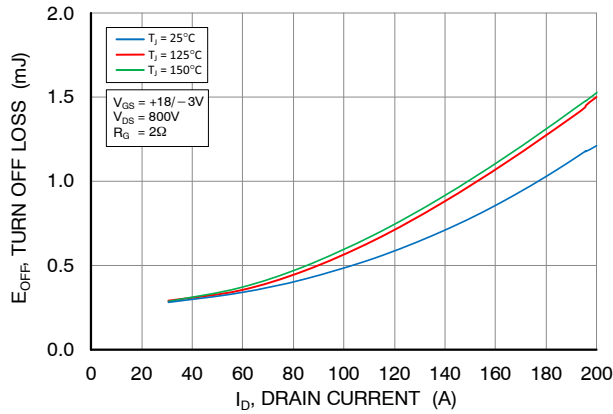


Figure 14. Switching off Loss vs. Drain Current  $V_{DS} = 800\text{ V}$

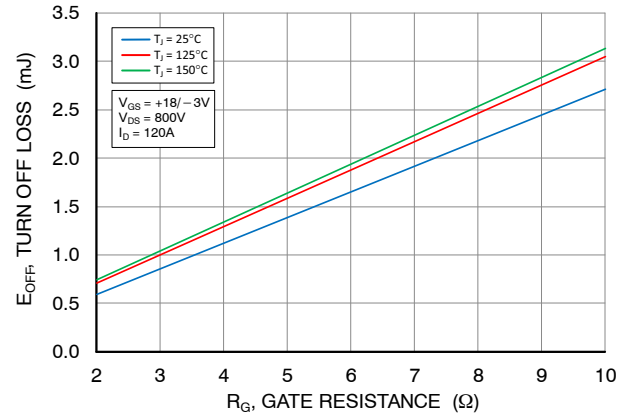


Figure 15. Switching off Loss vs. Gate Resistance  $V_{DS} = 800\text{ V}$

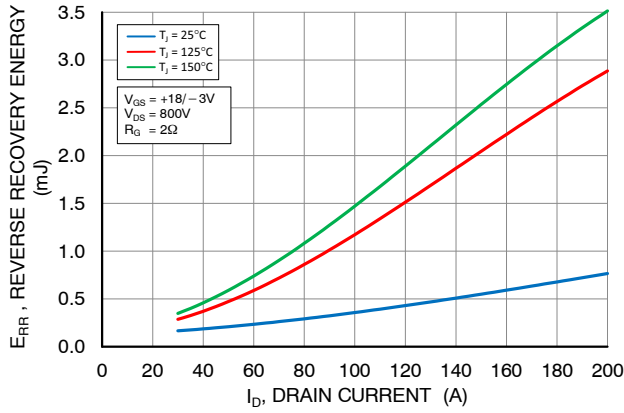


Figure 16. Reverse Recovery Energy vs. Drain Current  $V_{DS} = 800\text{ V}$

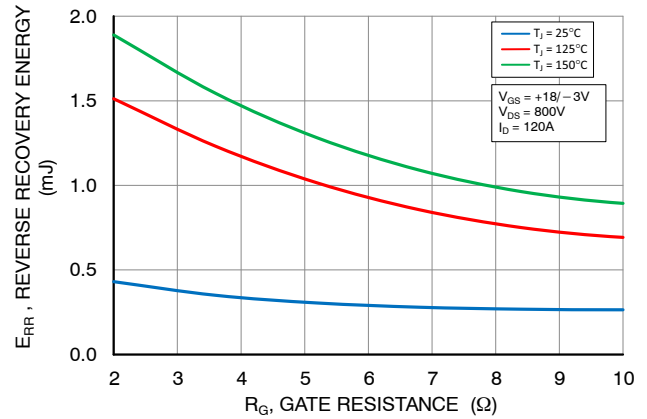


Figure 17. Reverse Recovery Energy vs. Gate Resistance  $V_{DS} = 800\text{ V}$

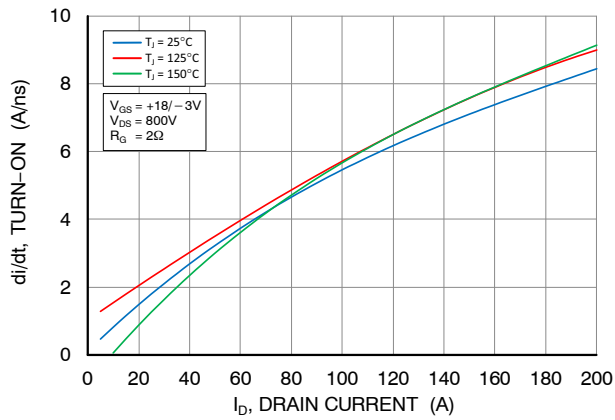


Figure 18. di/dt Turn ON vs. Drain Current  $V_{DS} = 800\text{ V}$

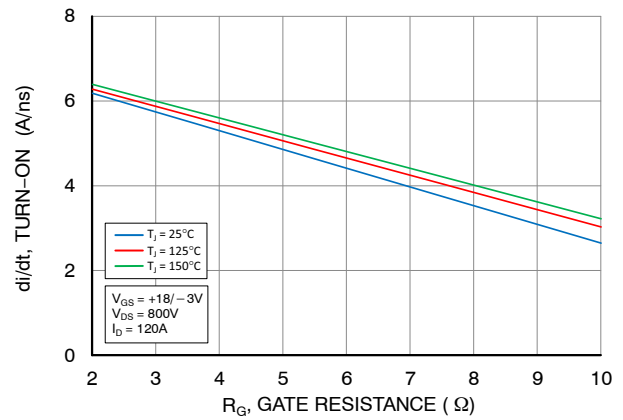
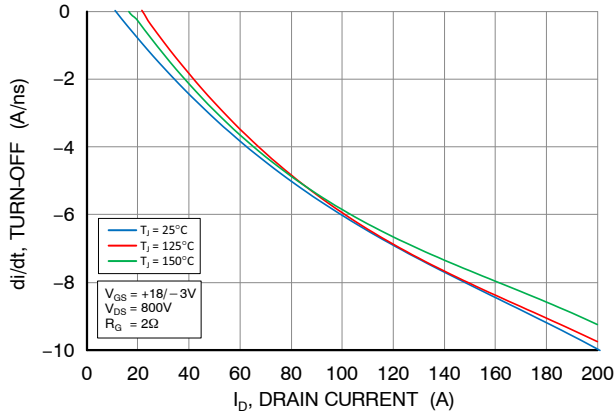
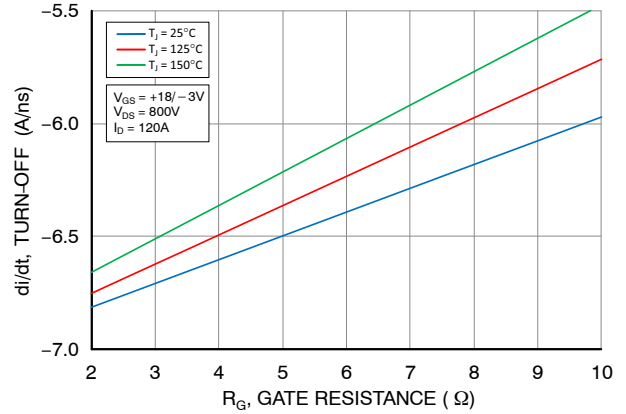


Figure 19. di/dt Turn ON vs. Gate Resistance  $V_{DS} = 800\text{ V}$

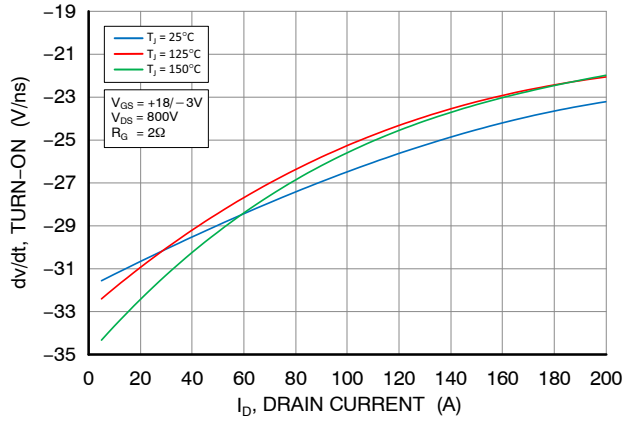
**TYPICAL CHARACTERISTICS**  
M1/M2 SIC MOSFET CHARACTERISTIC



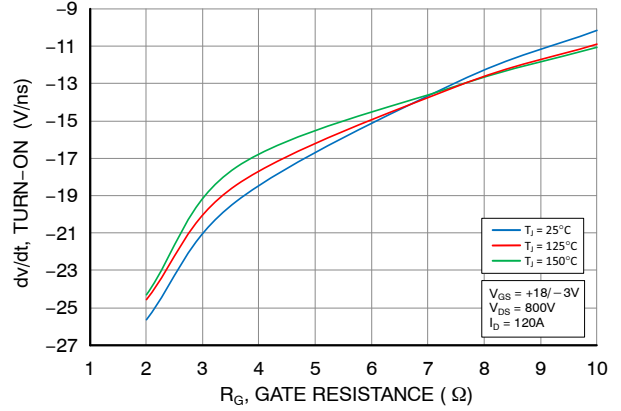
**Figure 20. di/dt Turn OFF vs. Drain Current**  
 $V_{DS} = 800 \text{ V}$



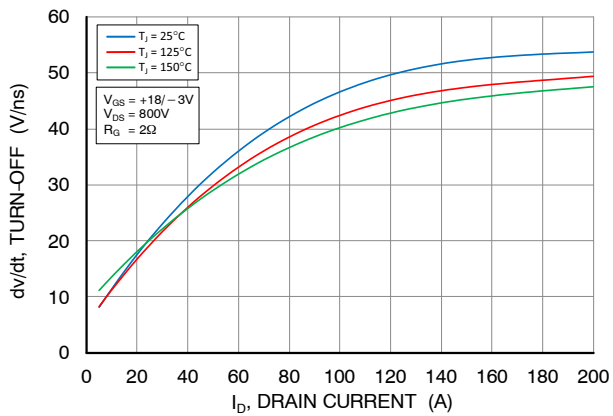
**Figure 21. di/dt Turn OFF vs. Gate Resistance  $V_{DS} = 800 \text{ V}$**



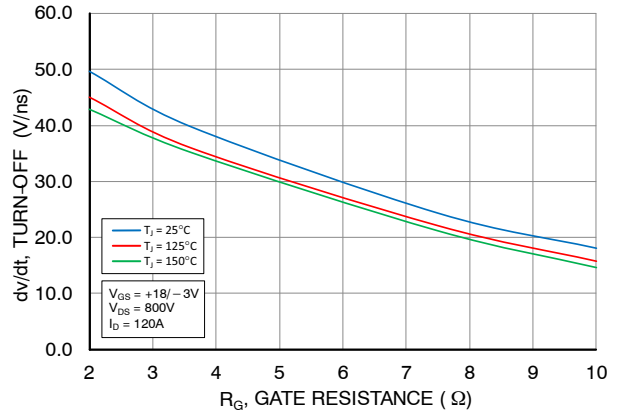
**Figure 22. dv/dt Turn ON vs. Drain Current**  
 $V_{DS} = 800 \text{ V}$



**Figure 23. dv/dt Turn ON vs. Gate Resistance  $V_{DS} = 800 \text{ V}$**

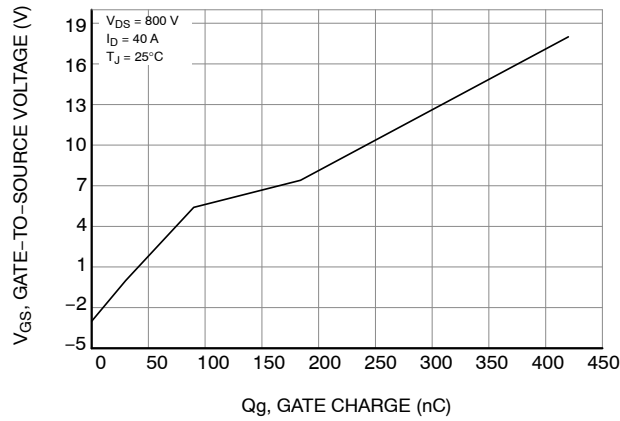


**Figure 24. dv/dt Turn OFF vs. Drain Current  $V_{DS} = 800 \text{ V}$**

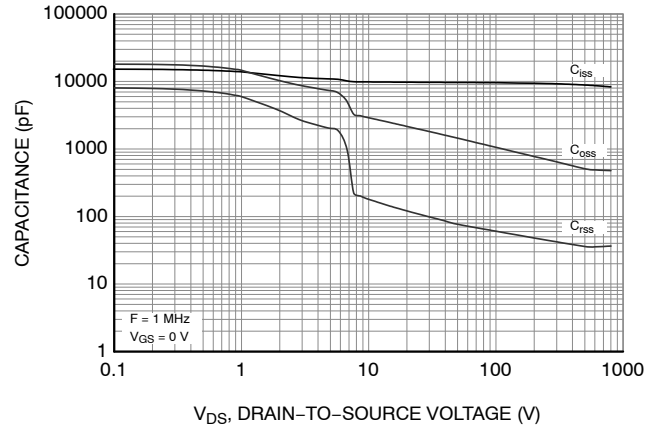


**Figure 25. dv/dt Turn OFF vs. Gate Resistance  $V_{DS} = 800 \text{ V}$**

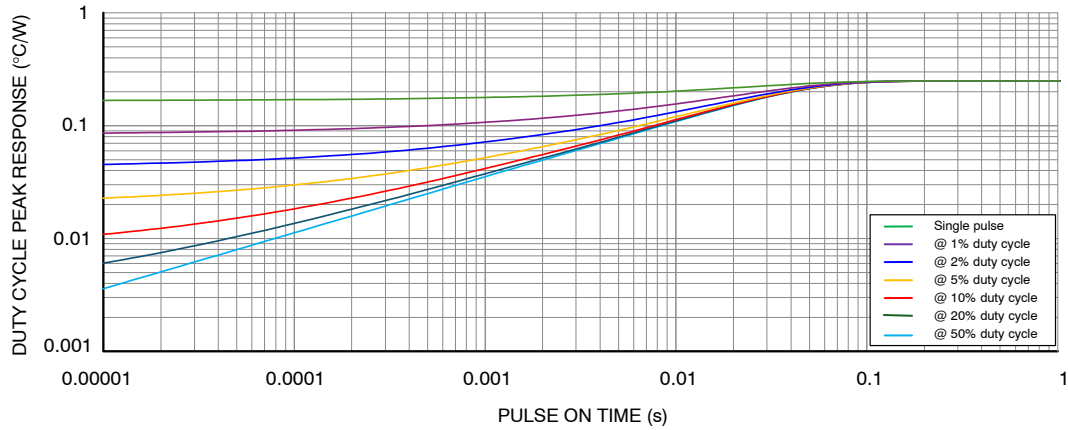
**TYPICAL CHARACTERISTICS**  
M1/M2 SIC MOSFET CHARACTERISTIC



**Figure 26. Gate-to-Source Voltage vs. Total Charge**



**Figure 27. Capacitance vs. Drain-to-Source Voltage**



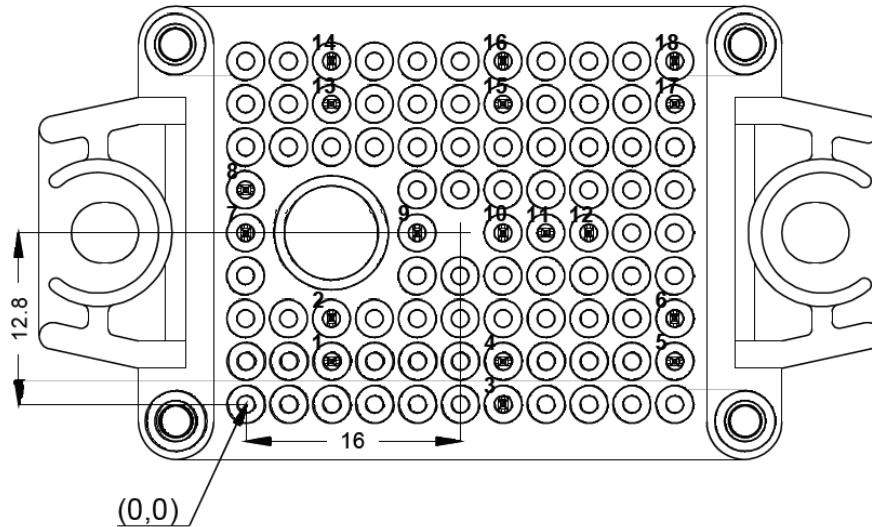
**Figure 28. Duty Cycle Response vs. Pulse On Time**

**Table 1. CAUER NETWORKS**

Cauer Element #	Rth (K/W)	Cth (Ws/K)
1	0.0015405	0.0032582
2	0.0034038	0.0011216
3	0.0167500	0.0053859
4	0.0498300	0.0154460
5	0.0925960	0.0870830
6	0.0540320	1.7250000

PIN POSITION INFORMATION

scale = 2.5 : 1

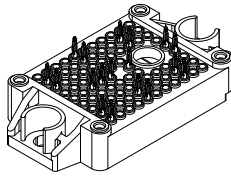


S Pin position

Pin #	X	Y	Function	Pin #	X	Y	Function
1	6.4	3.2	DC+	10	19.2	12.8	DC-
2	6.4	6.4	DC+	11	22.4	12.8	DC-
3	19.2	0.0	S1	12	25.6	12.8	DC-
4	19.2	3.2	G1	13	6.4	22.4	Phase
5	32.0	3.2	DC+	14	6.4	25.6	Phase
6	32.0	6.4	DC+	15	19.2	22.4	G2
7	0.0	12.8	TH2	16	19.2	25.6	S2
8	0.0	16.0	TH1	17	32.0	22.4	Phase
9	12.8	12.8	DC-	18	32.0	25.6	Phase

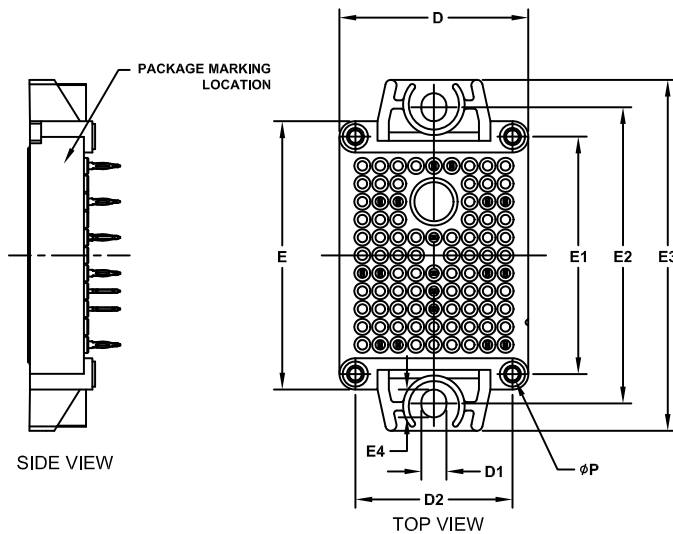
# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS



**PIM18 33.8x42.5 (PRESS FIT)**  
CASE 180BW  
ISSUE B

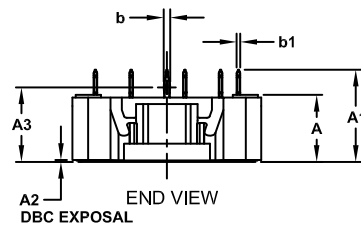
DATE 30 APR 2021



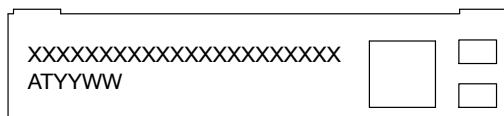
### NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS
2. PIN POSITION TOLERANCE IS  $\pm 0.4\text{mm}$

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	11.65	12.00	12.35
A1	16.00	16.50	17.00
A2	0.00	0.35	0.60
A3	12.85	13.35	13.85
b	1.15	1.20	1.25
b1	0.59	0.64	0.69
D	33.50	33.80	34.10
D1	4.40	4.50	4.60
D2	27.95	28.10	28.25
E	47.70	48.00	48.30
E1	42.35	42.50	42.65
E2	52.90	53.00	53.10
E3	62.30	62.80	63.30
E4	4.90	5.00	5.10
P	2.20	2.30	2.40

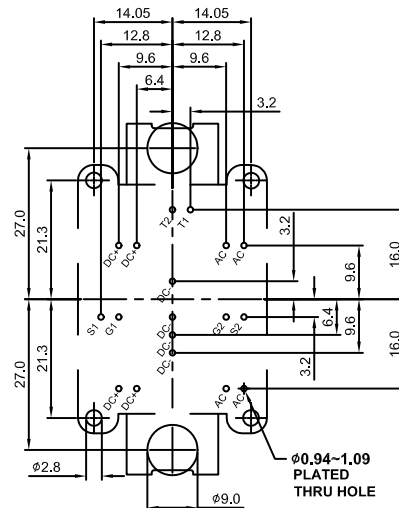


### GENERIC MARKING DIAGRAM\*



XXXXX = Specific Device Code  
AT = Assembly & Test Site Code  
YYWW = Year and Work Week Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



### RECOMMENDED MOUNTING PATTERN

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<b>DESCRIPTION:</b>	<b>PIM18 33.8x42.5 (PRESS FIT)</b>	<b>PAGE 1 OF 1</b>

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