

N-Channel 650V (D-S) Super Junction Power MOSFET

| PRODUCT SUMMARY | | |
|---|------------------------|------|
| V_{DS} (V) at T_J max. | 650 | |
| $R_{DS(on)}$ max. at 25 °C (Ω) | $V_{GS} = 10\text{ V}$ | 0.50 |
| Q_g max. (nC) | 25 | |
| Q_{gs} (nC) | 2.0 | |
| Q_{gd} (nC) | 2.7 | |
| Configuration | Single | |

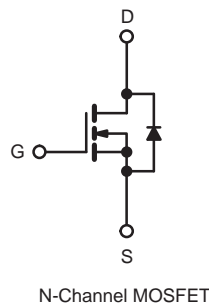
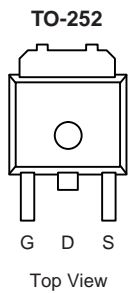
FEATURES

- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)



APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial

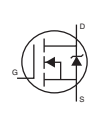


| ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted) | | | | |
|---|-----------------------------------|-----------------------------------|-------------|---------------------|
| PARAMETER | SYMBOL | | LIMIT | UNIT |
| Drain-Source Voltage | V_{DS} | | 650 | V |
| Gate-Source Voltage | V_{GS} | | ± 30 | |
| Continuous Drain Current ($T_J = 150\text{ }^\circ\text{C}$) | V_{GS} at 10 V | $T_C = 25\text{ }^\circ\text{C}$ | 9 | A |
| | | $T_C = 100\text{ }^\circ\text{C}$ | 6 | |
| Pulsed Drain Current ^a | I_{DM} | | 21 | |
| Linear Derating Factor | | | 1.5 | W/ $^\circ\text{C}$ |
| Single Pulse Avalanche Energy ^b | E_{AS} | | 86 | mJ |
| Maximum Power Dissipation | P_D | | 83 | W |
| Operating Junction and Storage Temperature Range | T_J, T_{stg} | | -55 to +150 | $^\circ\text{C}$ |
| Drain-Source Voltage Slope | $T_J = 125\text{ }^\circ\text{C}$ | | 50 | V/ns |
| Reverse Diode dV/dt ^d | | | 4.5 | |
| Soldering Recommendations (Peak Temperature) ^c | for 10 s | | 300 | $^\circ\text{C}$ |

Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 28.2\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 3.5\text{ A}$.
- 1.6 mm from case.
- $I_{SD} \leq I_D$, $dI/dt = 100\text{ A}/\mu\text{s}$, starting $T_J = 25\text{ }^\circ\text{C}$.

| THERMAL RESISTANCE RATINGS | | | | |
|----------------------------------|------------|------|------|------|
| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
| Maximum Junction-to-Ambient | R_{thJA} | - | 63 | °C/W |
| Maximum Junction-to-Case (Drain) | R_{thJC} | - | 0.6 | |

| SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted) | | | | | | | |
|---|---------------------|--|---|------|------|-----------|---------------|
| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
| Static | | | | | | | |
| Drain-Source Breakdown Voltage | V_{DS} | $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$ | | 650 | - | - | V |
| V_{DS} Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to $25\text{ }^\circ\text{C}, I_D = 1\text{ mA}$ | | - | 0.65 | - | V/°C |
| Gate-Source Threshold Voltage (N) | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | | 2 | - | 4 | V |
| Gate-Source Leakage | I_{GSS} | $V_{GS} = \pm 20\text{ V}$ | | - | - | ± 100 | nA |
| | | $V_{GS} = \pm 30\text{ V}$ | | - | - | ± 1 | μA |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$ | | - | - | 1 | μA |
| | | $V_{DS} = 520\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$ | | - | - | 10 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}$ | $I_D = 4\text{ A}$ | - | 0.50 | - | Ω |
| Forward Transconductance | g_{fs} | $V_{DS} = 30\text{ V}, I_D = 4\text{ A}$ | | - | 16 | - | S |
| Dynamic | | | | | | | |
| Input Capacitance | C_{iss} | $V_{GS} = 0\text{ V}, V_{DS} = 100\text{ V}, f = 1\text{ MHz}$ | | - | 360 | - | pF |
| Output Capacitance | C_{oss} | | | - | 25 | - | |
| Reverse Transfer Capacitance | C_{rss} | | | - | 12 | - | |
| Effective Output Capacitance, Energy Related ^a | $C_{o(er)}$ | $V_{DS} = 0\text{ V to } 520\text{ V}, V_{GS} = 0\text{ V}$ | | - | 45 | - | |
| Effective Output Capacitance, Time Related ^b | $C_{o(tr)}$ | | | - | 62 | - | |
| Total Gate Charge | Q_g | $V_{GS} = 10\text{ V}$ | $I_D = 4\text{ A}, V_{DS} = 520\text{ V}$ | - | 25 | - | nC |
| Gate-Source Charge | Q_{gs} | | | - | 2.0 | - | |
| Gate-Drain Charge | Q_{gd} | | | - | 2.7 | - | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = 520\text{ V}, I_D = 4\text{ A}, V_{GS} = 10\text{ V}, R_g = 9.1\text{ }\Omega$ | | - | 25 | - | ns |
| Rise Time | t_r | | | - | 55 | - | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | - | 70 | - | |
| Fall Time | t_f | | | - | 40 | - | |
| Gate Input Resistance | R_g | $f = 1\text{ MHz}, \text{open drain}$ | | - | 3.5 | - | Ω |
| Drain-Source Body Diode Characteristics | | | | | | | |
| Continuous Source-Drain Diode Current | I_S | MOSFET symbol showing the integral reverse p - n junction diode  | | - | - | 7 | A |
| Pulsed Diode Forward Current | I_{SM} | | | - | - | 18 | |
| Diode Forward Voltage | V_{SD} | $T_J = 25\text{ }^\circ\text{C}, I_S = 4\text{ A}, V_{GS} = 0\text{ V}$ | | - | - | 1.5 | V |
| Reverse Recovery Time | t_{rr} | $T_J = 25\text{ }^\circ\text{C}, I_F = I_S = 4\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}, V_R = 400\text{ V}$ | | - | 190 | - | ns |
| Reverse Recovery Charge | Q_{rr} | | | - | 2.3 | - | μC |
| Reverse Recovery Current | I_{RRM} | | | - | 10 | - | A |

Notes

- $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .
- $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Fig. 1 - Typical Output Characteristics

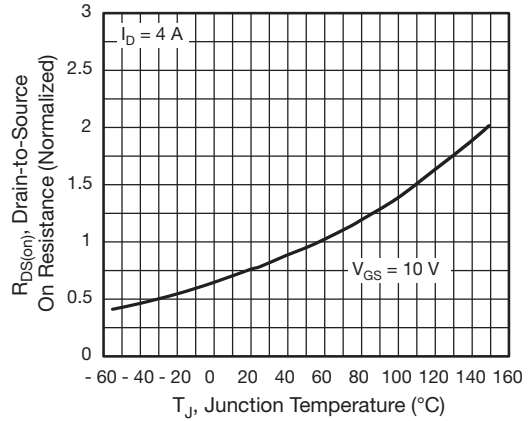


Fig. 4 - Normalized On-Resistance vs. Temperature



Fig. 2 - Typical Output Characteristics



Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



Fig. 3 - Typical Transfer Characteristics



Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



Fig. 7 - Typical Source-Drain Diode Forward Voltage



Fig. 9 - Maximum Drain Current vs. Case Temperature



Fig. 8 - Maximum Safe Operating Area

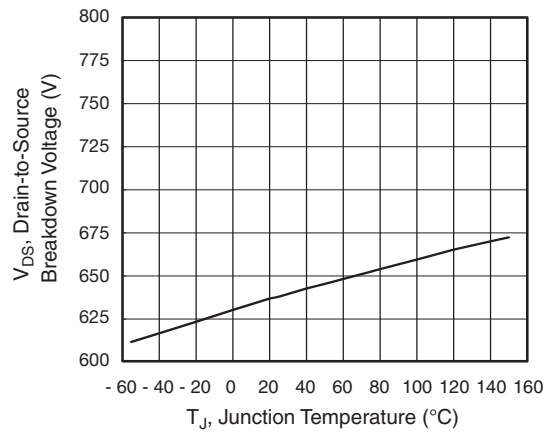


Fig. 10 - Temperature vs. Drain-to-Source Voltage



Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case

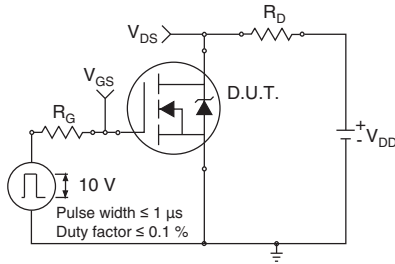


Fig. 12 - Switching Time Test Circuit



Fig. 16 - Basic Gate Charge Waveform



Fig. 13 - Switching Time Waveforms

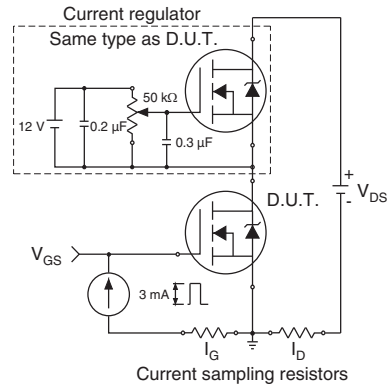


Fig. 17 - Gate Charge Test Circuit



Fig. 14 - Unclamped Inductive Test Circuit



Fig. 15 - Unclamped Inductive Waveforms

Peak Diode Recovery dV/dt Test Circuit

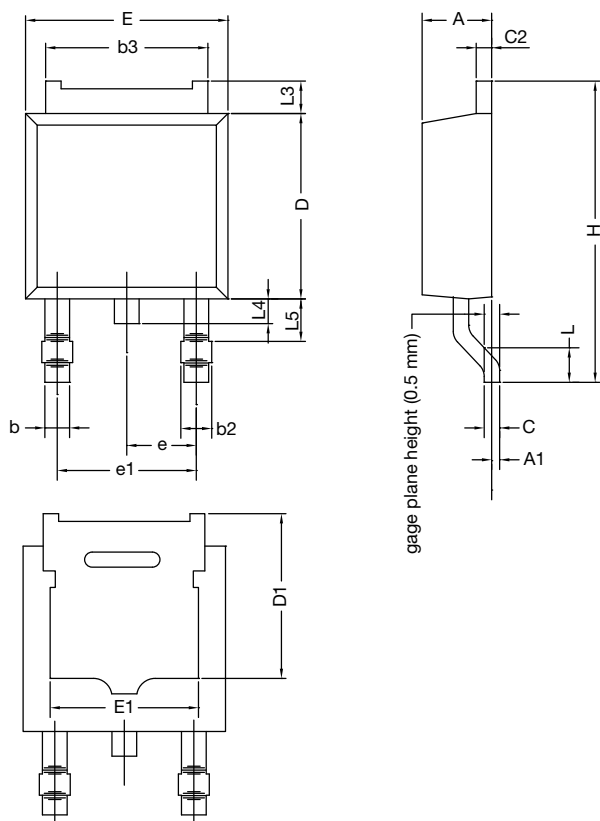


Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 18 - For N-Channel

TO-252AA CASE OUTLINE



| DIM. | MILLIMETERS | | INCHES | |
|------|-------------|-------|-----------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| A | 2.18 | 2.38 | 0.086 | 0.094 |
| A1 | - | 0.127 | - | 0.005 |
| b | 0.64 | 0.88 | 0.025 | 0.035 |
| b2 | 0.76 | 1.14 | 0.030 | 0.045 |
| b3 | 4.95 | 5.46 | 0.195 | 0.215 |
| C | 0.46 | 0.61 | 0.018 | 0.024 |
| C2 | 0.46 | 0.89 | 0.018 | 0.035 |
| D | 5.97 | 6.22 | 0.235 | 0.245 |
| D1 | 5.21 | - | 0.205 | - |
| E | 6.35 | 6.73 | 0.250 | 0.265 |
| E1 | 4.32 | - | 0.170 | - |
| H | 9.40 | 10.41 | 0.370 | 0.410 |
| e | 2.28 BSC | | 0.090 BSC | |
| e1 | 4.56 BSC | | 0.180 BSC | |
| L | 1.40 | 1.78 | 0.055 | 0.070 |
| L3 | 0.89 | 1.27 | 0.035 | 0.050 |
| L4 | - | 1.02 | - | 0.040 |
| L5 | 1.14 | 1.52 | 0.045 | 0.060 |

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DWG: 5347

Note

- Dimension L3 is for reference only.

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