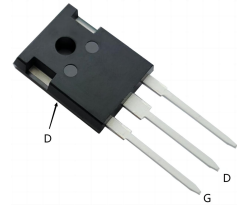
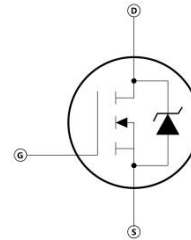


**Features**

- 100% avalanche tested
- Avalanche ruggedness
- Gate charge minimized
- Very low intrinsic capacitance
- Very low on-resistance


**Applications**

- UPS
- PV Inverter
- Switching applications


**Electrical ratings**

Absolute maximum ratings			
Parameter	Symbol	Value	Unit
Drain-source voltage ( $V_{GS} = 0$ )	$V_{DS}$	850	V
Gate- source voltage	$V_{GS}$	$\pm 30$	
Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	$I_D$	50	A
Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$		28	
Drain current (pulsed)	$I_{DM}$	125	
continuous pulse avalanche current	$I_{AR}$	25	A
Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	$E_{AS}$	1000	mJ
Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	$P_{TOT}$	890	W
Derating factor		2.23	W/ $^\circ\text{C}$
Operating junction temperature	$T_J$	-55 to 150	$^\circ\text{C}$
Storage temperature	$T_{stg}$		
Maximum lead temperature for soldering purpose	$T_L$	260	
Isolation Voltage for terminal to case	$V_{ISO}$	3.0	KV

**Electrical Characteristics ( $T_{vj} = 25\text{ }^\circ\text{C}$  unless otherwise specified)**

On /off states						
Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	850			V
Zero gate voltage drain current ( $V_{GS} = 0$ )	$I_{DSS}$	$V_{DS} = \text{Max rating}$			50	$\mu\text{A}$
		$V_{DS} = \text{Max rating}$ , $T_C = 125\text{ }^\circ\text{C}$			3000	

Gate-body leakage current ( $V_{DS} = 0$ )	$I_{GSS}$	$V_{GS} = \pm 30 V$			$\pm 100$	nA
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu A$	3	4	5	V
Static drain-source on resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 16A$ @25°C		111		mΩ
<b>Dynamic</b>						
<b>Parameter</b>	<b>Symbol</b>	<b>Test conditions</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Unit</b>
Input capacitance	$C_{iss}$	$V_{DS}=25V, f=1MHz, V_{GS}=0$		3010		pF
Output capacitance	$C_{oss}$			1200		
Reverse transfer capacitance	$C_{rss}$			10		
Gate input resistance	$R_g$	f=1MHz Gate DC Bias=0 Test signal level=20mV open drain		2.0		Ω
	Gfs	$V_{DS}=10V, I_D=25A$	19	32		S
Total gate charge	$Q_g$	$V_{DD}=425V, I_D=25A$ $V_{GS}=10V$		178		nC
Gate-source charge	$Q_{gs}$			23		
Gate-drain charge	$Q_{gd}$			63		
Gate plateau voltage	$V_P$			6		V
<b>Switching times</b>						
<b>Parameter</b>	<b>Symbol</b>	<b>Test conditions</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Unit</b>
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 425 V, I_D = 25A,$ $R_G = 10\Omega, V_{GS} = 10 V$		31		ns
Rise time	$t_r$			43		
Turn-off-delay time	$t_{d(off)}$			85		
Fall time	$t_f$			13		
<b>Source drain diode</b>						
<b>Parameter</b>	<b>Symbol</b>	<b>Test conditions</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Unit</b>
Forward on voltage	$V_{SD}$	$I_{SD} = 25 A, V_{GS} = 0V$		0.85	1.2	V
Reverse recovery time	$t_{rr}$	$I_{SD} = 25A, di/dt = 100A/\mu s$ $V_R = 100 V$		210		ns
Reverse recovery charge	$Q_{rr}$			1.75		μC
Reverse recovery current	$I_{RRM}$			15		A

<b>Thermal data</b>			
<b>Parameter</b>	<b>Symbol</b>	<b>Value</b>	<b>Unit</b>
Thermal resistance junction-case max	$R_{thj-case}$	0.21	°C/W
Thermal resistance junction-ambient max	$R_{thj-amb}$	40	

Electrical characteristics

Fig. 1. Output Characteristics @  $T_J = 25^\circ\text{C}$

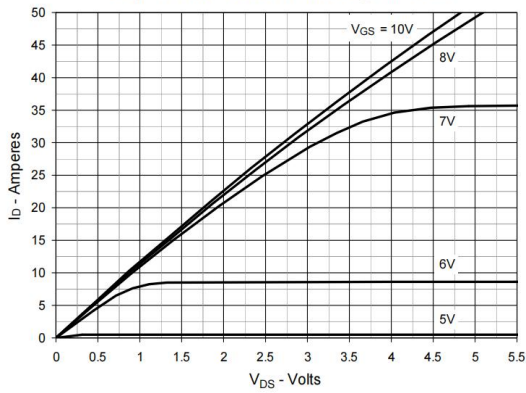


Fig. 2. Extended Output Characteristics @  $T_J = 25^\circ\text{C}$

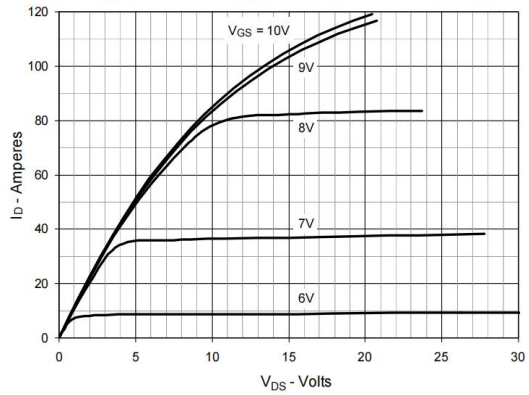


Fig. 3. Output Characteristics @  $T_J = 125^\circ\text{C}$

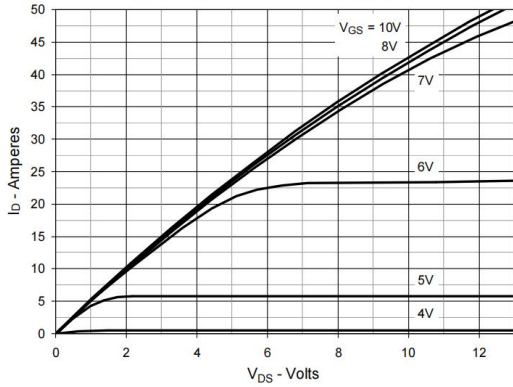


Fig. 4.  $R_{DS(on)}$  Normalized to  $I_D = 25A$  Value vs. Junction Temperature

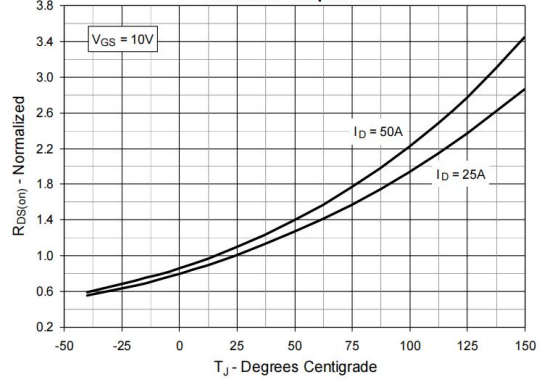


Fig. 5.  $R_{DS(on)}$  Normalized to  $I_D = 25A$  Value vs. Drain Current

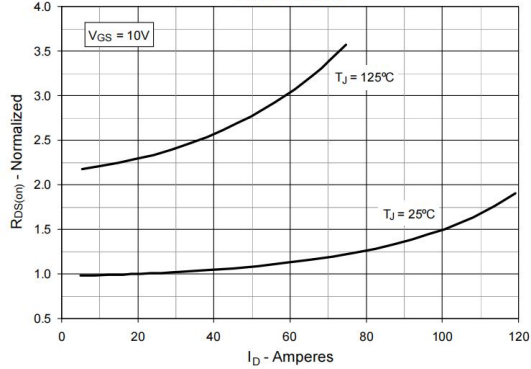
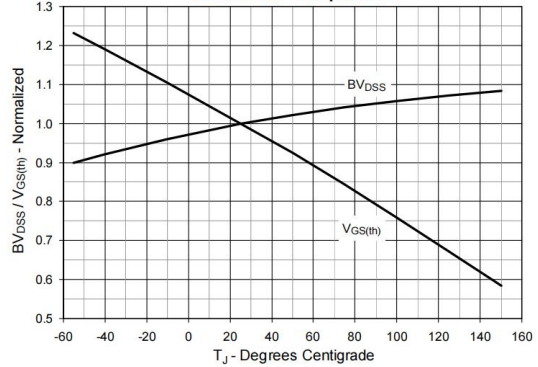
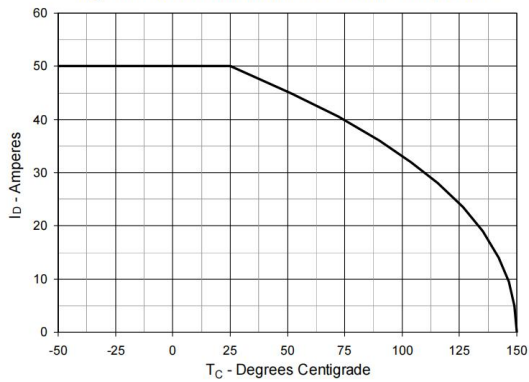


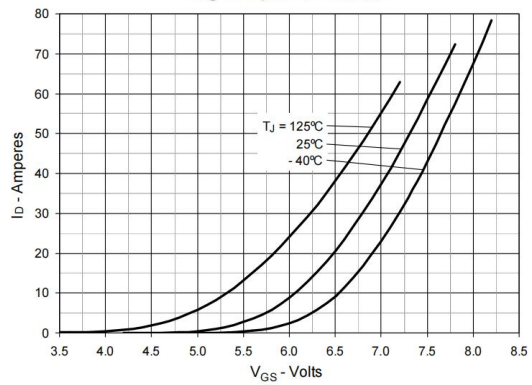
Fig. 6. Normalized Breakdown & Threshold Voltages vs. Junction Temperature



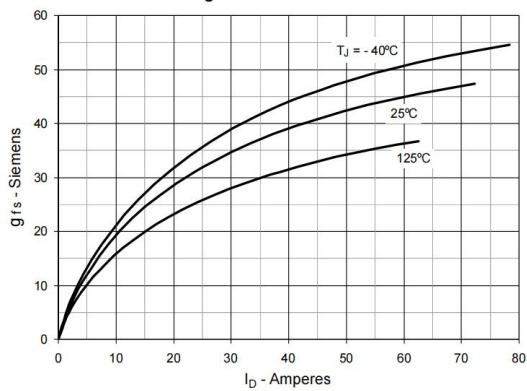
**Fig. 7. Maximum Drain Current vs. Case Temperature**



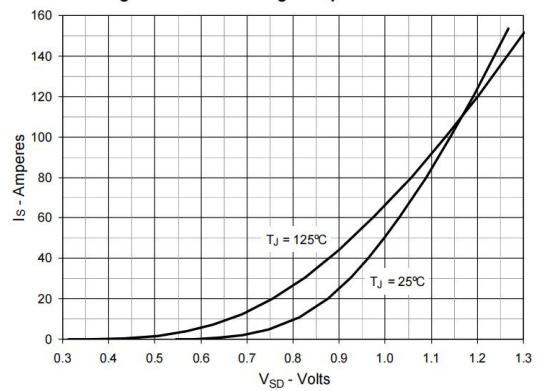
**Fig. 8. Input Admittance**



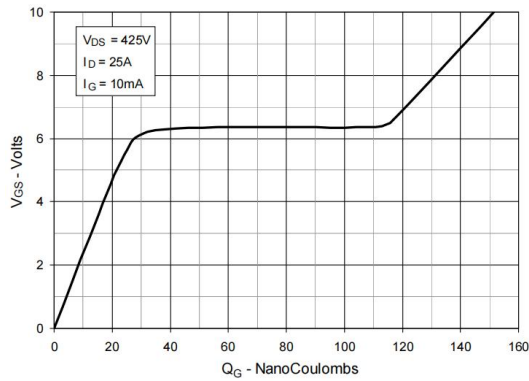
**Fig. 9. Transconductance**



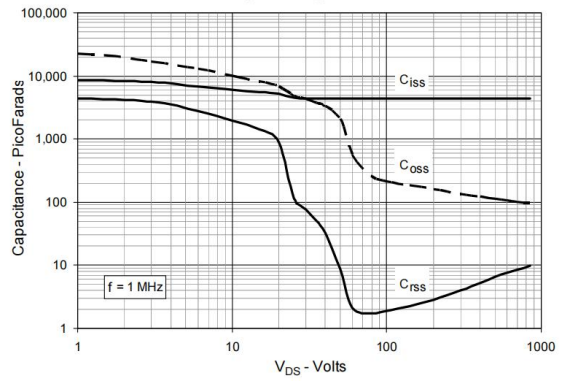
**Fig. 10. Forward Voltage Drop of Intrinsic Diode**



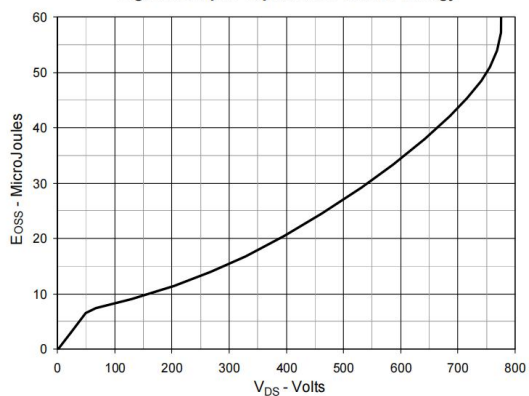
**Fig. 11. Gate Charge**



**Fig. 12. Capacitance**



**Fig. 13. Output Capacitance Stored Energy**



**Fig. 14. Forward-Bias Safe Operating Area**

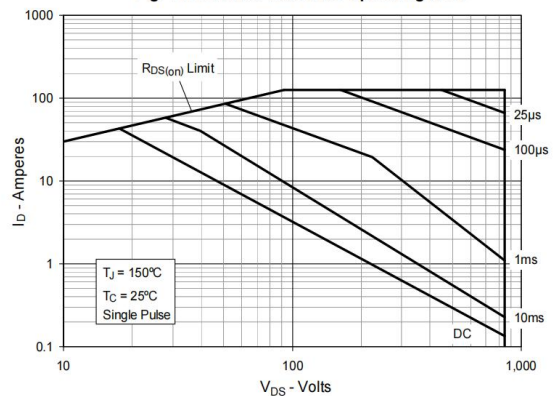
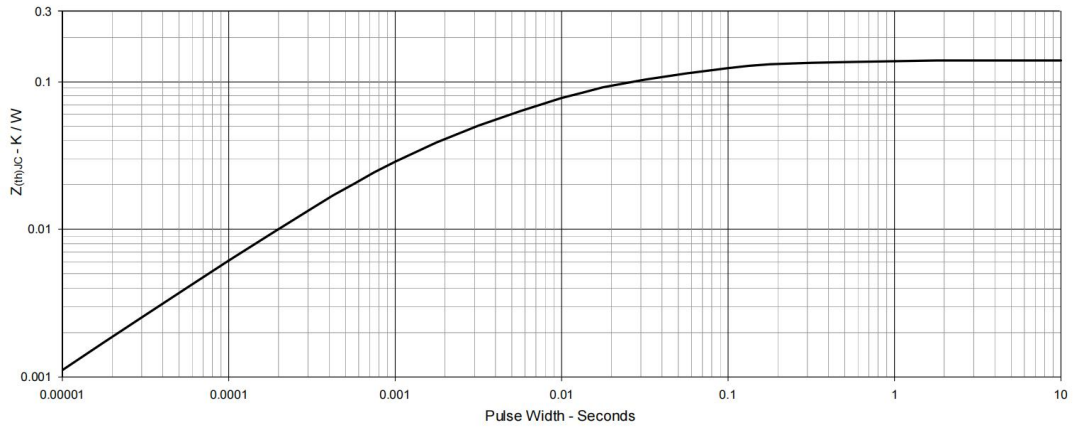


Fig. 15. Maximum Transient Thermal Impedance



Package outline dimension

