SGM25062
6-Channel Load Switch with I²C Control

GENERAL DESCRIPTION

The SGM25062 is a 6-channel low R_{ON} load switch, which can support a continuous load current of up to 2A. The device can operate over a wide input voltage range of 1.2V to 5.5V.

The switch can be controlled by I²C signal directly. Through the I²C interface, it can control the register to set the commands, so as to control the on/off, discharge and power-up sequence of each channel.

The SGM25062 is available in a Green WLCSP-1.55×1.55-16B-A package and operates over a temperature range of -40℃ to +85℃.

FEATURES

- **Integrated 6-Channel Load Switch**
- **1.2V to 5.5V Input Voltage Range/Channel**
- **VSYS Operating Voltage Range: 1.5V to 5.5V**
- **Low On-Resistance:**
  - **R_{ON1} = 55mΩ (TYP) at V_{SYS} = 5.5V**
  - **R_{ON1} = 62mΩ (TYP) at V_{SYS} = 1.5V**
- **Maximum Continuous Load Current: 2A**
- **I²C Interface Control to Program Each Channel Power-up Sequence**
- **-40℃ to +85℃ Operating Temperature Range**
- **Available in a Green WLCSP-1.55×1.55-16B-A Package**

APPLICATIONS

Smartphones, Tablets
Battery-Powered Devices
Cameras, DVRs, Camcorders and STB

TYPICAL APPLICATION

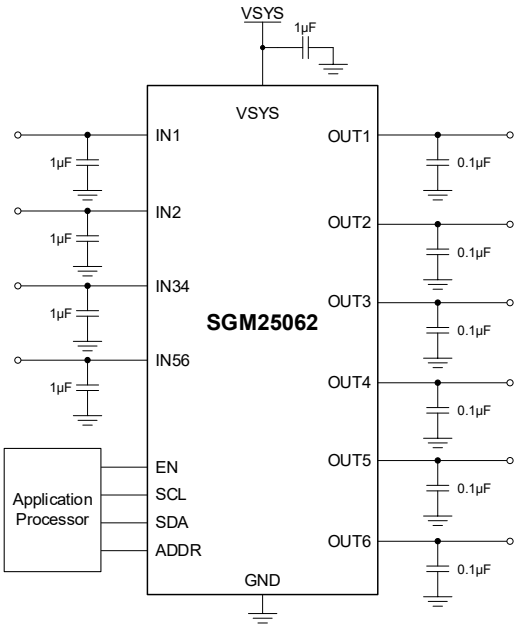


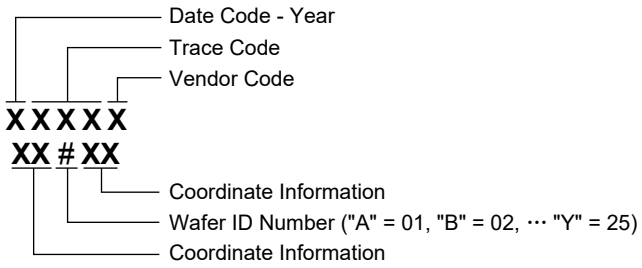
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM25062	WLCSP-1.55×1.55-16B-A	-40℃ to +85℃	SGM25062YG/TR	040 XXXXX XX#XX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

INx, OUTx, VSYS Pins Voltage Range ..... -0.3V to 6V
Other Pins Voltage Range..... -0.3V to V_{SYS} + 0.3V
Each Channel Maximum Load Current 2A
Package Thermal Resistance
WLCSP-1.55×1.55-16B-A, θ_{JA} ..... 102℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM..... 4000V
CDM..... 1000V

RECOMMENDED OPERATING CONDITIONS

Operating Ambient Temperature Range ..... -40℃ to +85℃
Operating Junction Temperature Range ..... -40℃ to +125℃

NOTES:

1. The control enable bit LDSWx_EN needs to be reset to the default value if V_{INx} is floating or lower than the minimum operation voltage.

2. It is not recommended that V_{INx} is powered on before V_{SYS}.

3. It is not recommended that the $V_{PULL-UP}$ of I²C is lower than V_{SYS}, in case of the unexpected leakage current from V_{SYS} to GND.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

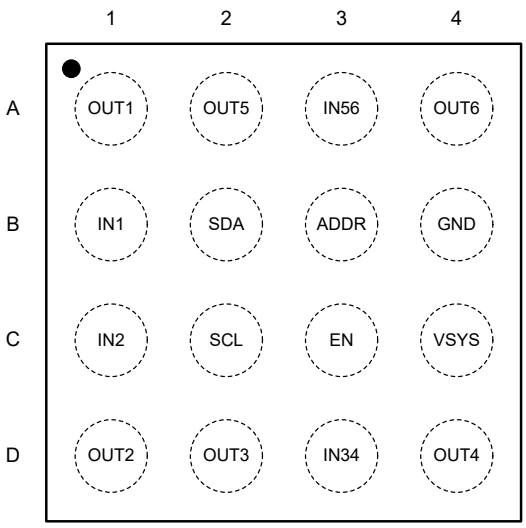
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-1.55×1.55-16B-A

PIN DESCRIPTION

PIN	NAME	FUNCTION
A1	OUT1	Output 1 of the Device.
A2	OUT5	Output 5 of the Device.
A3	IN56	Input Power Supply for Load Switch 5 and 6.
A4	OUT6	Output 6 of the Device.
B1	IN1	Input Power Supply for Load Switch 1.
B2	SDA	I^2C Data Signal.
B3	ADDR	I^2C Address Set Pin.
B4	GND	Ground.
C1	IN2	Input Power Supply for Load Switch 2.
C2	SCL	I^2C Clock Signal.
C3	EN	Enable Control Pin. Apply high to enable device, and low to reset all registers to their default values.
C4	VSYS	System Power Supply.
D1	OUT2	Output 2 of the Device.
D2	OUT3	Output 3 of the Device.
D3	IN34	Input Power Supply for Load Switch 3 and 4.
D4	OUT4	Output 4 of the Device.

ELECTRICAL CHARACTERISTICS

(C_{VSYS} = 1μF, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VSYS Supply Voltage Range	V_{SYS}		1.5		5.5	V
VSYS Quiescent Current	$I_{Q\_ON\_VSYS}$	One channel on, V_{INx} = V_{SYS} = 5.5V		0.6	1	μA
		All channels on, V_{IN1} = V_{IN2} = V_{IN34} = V_{IN56} = V_{SYS} = 5.5V		1.2	2.5	
VSYS Shutdown Current	$I_{Q\_OFF\_VSYS}$	V_{EN} = 0V and V_{ADDR} = V_{SCL} = V_{SDA} = 0V or V_{ADDR} = V_{SCL} = V_{SDA} = V_{SYS} = V_{IN1} = V_{IN2} = V_{IN34} = V_{IN56} = 1.5V		0.1	0.5	μA
		V_{EN} = 0V and V_{ADDR} = V_{SCL} = V_{SDA} = 0V or V_{ADDR} = V_{SCL} = V_{SDA} = V_{SYS} = V_{IN1} = V_{IN2} = V_{IN34} = V_{IN56} = 5.5V		0.2	0.5	
EN Pin Pull-Down Resistance	R_{EN}		8	17		MΩ
EN Pin Leakage Current	I_{EN}	V_{EN} = 5V		0.3	0.5	μA
EN Pin Input High Voltage	V_{IH}		1.2			V
EN Pin Input Low Voltage	V_{IL}				0.4	V
SCL/SDA Pins Input High Voltage	V_{I2CH}		1.2			V
SCL/SDA Pins Input Low Voltage	V_{I2CL}				0.4	V
SDA Pin Logic Low Output	V_{OL}	3mA sinking current			0.3	V
SCL/SDA Pins Input Current	I_{I2C}	V_{EN} = 0V, V_{SCL} = V_{SDA} = V_{SYS} or V_{SCL} = V_{SDA} = 0V		0.1		μA
SCL Pin Clock Frequency	f_{SCL}				400	kHz

(V_{IN1} = V_{IN2} = V_{IN34} = V_{IN56} = 1.2V to 5.5V, V_{SYS} = 1.5V to 5.5V, T_J = -40℃ to +85℃, typical values are at V_{INx} = 3.3V and T_J = +25℃, unless otherwise noted.)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Basic Operation						
Input Voltage	V_{INx}		1.2		5.5	V
Off Supply Current of One Channel	I_{Q_OFF}	V_{EN} = 0V, V_{OUTx} floating, V_{INx} = 5.5V		0.1	0.5	μA
Leakage Current of One Channel	$I_{LEAKAGE\_IN}$	V_{EN} = 0V, V_{OUTx} = 0V, V_{INx} = 5.5V		0.1	0.6	μA
Quiescent Current of One Channel	I_Q	Channelx enabled, I_{OUTx} = 0mA, V_{INx} = 5.5V		0.37	1.0	μA
		Channelx enabled, I_{OUTx} = 0mA, V_{INx} = 3.3V		0.29	0.9	
		Channelx enabled, I_{OUTx} = 0mA, V_{INx} = 1.2V		0.26	0.8	
OUTx Leakage Current	$I_{LEAKAGE\_OUT}$	LDSW off, QOD disabled, V_{OUTx} = 5.0V, V_{INx} = short to GND			0.5	μA
On-Resistance	$R_{ON1/2}$	$V_{IN1/2}$ = 3.3V, $I_{OUT1/2}$ = 200mA, V_{SYS} = 1.5V		62	120	mΩ
		$V_{IN1/2}$ = 3.3V, $I_{OUT1/2}$ = 200mA, V_{SYS} = 3.3V		56	110	
		$V_{IN1/2}$ = 3.3V, $I_{OUT1/2}$ = 200mA, V_{SYS} = 5.5V		55	100	
	$R_{ON34/56}$	$V_{IN34/56}$ = 3.3V, $I_{OUT34/56}$ = 200mA, V_{SYS} = 1.5V		53	110	
		$V_{IN34/56}$ = 3.3V, $I_{OUT34/56}$ = 200mA, V_{SYS} = 3.3V		47	100	
		$V_{IN34/56}$ = 3.3V, $I_{OUT34/56}$ = 200mA, V_{SYS} = 5.5V		46	90	
OUTx Pin Discharge Resistance (Default)	R_{PD}	V_{SYS} = 3.3V, V_{EN} = 0V, I_{SINK_OUTx} = 1mA		44	80	Ω
True Reverse Current Blocking						
RCB Protection Trip Point	V_{T_RCB}	V_{OUTx} - V_{INx}		70		mV
RCB Protection Release Trip Point	V_{R_RCB}	V_{INx} - V_{OUTx}		90		mV
RCB Hysteresis				160		mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1} = V_{IN2} = V_{IN34} = V_{IN56} = 1.2V to 5.5V, V_{SYS} = 1.5V to 5.5V, T_J = -40℃ to +85℃, typical values are at V_{INx} = 3.3V and T_J = +25℃, unless otherwise noted.)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Dynamic Characteristics (See Figure 2)						
Turn-On Delay	t_{DON}	V_{INx} = 3.3V, R_{Lx} = 150Ω, C_{Lx} = 0.1μF		485		μs
V_{OUTx} Rise Time	t_R			285		
Turn-On Delay	t_{DON}	V_{INx} = 3.3V, R_{Lx} = 500Ω, C_{Lx} = 0.1μF		480		μs
V_{OUTx} Rise Time	t_R			280		
Turn-Off Delay	t_{DOFF}	V_{INx} = 3.3V, R_{Lx} = 150Ω, C_{Lx} = 0.1μF		0.5		μs
V_{OUTx} Fall Time	t_F			6.5		
Turn-Off Delay	t_{DOFF}	V_{INx} = 3.3V, R_{Lx} = 500Ω, C_{Lx} = 0.1μF		0.6		μs
V_{OUTx} Fall Time	t_F			7.5		

TIMING DIAGRAM

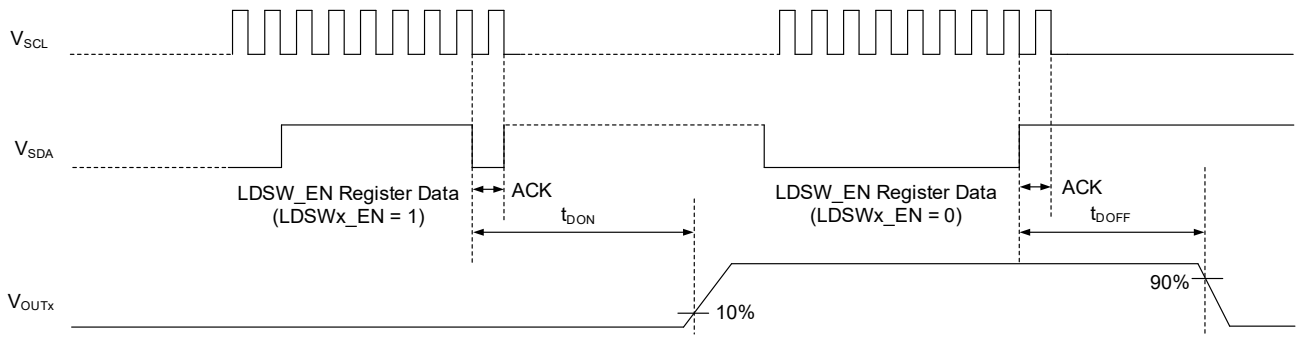


Figure 2. Timing Definition (LDSW_EN Register Control V_{OUTx} When EN is Active)

I²C MODE TIMING

(T_J = -40℃ to +85℃, V_{SYS} = 1.5V to 5.5V, unless otherwise noted.)

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}			400	kHz
Bus Free Time between Stop and Start Conditions	t_{BUF}	1.3			μs
Hold Time (Repeated) Start Condition	t_{HD_STA}	0.6			μs
Low Period of SCL Clock	t_{LOW}	1.3			μs
High Period of SCL Clock	t_{HIGH}	0.6			μs
Setup Time for Restart Condition	t_{SU_STA}	0.6			μs
Data Hold Time	t_{HD_DAT}			1	μs
Data Setup Time	t_{SU_DAT}	100			ns
Data Hold Time 2	t_{HD_R}	$20 + 0.1C_b$ (1)		500	ns
	t_{HD_F}	$20 + 0.1C_b$ (1)		500	ns
Setup Time for Stop Condition	t_{SU_STO}	0.6			μs

NOTE: 1. C_b is the total capacitance of one bus in pF.

I²C MODE TIMING DIAGRAM

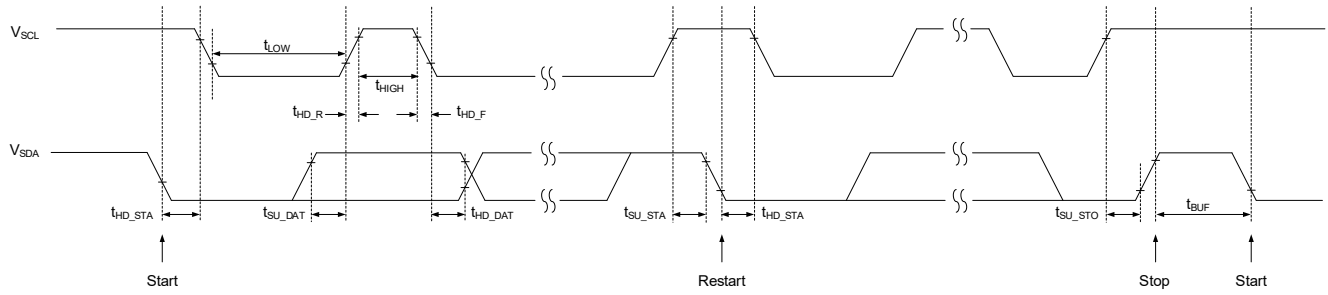
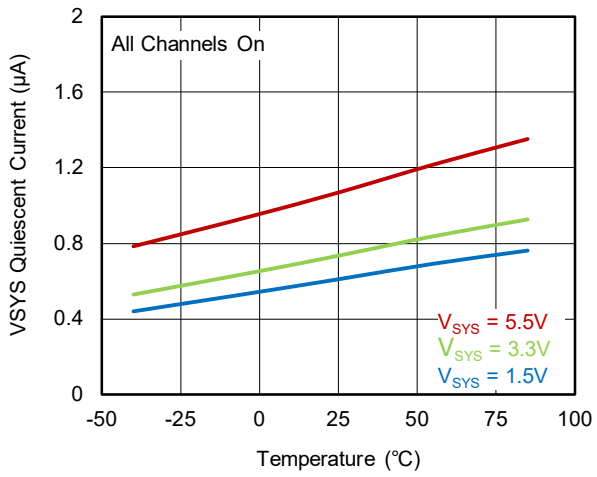


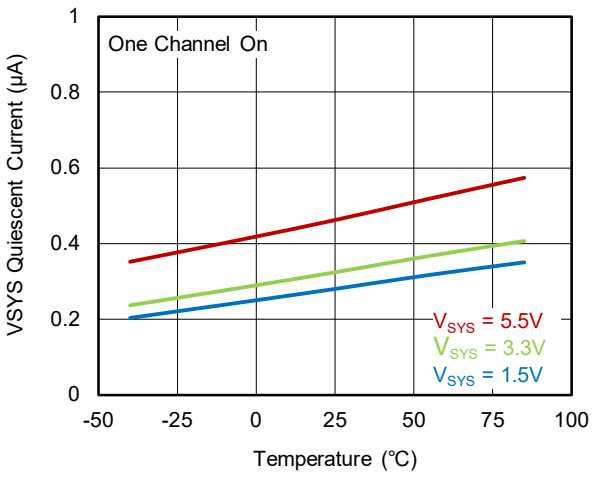
Figure 3. I²C Mode Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

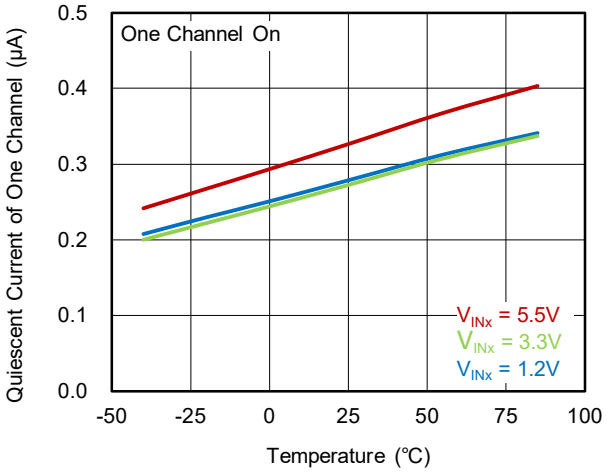
VSYS Quiescent Current vs. Temperature



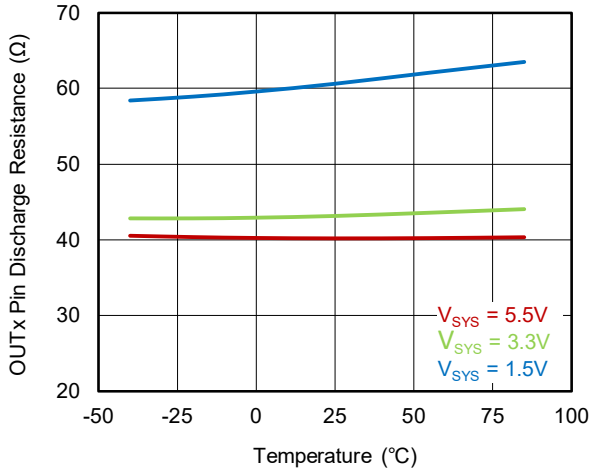
VSYS Quiescent Current vs. Temperature



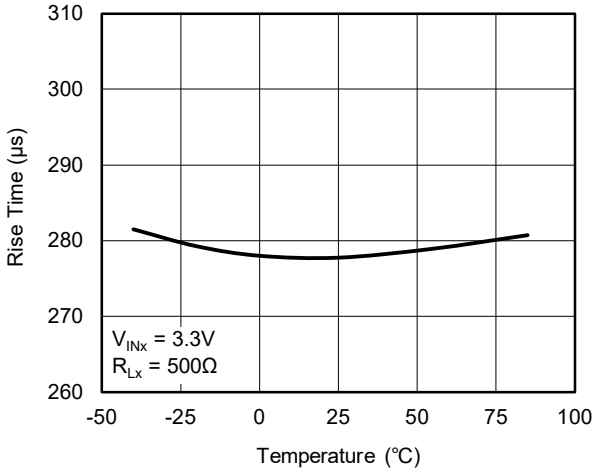
Quiescent Current of One Channel vs. Temperature



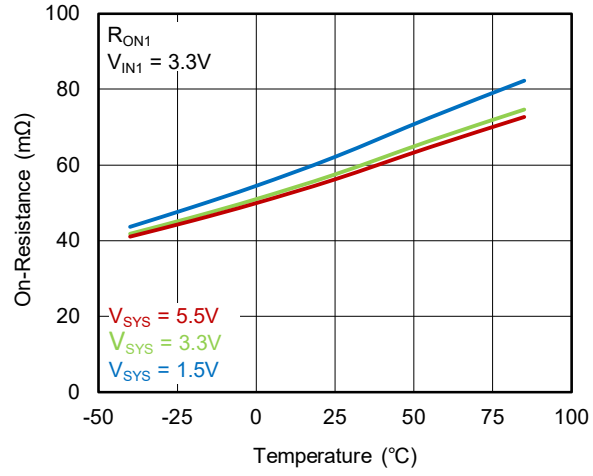
OUTx Pin Discharge Resistance vs. Temperature



Rise Time vs. Temperature



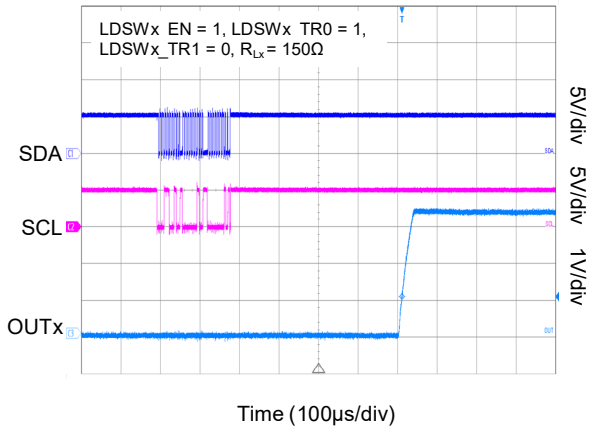
On-Resistance vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

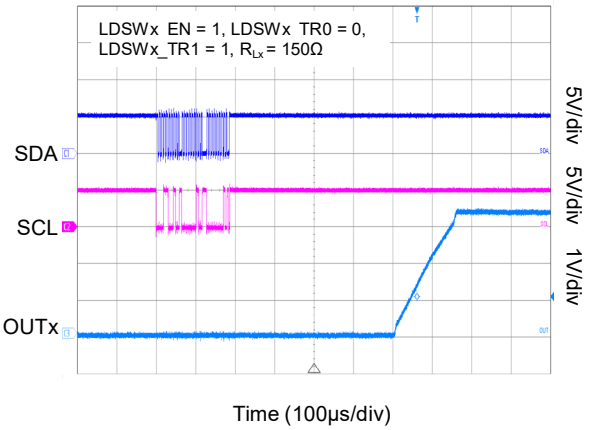
T_J = +25℃, V_{INx} = 3.3V, V_{SYS} = 5V and C_{Lx} = 100nF, unless otherwise noted.

LDSWx On Response



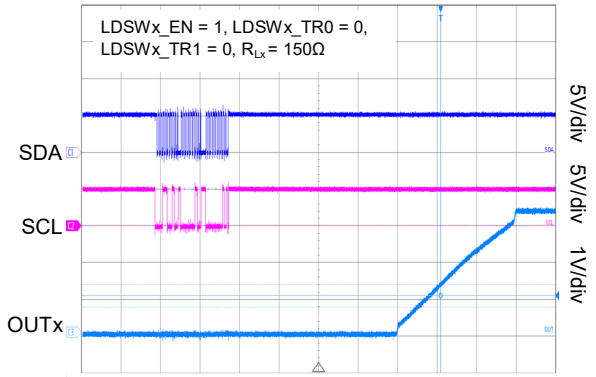
Time (100μs/div)

LDSWx On Response



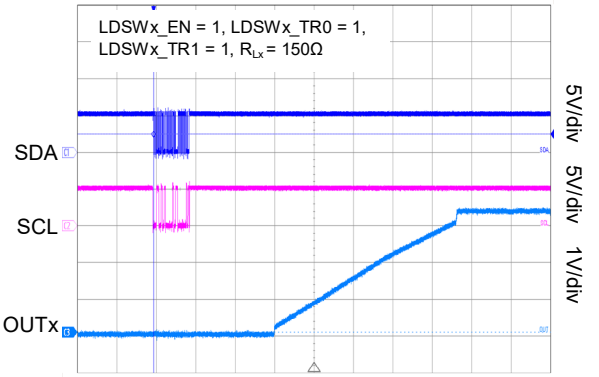
Time (100μs/div)

LDSWx On Response



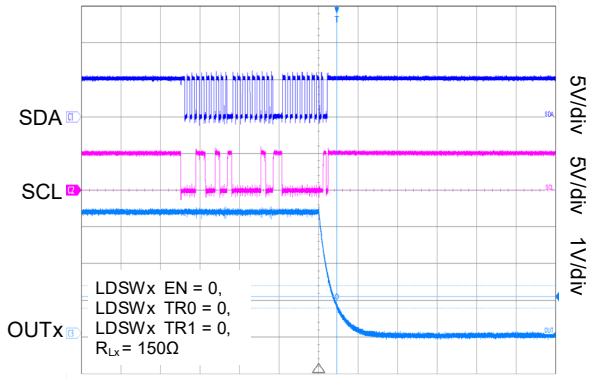
Time (100μs/div)

LDSWx On Response



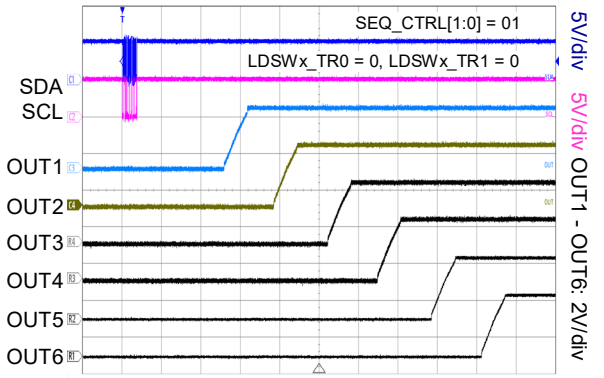
Time (200μs/div)

LDSWx Off Response



Time (50μs/div)

LDSWx Sequence On Response

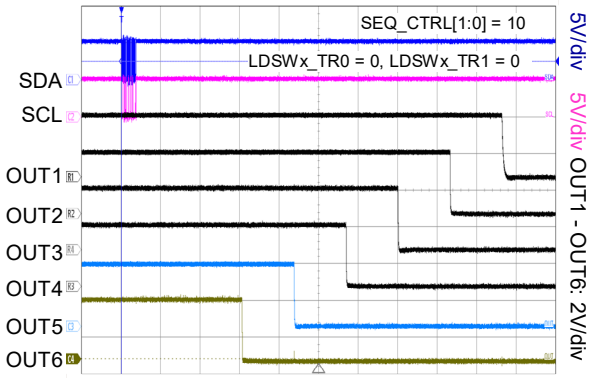


Time (500μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

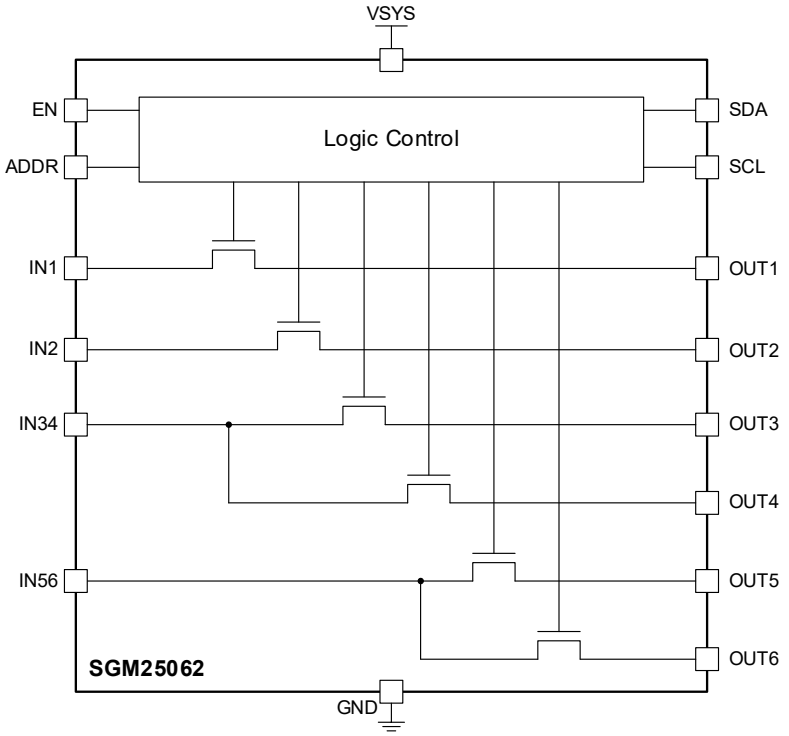
T_J = +25℃, V_{INx} = 3.3V, V_{SYS} = 5V and C_{Lx} = 100nF, unless otherwise noted.

LDSWx Sequence Off Response



Time (500μs/div)

FUNCTIONAL BLOCK DIAGRAM



NOTE: Each OUTx port has quick output discharge (QOD) function which can be enabled by I²C command.

Figure 4. Block Diagram

DETAILED DESCRIPTION

The SGM25062 is a small size, ultra-low on-resistance N-MOSFET, 6-channel load switch which operates from 1.2V to 5.5V single supply. It can support a continuous load current up to 2A per channel. Each channel load switch is controlled by programming. Through the I²C interface, the register can be set by the command which controls the on/off, QOD, rise time and power-up sequence of per channel and slot period.

On/Off Control

Turn-on and off of each channel can be controlled by an I²C register. There are two ways to set and control the LDSWx by the I²C register when the EN control pin is active at high level. The setting of registers LDSWx_SEQ[2:0] (x = 1 to 6) is as follows.

- Setting LDSWx_SEQ[2:0] = 000 in LDSW12_SEQ (0x05) or LDSW34_SEQ (0x06) or LDSW56_SEQ (0x07), and then set the bit LDSWx_EN = 1 in the 0x02 register to enable the corresponding channel respectively.
- Setting LDSWx_SEQ[2:0] > 000 in LDSW12_SEQ (0x05) or LDSW34_SEQ (0x06) or LDSW56_SEQ (0x07) registers and then set SEQ_CTRL[1:0] = 01 in SEQ_CTR register to enable the power-up respectively.

DETAILED DESCRIPTION (continued)

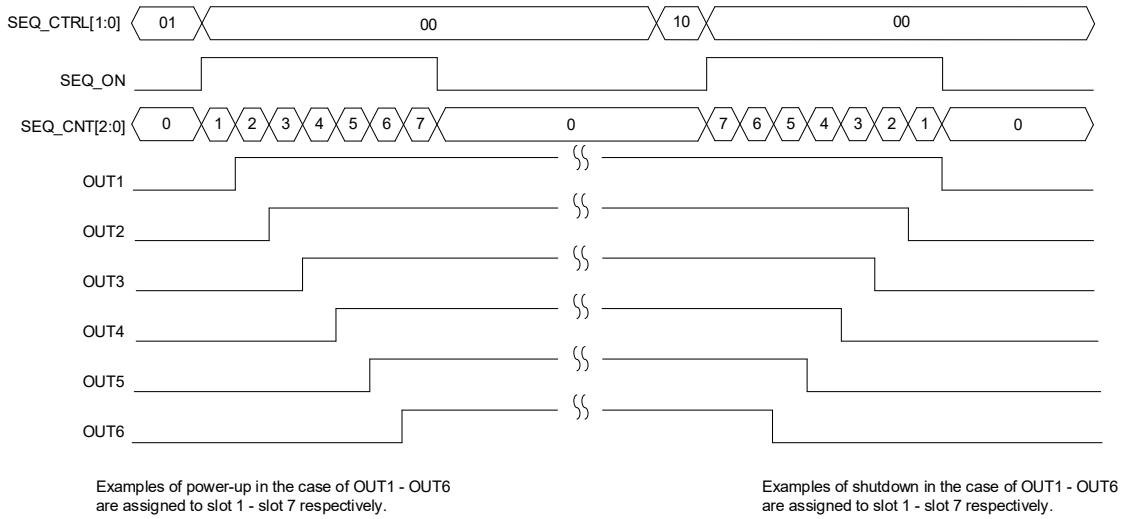
Sequence Control

Automatic power-up/power-down sequence control can be accomplished by register LDSWx_SEQ. The SGM25062 has 7 slots to which each channel can be assigned. They are set by SEQ_CTRL[1:0].

- When setting SEQ_CTRL[1:0] = 01, assigned the slots start power-up sequentially as the slot number from 0 (000) to 7 (111) while internal counter SEQ_CNT[2:0] starts to count the slot number of SEQ at this moment.
- When setting SEQ_CTRL[1:0] = 10, these channels assigned the slots start power-down as the slot number in reverse order from 7 (111) to 0 (000) while SEQ_CNT[2:0] decrements the slot number.

The SEQ_CNT[2:0] matches the slot number. When SEQ_CNT[2:0] = 000, indicates that sequencing has been completed or has not yet begun.

When SEQ_ON = 1, it indicates that the sequencing is in progress and is between the start position of slot 1 and the end position of slot 7. When SEQ_ON = 0, sequencing has completed or not started.



EN Pin

EN is the device enable control pin. High level is active. The default is pulled down to GND through a resistor of about 17MΩ. When the EN is driven high, the device is enabled and I^2C is active. When the EN is driven low, the device is disabled and drawn very little current. In this shutdown state, all the registers will be reset to their default values, and I^2C is invalid, so it cannot be written or read.

ADDR Pin

ADDR is the I^2C address set pin. It can be connected to GND or V_{SYS}. When ADDR is connected to GND, the address is 0011000. When ADDR is connected to V_{SYS}, the address is 0011001.

Input Capacitor

Turning on the N-MOSFET to charge the load capacitor will generate inrush current, which may lead to the decrease of V_{IN}. In order to prevent the drop, it is recommended to place a 1μF ceramic capacitor between the INx and GND pins. However, higher capacitance values could further reduce the voltage drop. Therefore, higher C_{INx} can further reduce the voltage drop in high current applications.

DETAILED DESCRIPTION (continued)

Output Capacitor

It is recommended that the output capacitance (C_{Lx}) between OUTx and GND should be at least 0.1μF. The capacitor should be placed near to the device pins. The capacitor prevents the V_{OUTx} from falling below GND due to onboard parasitic inductance when the switch is turned off. When the device is turned on, V_{INx} will drop due to the C_{INx} charging for C_{Lx}. To improve the decrease of V_{INx}, C_{INx} is usually larger than C_{Lx}.

V_{SYS} Power Supply

V_{SYS} is the power supply to the inner circuit, including control logic, I²C, quick output discharge and charge pump. The support voltage range is from 1.5V to 5.5V. It is recommended to use ceramic capacitors of 1μF or larger.

Quick Output Discharge (QOD)

The QOD feature is available for each channel. The device has a QOD circuit which is not activated to discharge by default. When the output is shutdown, the resistor will be connected the OUTx and GND pins to discharge the output capacitor quickly and reduce the output pin voltage in a very short time.

Setting LDSW_DIS related bits in 0x03 register can enable or disable QOD function. The default is enabled. QOD function can avoid timing disorder during fast on-off test.

Reverse Current Blocking Function

SGM25062 has a true reverse current blocking (RCB) function that prevents unwanted reverse current flowing from OUTx to INx during both on/off states. The RCB function can be controlled by LDSWx_RCB register.

LDSWx State	LDSWx_RCB	RCB Function
Off	0	Y
Off	1	Y
On	0	N
On	1	Y

I²C Data Communication

Bus Interface

I²C bus is 2 wire serial communication interface which is composed of SDA and SCL. SDA is the data line. SCL is the clock line. Both the SDA and SCL pins are open-drain which need to be pulled up through resistor. The micro-controller or DSP which generates the SCL pulses is usually used as a master device. SGM25062 is usually a slave device.

START and STOP Conditions

START condition is that SCL is high and a high to low transition on the SDA is generated by master. Similarly, a STOP is defined when SCL is high and SDA goes from low to high. START and STOP are always generated by a master. After a START and before a STOP the bus is considered busy.

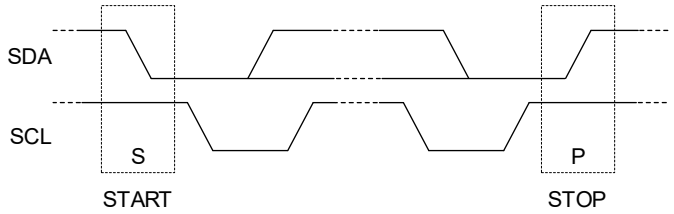


Figure 5. I²C Bus in START and STOP Conditions

DETAILED DESCRIPTION (continued)

Data Bit Transmission and Validity

The data bit (high or low) must remain stable on the SDA line during the high period of the clock. Only when the clock (SCL) is at a low level, the state of SDA will change. One clock pulse transmits one bit data. Bit transfer in I²C is shown in Figure 6.

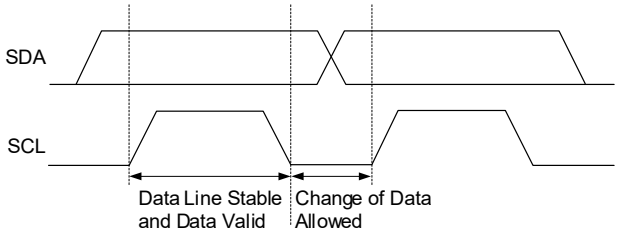


Figure 6. I²C Bus Bit Transfer

Byte Format

Data is transmitted in 8-bit packets (one byte at a time). There is no limit on the number of bytes in a transaction. In each data packet, 8 bits are sent in sequence, and the most significant bit (MSB) takes priority. The 8 data bits must be followed by an acknowledge (or not acknowledge) bit. This bit informs the transmitter whether the receiver is ready to proceed with the next byte or not. Figure 7 shows the byte transfer process with I²C interface.

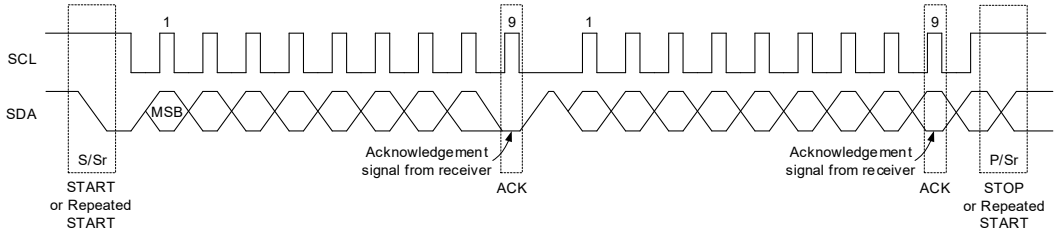


Figure 7. Byte Transfer Process

Acknowledge (ACK) and Not-Acknowledge (NCK)

The acknowledge takes place following every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master. The transmitter releases the SDA line during the acknowledge clock pulse, so the receiver can pull the SDA line low and it remains stable low during the high period of this clock pulse. When SDA remains high during the 9th clock pulse, this is the not-acknowledge signal. Then the master can generate a STOP to abort the transmission or a repeated START to start a new transmission.

Slave Address and Data Direction Bit

A slave address is sent after the start. This address is 7 bits long followed by the 8th bit as a data direction bit (bit R/W). A zero indicates a transmission (Write) and a one indicates a data request (Read).

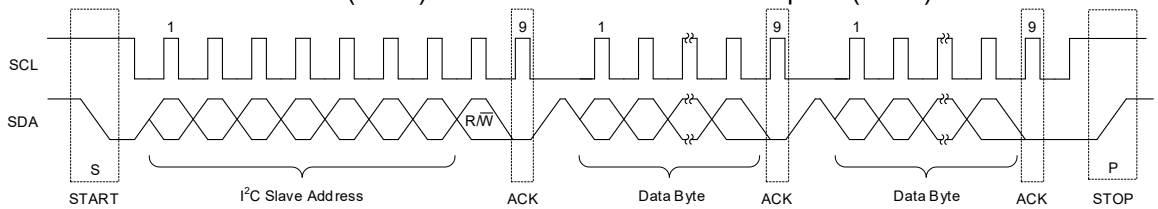


Figure 8. Data Transfer Transaction

DETAILED DESCRIPTION (continued)

Single-Read and Single-Write

Single-Write: If the master wants to write in the register, the third byte can be written directly as shown in Figure 9 for a single write data transfer. After receiving the ACK, master may issue a STOP condition to end the transaction or send the next register data, which will be written to the next address in a slave as multi-write. A STOP is needed after sending the last data.

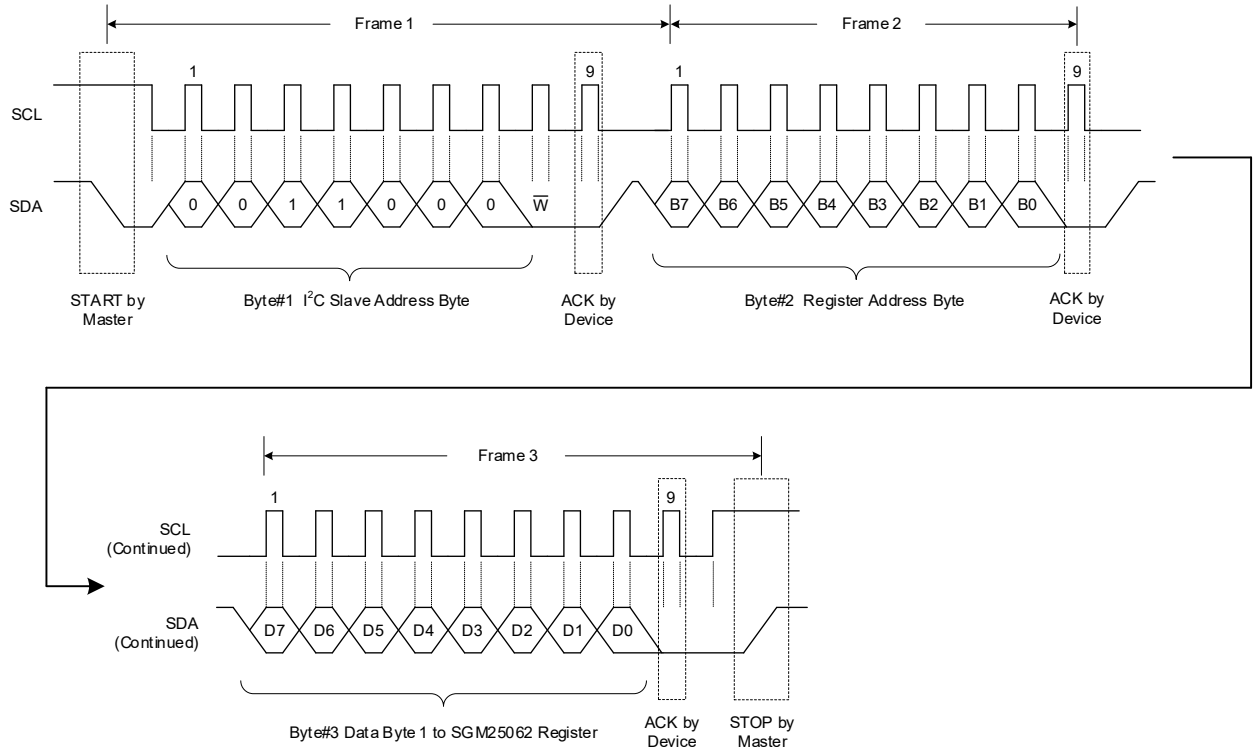


Figure 9. I²C Single-Writing Command Register

DETAILED DESCRIPTION (continued)

Single-Read: If the master wants to read a single register (Figure 10), it sends a new START condition along with device address with R/W bit = 1. After ACK is receiving, master reads the SDA line to receive the content of the register. Master replies with NCK to inform slave that no more data is needed (single read) or it can send an ACK to request for sending the next register content (multi-read). This can continue until an NCK is sent by master. In any case, the master must send a stop loss signal to end the transaction.

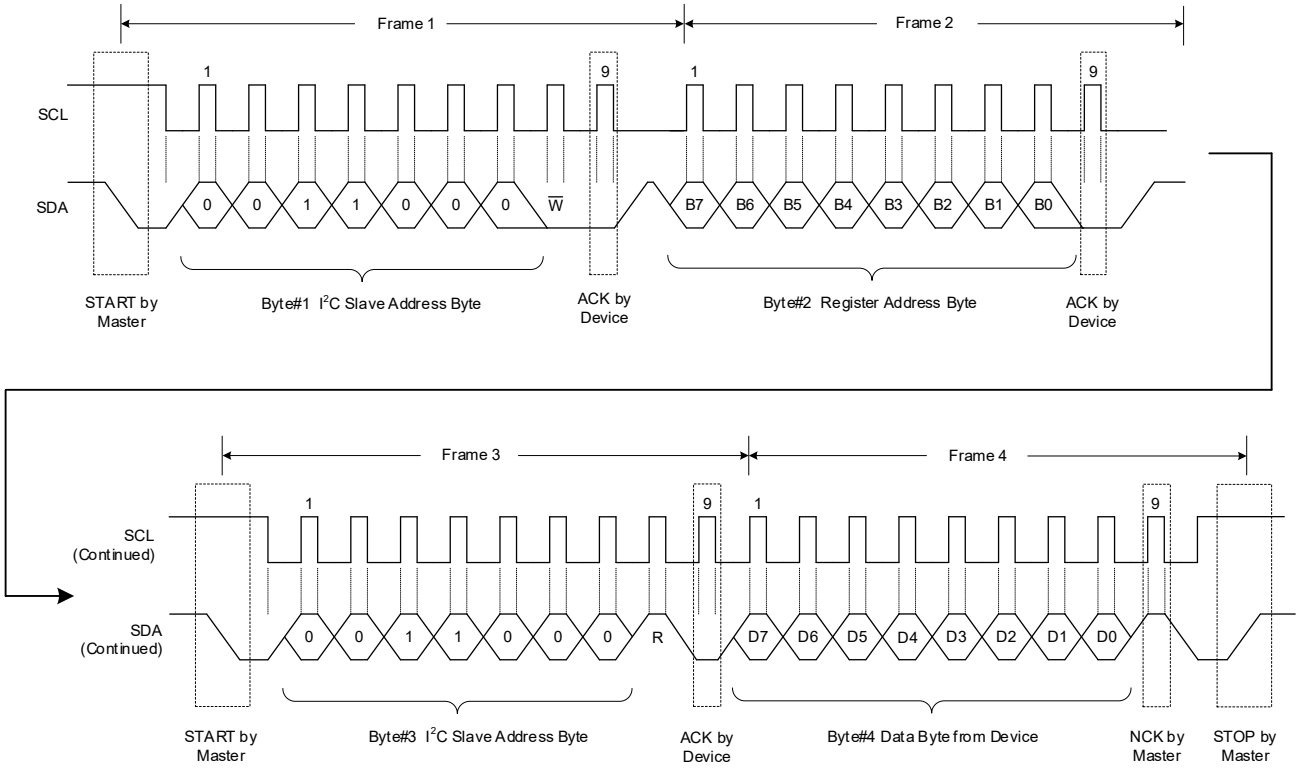


Figure 10. I²C Single-Reading Command Register

DETAILED DESCRIPTION (continued)

Multi-Write and Multi-Read

SGM25062 supports multi-write and multi-read.

Multi-Write: In the multi-write transaction, firstly write the chip address and command start address. Then the register data is sent and written to the command register addresses by the master byte by byte until a STOP occurs or a restart. In the multi-write, every new data byte sent by master is written to the next register of the device.

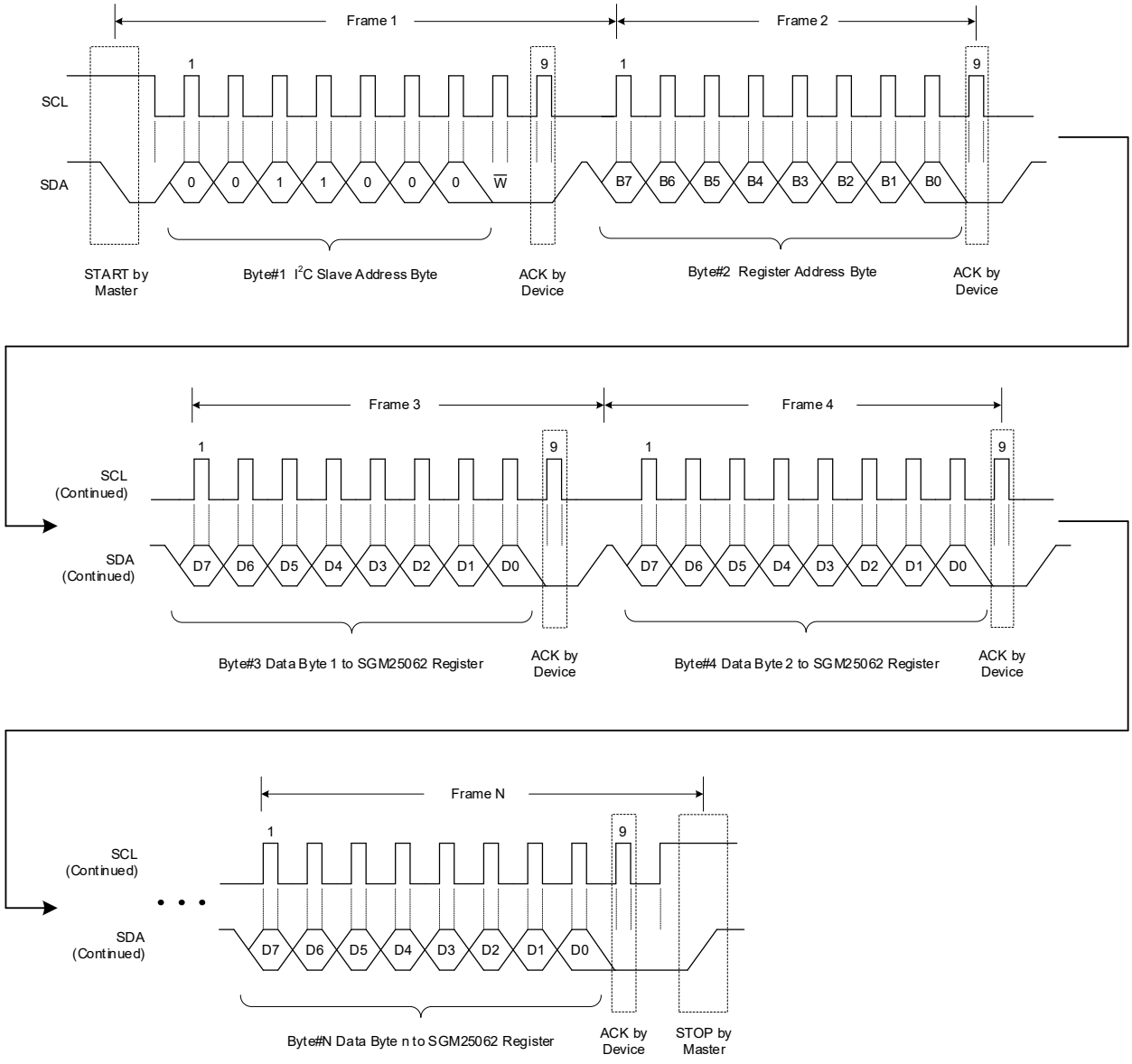


Figure 11. I²C Writing Command Register (Continuous)

DETAILED DESCRIPTION (continued)

Multi-Read: In the multi-read transaction, firstly write the chip address and command start address and then read the chip address. After that, the register dates are sent and read from the command start register address byte by byte until an NCK occurs following a STOP or a restart. In the multi-read, an ACK is sent to request for sending the next register content.

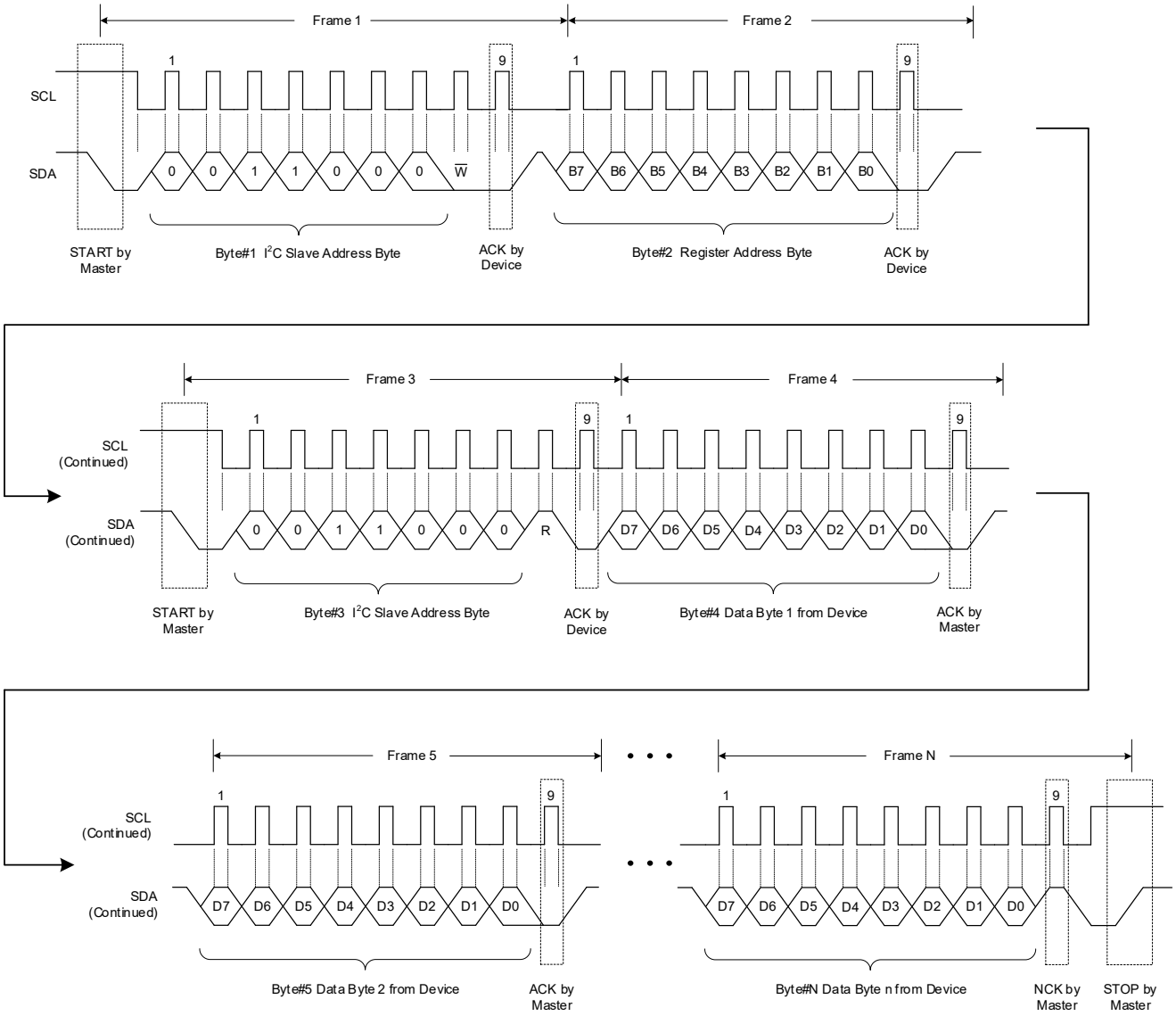


Figure 12. I²C Reading Command Register (Continuous)

NOTE: The slave address in above transmission frame is 0011000 (ADDR connect to GND) as an example.

REGISTER MAPS

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

I²C 7-Bit Slave Address of SGM25062: 0011000 (ADDR connect to GND) or 0011001 (ADDR connect to V_{SYS}).

R/W: Read/Write bit(s)
R: Read only bit(s)
W/C: Write/Clear bit(s)

Register Map

ADDRESS	NAME	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	RESET
0x00	CHIPID	001100						CHIP_ID[1:0]		0x32
0x01	VERID	000000						VER_ID[1:0]		0x00
0x02	LDSW_EN	0	0	LDSW6_EN	LDSW5_EN	LDSW4_EN	LDSW3_EN	LDSW2_EN	LDSW1_EN	0x00
0x03	LDSW_DIS	0	0	LDSW6_DIS	LDSW5_DIS	LDSW4_DIS	LDSW3_DIS	LDSW2_DIS	LDSW1_DIS	0x3F
0x04	LDSW_TR0	0	0	LDSW6_TR0	LDSW5_TR0	LDSW4_TR0	LDSW3_TR0	LDSW2_TR0	LDSW1_TR0	0x00
0x05	LDSW12_SEQ	0	0	LDSW2_SEQ[2:0]			LDSW1_SEQ[2:0]			0x00
0x06	LDSW34_SEQ	0	0	LDSW4_SEQ[2:0]			LDSW3_SEQ[2:0]			0x00
0x07	LDSW56_SEQ	0	0	LDSW6_SEQ[2:0]			LDSW5_SEQ[2:0]			0x00
0x08	SEQ_CTR	SEQ_SPEED[1:0]		SEQ_CTRL[1:0]		SEQ_ON	SEQ_CNT[2:0]			0x00
0x09	LDSW_TR1	0	0	LDSW6_TR1	LDSW5_TR1	LDSW4_TR1	LDSW3_TR1	LDSW2_TR1	LDSW1_TR1	0x00
0x0A	LDSW_RCB	0	0	LDSW6_RCB	LDSW5_RCB	LDSW4_RCB	LDSW3_RCB	LDSW2_RCB	LDSW1_RCB	0x00
0x0B	LDSW_STA	0	0	LDSW6_STA	LDSW5_STA	LDSW4_STA	LDSW3_STA	LDSW2_STA	LDSW1_STA	0x00
0x69	SOFTRST_CTR	Write B0H to this register can reset all the registers to their default value								0x00

NOTE: Reserved keeps 0.

CHIPID

Register address: 0x00
Reset = 0x32
CHIP_ID[1:0] indicates the device ID.

VERID

Register address: 0x01
Reset = 0x00
VER_ID[1:0] indicates the revision ID.

REGISTER MAPS (continued)

LDSW_EN

Register address: 0x02; R or R/W
Reset = 0x00

Table 1. LDSW_EN Register Details

BITS	BIT NAME	DESCRIPTION	DEFAULT	TYPE
D[7]	RESERVED	Reserved	0	R
D[6]	RESERVED	Reserved	0	R
D[5]	LDSW6_EN	LDSW6 Enable Control: 0 = Disable 1 = Enable	0	R/W
D[4]	LDSW5_EN	LDSW5 Enable Control: 0 = Disable 1 = Enable	0	R/W
D[3]	LDSW4_EN	LDSW4 Enable Control: 0 = Disable 1 = Enable	0	R/W
D[2]	LDSW3_EN	LDSW3 Enable Control: 0 = Disable 1 = Enable	0	R/W
D[1]	LDSW2_EN	LDSW2 Enable Control: 0 = Disable 1 = Enable	0	R/W
D[0]	LDSW1_EN	LDSW1 Enable Control: 0 = Disable 1 = Enable	0	R/W

LDSW_DIS

Register address: 0x03; R or R/W
Reset = 0x3F

Table 2. LDSW_DIS Register Details

BITS	NAME	DESCRIPTION	DEFAULT	TYPE
D[7]	RESERVED	Reversed	0	R
D[6]	RESERVED	Reversed	0	R
D[5]	LDSW6_DIS	LDSW6 Discharge Enabled/Disabled Control: 0 = Disable. QOD6 will not discharge the V_{OUT6} when LDSW6 is disabled. 1 = Enable. QOD6 will discharge the V_{OUT6} when LDSW6 is disabled.	1	R/W
D[4]	LDSW5_DIS	LDSW5 Discharge Enabled/Disabled Control: 0 = Disable. QOD5 will not discharge the V_{OUT5} when LDSW5 is disabled. 1 = Enable. QOD5 will discharge the V_{OUT5} when LDSW5 is disabled.	1	R/W
D[3]	LDSW4_DIS	LDSW4 Discharge Enabled/Disabled Control: 0 = Disable. QOD4 will not discharge the V_{OUT4} when LDSW4 is disabled. 1 = Enable. QOD4 will discharge the V_{OUT4} when LDSW4 is disabled.	1	R/W
D[2]	LDSW3_DIS	LDSW3 Discharge Enabled/Disabled Control: 0 = Disable. QOD3 will not discharge the V_{OUT3} when LDSW3 is disabled. 1 = Enable. QOD3 will discharge the V_{OUT3} when LDSW3 is disabled.	1	R/W
D[1]	LDSW2_DIS	LDSW2 Discharge Enabled/Disabled Control: 0 = Disable. QOD2 will not discharge the V_{OUT2} when LDSW2 is disabled. 1 = Enable. QOD2 will discharge the V_{OUT2} when LDSW2 is disabled.	1	R/W
D[0]	LDSW1_DIS	LDSW1 Discharge Enabled/Disabled Control : 0 = Disable. QOD1 will not discharge the V_{OUT1} when LDSW1 is disabled. 1 = Enable. QOD1 will discharge the V_{OUT1} when LDSW1 is disabled.	1	R/W

REGISTER MAPS (continued)

LDSW_TR0/1

Register address: 0x04/09; R or R/W
Reset = 0x00

Table 3. LDSW_TR0/1 Register Details (V_{INx} = 3.3V, R_{Lx} = 150Ω, C_{Lx} = 0.1μF)

BITS	NAME	DESCRIPTION	DEFAULT	TYPE
D[7]	RESERVED	Reversed	0	R
D[6]	RESERVED	Reversed	0	R
D[5]	LDSW6_TR1 LDSW6_TR0	LDSW6 rise time (V_{OUT} from 10% to 90%): 00 = 285μs 01 = 29μs 10 = 140μs 11 = 820μs	0	R/W
D[4]	LDSW5_TR1 LDSW5_TR0	LDSW5 rise time (V_{OUT} from 10% to 90%): 00 = 285μs 01 = 29μs 10 = 140μs 11 = 820μs	0	R/W
D[3]	LDSW4_TR1 LDSW4_TR0	LDSW4 rise time (V_{OUT} from 10% to 90%): 00 = 285μs 01 = 29μs 10 = 140μs 11 = 820μs	0	R/W
D[2]	LDSW3_TR1 LDSW3_TR0	LDSW3 rise time (V_{OUT} from 10% to 90%): 00 = 285μs 01 = 29μs 10 = 140μs 11 = 820μs	0	R/W
D[1]	LDSW2_TR1 LDSW2_TR0	LDSW2 rise time (V_{OUT} from 10% to 90%): 00 = 285μs 01 = 29μs 10 = 140μs 11 = 820μs	0	R/W
D[0]	LDSW1_TR1 LDSW1_TR0	LDSW1 rise time (V_{OUT} from 10% to 90%): 00 = 285μs 01 = 29μs 10 = 140μs 11 = 820μs	0	R/W

LDSW12_SEQ

Register address: 0x05; R or R/W
Reset = 0x00

Table 4. LDSW12_SEQ Register Details

BITS	NAME	DESCRIPTION	DEFAULT	TYPE
D[7:6]	RESERVED	Reserved	00	R
D[5:3]	LDSW2_SEQ [2:0]	OUT2 000 = Controlled by LDSW2_EN register 001 = Slot 1 010 = Slot 2 011 = Slot 3 100 = Slot 4 101 = Slot 5 110 = Slot 6 111 = Slot 7	000	R/W
D[2:0]	LDSW1_SEQ[2:0]	OUT1 000 = Controlled by LDSW1_EN register 001 = Slot 1 010 = Slot 2 011 = Slot 3 100 = Slot 4 101 = Slot 5 110 = Slot 6 111 = Slot 7	000	R/W

REGISTER MAPS (continued)

LDSW34_SEQ

Register address: 0x06; R or R/W
Reset = 0x00

Table 5. LDSW34_SEQ Register Details

BITS	NAME	DESCRIPTION	DEFAULT	TYPE
D[7:6]	RESERVED	Reserved	00	R
D[5:3]	LDSW4_SEQ[2:0]	OUT4 000 = Controlled by LDSW4_EN register 001 = Slot 1 010 = Slot 2 011 = Slot 3 100 = Slot 4 101 = Slot 5 110 = Slot 6 111 = Slot 7	000	R/W
D[2:0]	LDSW3_SEQ[2:0]	OUT3 000 = Controlled by LDSW3_EN register 001 = Slot 1 010 = Slot 2 011 = Slot 3 100 = Slot 4 101 = Slot 5 110 = Slot 6 111 = Slot 7	000	R/W

LDSW56_SEQ

Register address: 0x07; R or R/W
Reset = 0x00

Table 6. LDSW56_SEQ Register Details

BITS	NAME	DESCRIPTION	DEFAULT	TYPE
D[7:6]	RESERVED	Reserved	00	R
D[5:3]	LDSW6_SEQ[2:0]	OUT6 000 = Controlled by LDSW6_EN register 001 = Slot 1 010 = Slot 2 011 = Slot 3 100 = Slot 4 101 = Slot 5 110 = Slot 6 111 = Slot 7	000	R/W
D[2:0]	LDSW5_SEQ[2:0]	OUT5 000 = Controlled by LDSW5_EN register 001 = Slot 1 010 = Slot 2 011 = Slot 3 100 = Slot 4 101 = Slot 5 110 = Slot 6 111 = Slot 7	000	R/W

REGISTER MAPS (continued)

SEQ_CTR

Register Address: 0x08; R, R/W or W/C
Reset = 0x00

Table 7. SEQ_CTR Register Details

BITS	NAME	DESCRIPTION	DEFAULT	TYPE
D[7:6]	SEQ_SPEED[1:0]	Slot period: 00 = 0.7ms 01 = 1.3ms 10 = 1.9ms 11 = 2.5ms	00	R/W
D[5:4]	SEQ_CTRL[1:0]	Enables power-up or shutdown of SEQ: 00 = Default 01 = Starts a power-up sequence. LDSWx start up as the slot number from slot 1 to slot 7 set in LDSWx_SEQ Register. 10 = Starts a shutdown sequence. LDSWx shutdown as the slot number from slot 7 to slot 1 set in LDSWx_SEQ Register. 11 = Bit configuration is ignored Note: When written, bits are always immediately cleared and always read back 00.	00	W/C
D[3]	SEQ_ON	Activation signal of SEQ: 0 = The sequencing is not in process 1 = The sequencing of LDSWx is in process.	0	R
D[2:0]	SEQ_CNT[2:0]	Slot number of SEQ at the moment: 000 = Sequencing has completed or not started. 001 = In slot 1 when register is read. 010 = In slot 2 when register is read. 011 = In slot 3 when register is read. 100 = In slot 4 when register is read. 101 = In slot 5 when register is read. 110 = In slot 6 when register is read. 111 = In slot 7 when register is read.	000	R

LDSW_RCB

Register address: 0x0A; R or R/W
Reset = 0x00

Table 8. LDSW_RCB Register Details

BITS	NAME	DESCRIPTION	DEFAULT	TYPE
D[7]	RESERVED	Reserved	0	R
D[6]	RESERVED	Reserved	0	R
D[5]	LDSW6_RCB	LDSW6 RCB function: 0 = Disable 1 = Enable	0	R/W
D[4]	LDSW5_RCB	LDSW5 RCB function: 0 = Disable 1 = Enable	0	R/W
D[3]	LDSW4_RCB	LDSW4 RCB function: 0 = Disable 1 = Enable	0	R/W
D[2]	LDSW3_RCB	LDSW3 RCB function: 0 = Disable 1 = Enable	0	R/W
D[1]	LDSW2_RCB	LDSW2 RCB function: 0 = Disable 1 = Enable	0	R/W
D[0]	LDSW1_RCB	LDSW1 RCB function: 0 = Disable 1 = Enable	0	R/W

REGISTER MAPS (continued)

LDSW_STA

Register address: 0x0B; R
Reset = 0x00

Table 9. LDSW_STA Register Details

BITS	NAME	DESCRIPTION	DEFAULT	TYPE
D[7]	RESERVED	Reserved	0	R
D[6]	RESERVED	Reserved	0	R
D[5]	LDSW6_STA	LDSW6 status: 0 = turn-off status 1 = turn-on status	0	R
D[4]	LDSW5_STA	LDSW5 status: 0 = turn-off status 1 = turn-on status	0	R
D[3]	LDSW4_STA	LDSW4 status: 0 = turn-off status 1 = turn-on status	0	R
D[2]	LDSW3_STA	LDSW3 status: 0 = turn-off status 1 = turn-on status	0	R
D[1]	LDSW2_STA	LDSW2 status: 0 = turn-off status 1 = turn-on status	0	R
D[0]	LDSW1_STA	LDSW1 status: 0 = turn-off status 1 = turn-on status	0	R

SOFTRST_CTR

Register Address: 0x69; R/W
Reset = 0x00

Table 10. SOFTRST_CTR Register Details

BITS	NAME	DESCRIPTION	DEFAULT	TYPE
D[7:0]	SOFTRST_CTR	Write B0H to this register will reset all the registers to default value, the read value always keep 00H.	00H	R/W

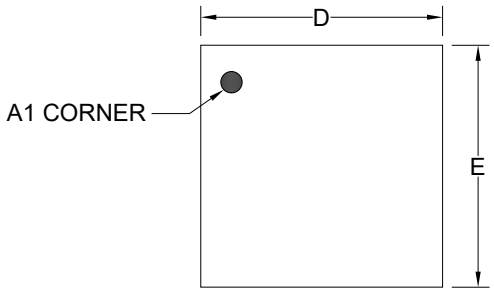
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

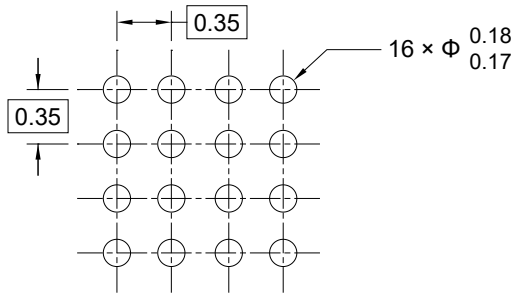
Changes from Original (DECEMBER 2022) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

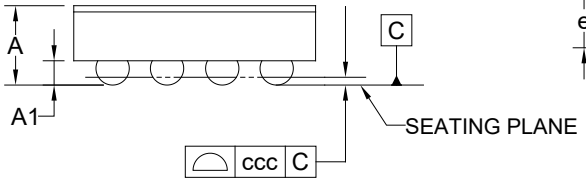
WLCSP-1.55×1.55-16B-A



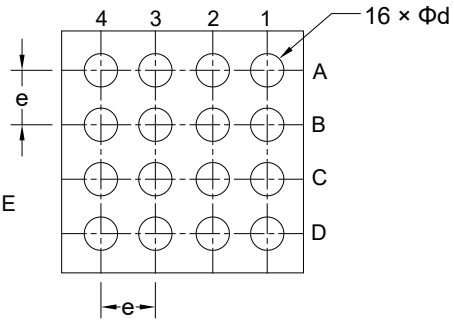
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



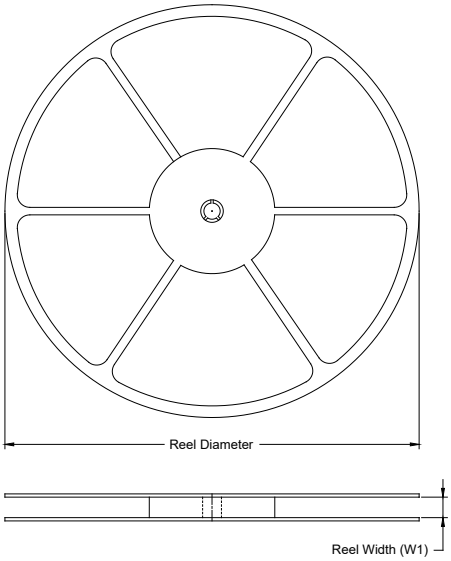
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	0.548
A1	0.136	-	0.176
D	1.520	-	1.580
E	1.520	-	1.580
d	0.184	-	0.244
e	0.350 BSC		
ccc	0.050		

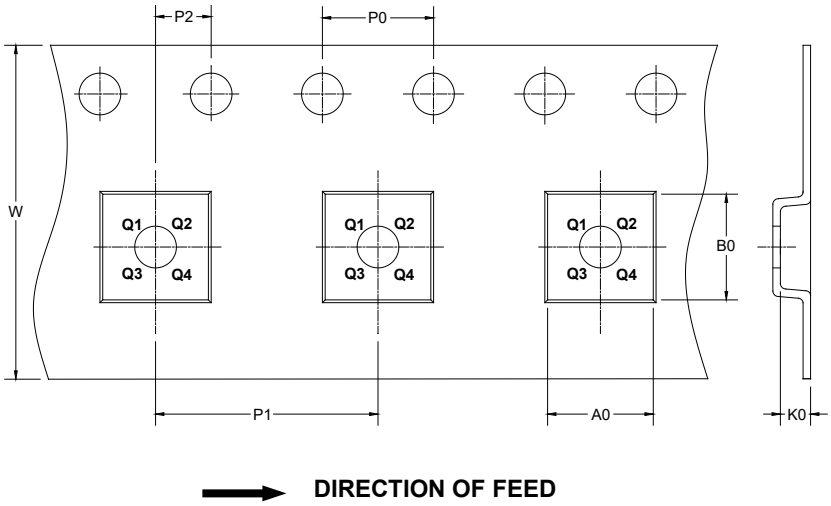
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



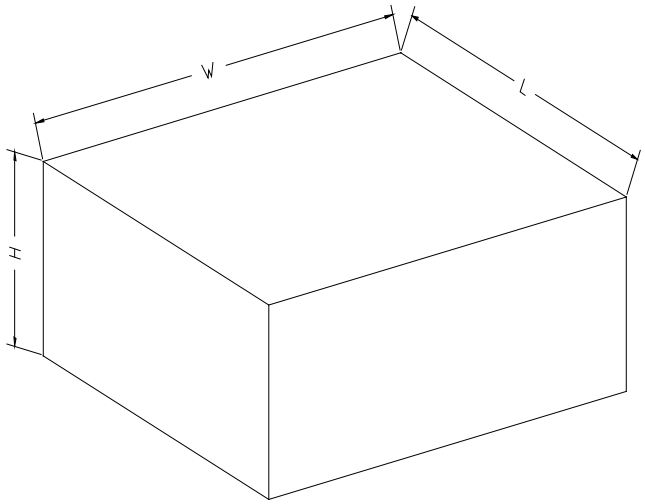
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-1.55×1.55-16B-A	7″	9.5	1.73	1.73	0.72	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002