

## Power MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V)	250	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	0.64
$Q_g$ (Max.) (nC)	14	
$Q_{gs}$ (nC)	2.7	
$Q_{gd}$ (nC)	7.8	
Configuration	Single	

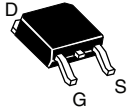
### FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Available in Tape and Reel
- Fast Switching
- Ease of Paralleling



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
Available

**DPAK  
(TO-252)**



N-Channel MOSFET

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V <sub>DS</sub>	250	V
Gate-Source Voltage			V <sub>GS</sub>	± 20	
Continuous Drain Current	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 25 °C	I <sub>D</sub>	4.5	A
		T <sub>C</sub> = 100 °C		3.0	
Pulsed Drain Current <sup>a</sup>			I <sub>DM</sub>	16	
Linear Derating Factor				0.33	W/°C
Linear Derating Factor (PCB Mount) <sup>e</sup>				0.020	
Single Pulse Avalanche Energy <sup>b</sup>			E <sub>AS</sub>	130	mJ
Repetitive Avalanche Current <sup>a</sup>			I <sub>AR</sub>	4.5	A
Repetitive Avalanche Energy <sup>a</sup>			E <sub>AR</sub>	5.2	mJ
Maximum Power Dissipation	T <sub>C</sub> = 25 °C		P <sub>D</sub>	45	W
Maximum Power Dissipation (PCB Mount) <sup>e</sup>	T <sub>A</sub> = 25 °C			2.5	
Peak Diode Recovery dV/dt <sup>c</sup>			dV/dt	4.8	V/ns
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature) <sup>d</sup>	for 10 s			260	

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$ ; starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 14\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 3.8\text{ A}$  (see fig. 12).
- $I_{SD} \leq 3.8\text{ A}$ ,  $di/dt \leq 90\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mount) <sup>a</sup>	$R_{thJA}$	-	50	°C/W
Maximum Junction-to-Ambient	$R_{thJA}$	-	110	
Maximum Junction-to-Case	$R_{thJC}$	-	3.0	

**Note**

a. When mounted on 1" square PCB (FR-4 or G-10 material).

**SPECIFICATIONS** ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		250	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}, I_D = 1\text{ mA}$		-	0.36	-	V/ $^\circ\text{C}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 250\text{ V}, V_{GS} = 0\text{ V}$		-	-	25	$\mu\text{A}$
		$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 2.3\text{ A}^b$	-	0.64	-	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 2.3\text{ A}^b$		1.5	-	-	S
Dynamic							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V},$ $V_{DS} = 25\text{ V},$ $f = 1.0\text{ MHz, see fig. 5}^c$		-	260	-	pF
Output Capacitance	$C_{oss}$			-	77	-	
Reverse Transfer Capacitance	$C_{rss}$			-	15	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 4.4\text{ A}, V_{DS} = 200\text{ V},$ see fig. 6 and 13 <sup>b, c</sup>	-	-	14	nC
Gate-Source Charge	$Q_{gs}$			-	-	2.7	
Gate-Drain Charge	$Q_{gd}$			-	-	7.8	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 125\text{ V}, I_D = 4.4\text{ A},$ $R_G = 18\text{ }\Omega, R_D = 28\text{ }\Omega,$ see fig. 10 <sup>b, c</sup>		-	7.0	-	ns
Rise Time	$t_r$			-	13	-	
Turn-Off Delay Time	$t_{d(off)}$			-	20	-	
Fall Time	$t_f$			-	12	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal Source Inductance	$L_S$			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode		-	-	3.8	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	15	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 3.8\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	1.8	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 4.4\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$		-	200	400	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	0.93	1.9	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
 b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

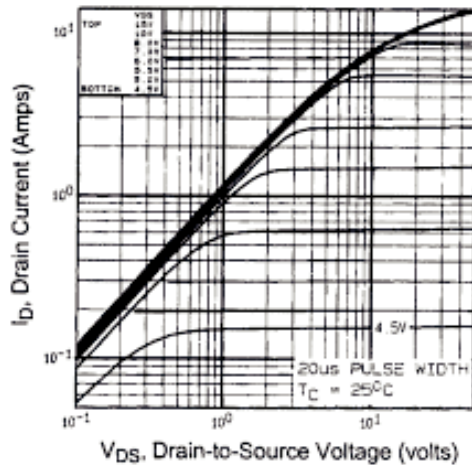
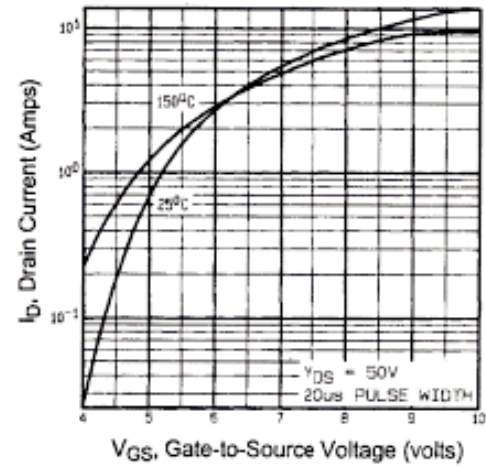
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

 Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^{\circ}\text{C}$ 


Fig. 3 - Typical Transfer Characteristics

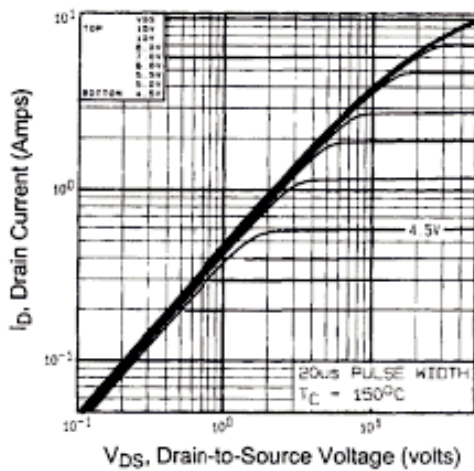
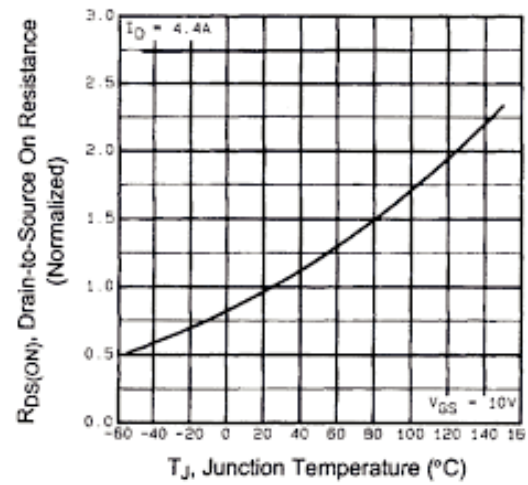

 Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ }^{\circ}\text{C}$ 


Fig. 4 - Normalized On-Resistance vs. Temperature

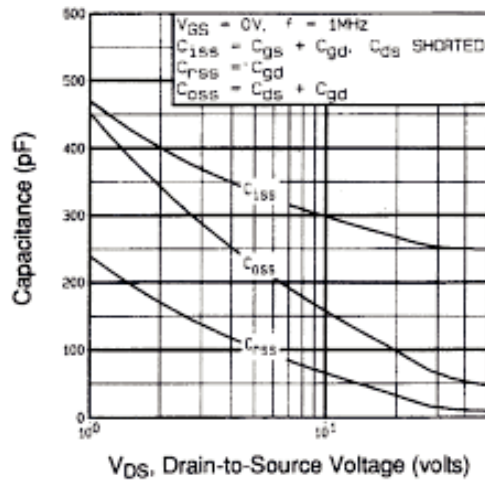


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

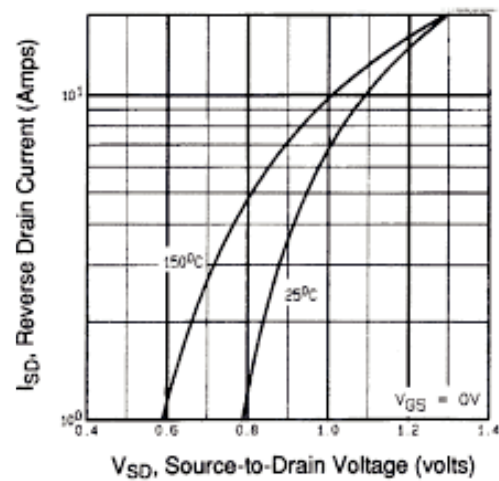


Fig. 7 - Typical Source-Drain Diode Forward Voltage

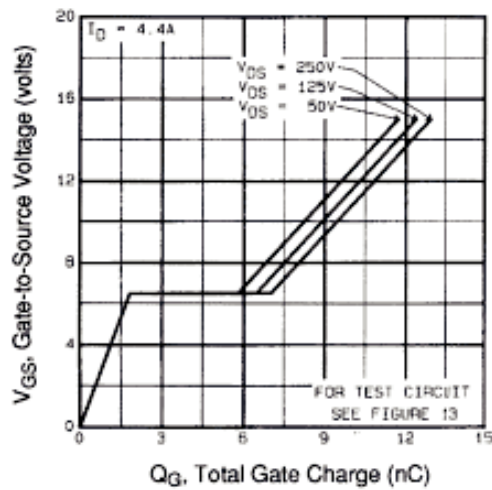


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

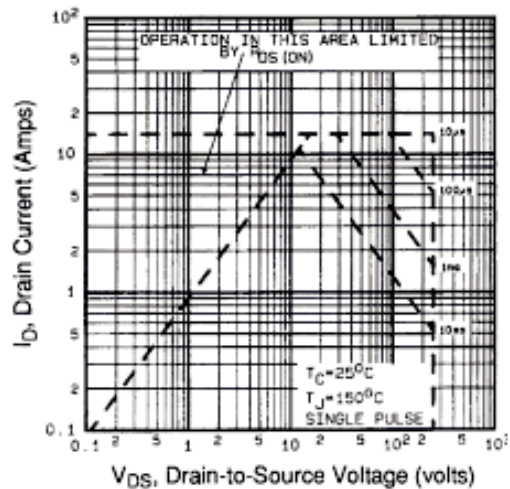


Fig. 8 - Maximum Safe Operating Area

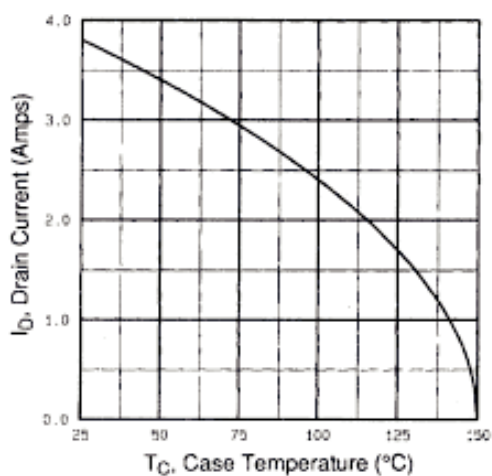


Fig. 9 - Maximum Drain Current vs. Case Temperature

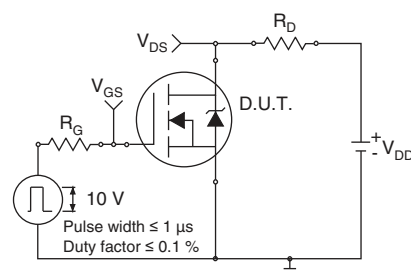


Fig. 10a - Switching Time Test Circuit

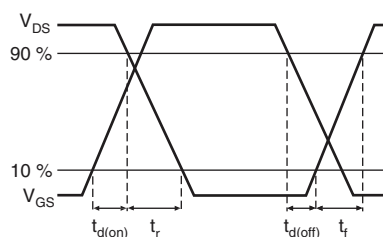


Fig. 10b - Switching Time Waveforms

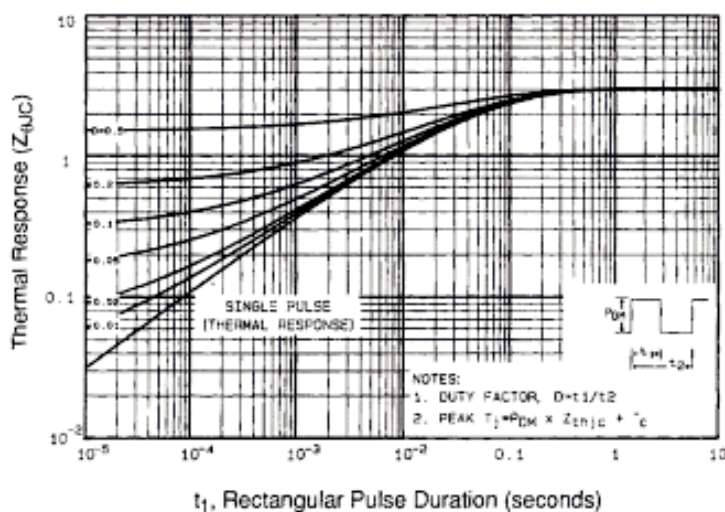


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

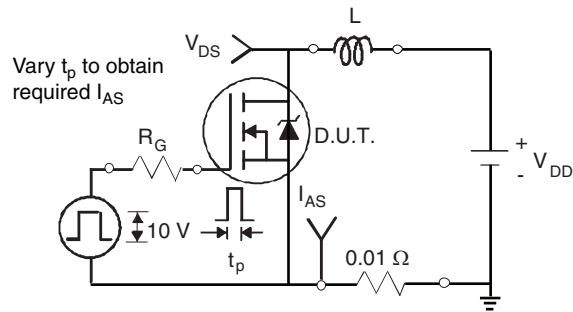


Fig. 12a - Unclamped Inductive Test Circuit

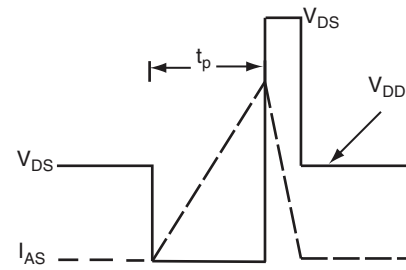


Fig. 12b - Unclamped Inductive Waveforms

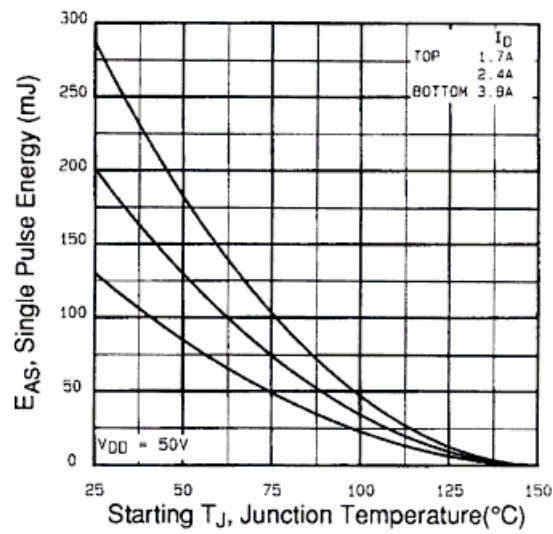


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

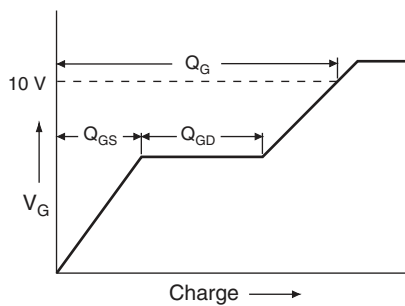


Fig. 13a - Basic Gate Charge Waveform

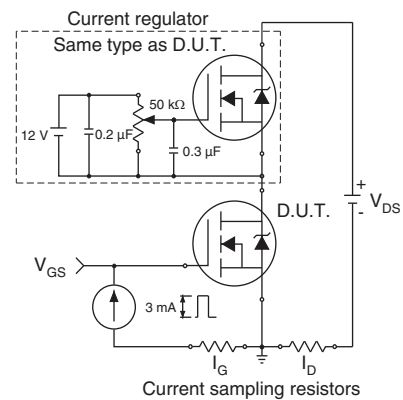
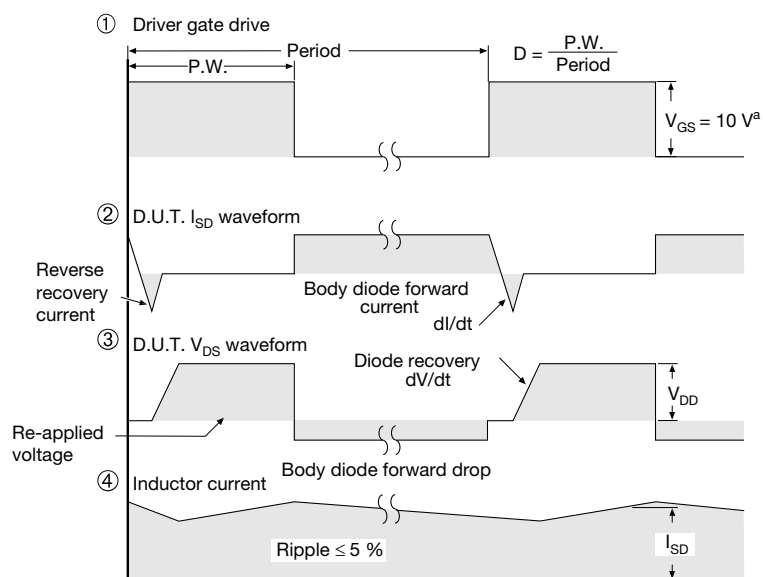
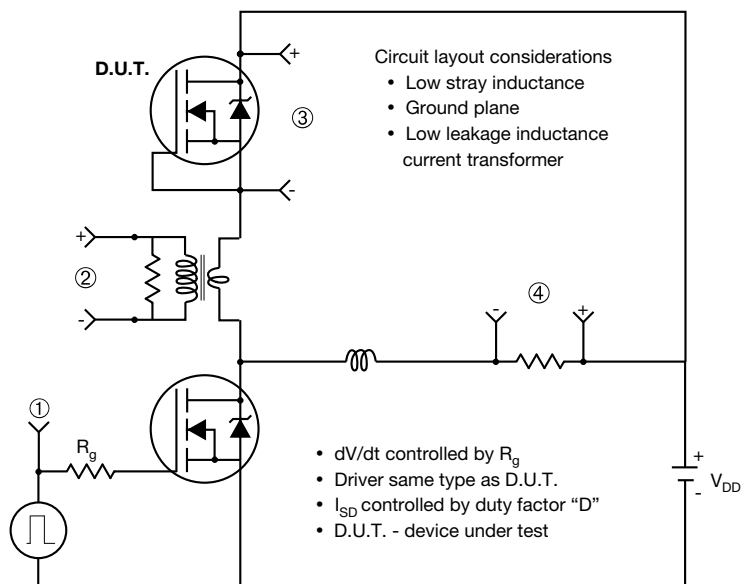


Fig. 13b - Gate Charge Test Circuit

### Peak Diode Recovery dV/dt Test Circuit

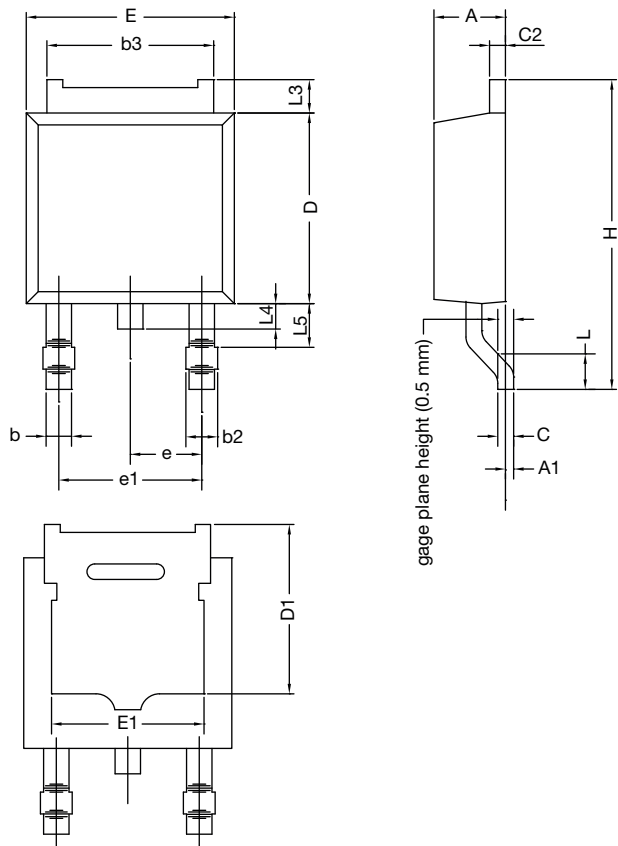


#### Note

a.  $V_{GS} = 5\text{ V}$  for logic level devices

**Fig. 14 - For N-Channel**

TO-252AA Case Outline



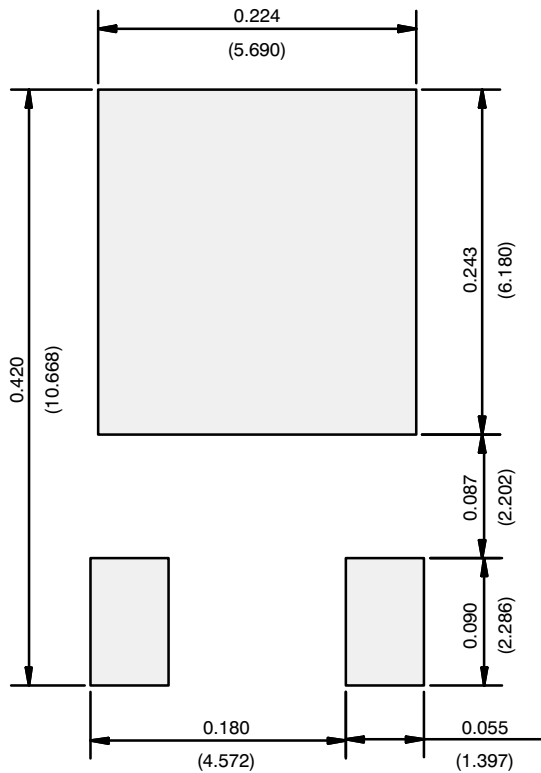
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060
ECN: T16-0236-Rev. P, 16-May-16 DWG: 5347				

Notes

- Dimension L3 is for reference only.



## RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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