ESD Protection Diodes

Low Capacitance ESD Protection Diode for High Speed Data Line

ESD8551, SZESD8551

The ESD8551 ESD protection diodes are designed to protect high speed data lines from ESD. Ultra−low capacitance and low ESD clamping voltage make this device an ideal solution for protecting voltage sensitive high speed data lines.

Features

- Low Capacitance (0.30 pF Max, I/O to GND)
- Protection for the Following IEC Standards: IEC 61000−4−2 (Level 4) & ISO 10605
- Low ESD Clamping Voltage
- SZESD8551MXWT5G − Wettable Flank Package for Optimal Automated Optical Inspection (AOI)
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- USB 3.0
- MHL 2.0
- eSATA

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

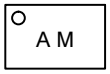
Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T_J	−55 to +125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Seconds)	T_L	260	°C
IEC 61000−4−2 Contact IEC 61000−4−2 Air ISO 10605 150 pF/2 kΩ ISO 10605 330 pF/2 kΩ ISO 10605 330 pF/330 Ω	ESD	±20 ±20 ±30 ±30 ±15	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

See Application Note AND8308/D for further description of survivability specs.

MARKING DIAGRAMS

X2DFN2
CASE 714AB

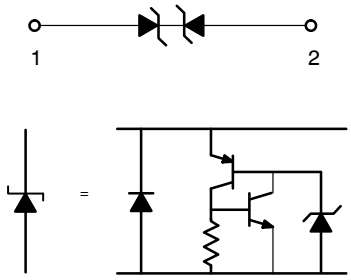


A = Specific Device Code
M = Date Code

X2DFNW2
CASE 711BG

K = Specific Device Code
M = Date Code

PIN CONFIGURATION AND SCHEMATIC



ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

Device	Package	Shipping†
ESD8551N2T5G	X2DFN2 (Pb−Free)	8000 / Tape & Reel
SZESD8551N2T5G*	X2DFN2 (Pb−Free)	8000 / Tape & Reel
SZESD8551MXWT5G*	X2DFNW2 (Pb−Free)	8000 / Tape & Reel

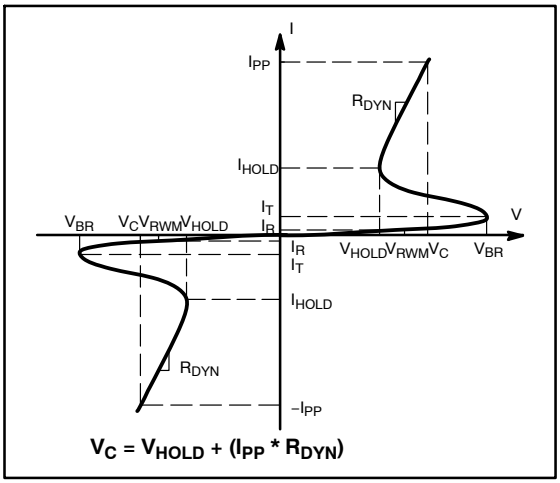
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
V_{RWM}	Working Peak Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
V_{HOLD}	Holding Reverse Voltage
I_{HOLD}	Holding Reverse Current
R_{DYN}	Dynamic Resistance
I_{PP}	Maximum Peak Pulse Current
V_C	Clamping Voltage @ I_{PP} $V_C = V_{HOLD} + (I_{PP} * R_{DYN})$



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	I/O Pin to GND			3.3	V
Breakdown Voltage	V_{BR}	I_T = 1 mA, I/O Pin to GND	5.5	7.9	8.3	V
Reverse Leakage Current	I_R	V_{RWM} = 3.3 V, I/O Pin to GND		5	500	nA
Reverse Holding Voltage	V_{HOLD}	I/O Pin to GND		2.05		V
Holding Reverse Current	I_{HOLD}	I/O Pin to GND		17		mA
Clamping Voltage (Note 1)	V_C	IEC61000−4−2, ±8 KV Contact				V
Clamping Voltage TLP (Note 2)	V_C	I_{PP} = 8 A } IEC 61000−4−2 Level 2 equivalent (±4 kV Contact, ±4 kV Air)		9.0		V
		I_{PP} = 16 A } IEC 61000−4−2 Level 4 equivalent (±8 kV Contact, ±8 kV Air)		16.0		
Dynamic Resistance	R_{DYN}	Pin1 to Pin2 Pin2 to Pin1		0.84 0.84		Ω
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz		0.20	0.30	pF
Junction Capacitance	C_J	V_R = 0 V, f = 2.5 GHz		0.19	0.25	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. For test procedure see Figure 7 and application note AND8307/D.
2. ANSI/ESD STM5.5.1 − Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model. TLP conditions: Z_0 = 50 Ω, t_p = 100 ns, t_r = 4 ns, averaging window; t_1 = 30 ns to t_2 = 60 ns.

TYPICAL CHARACTERISTICS

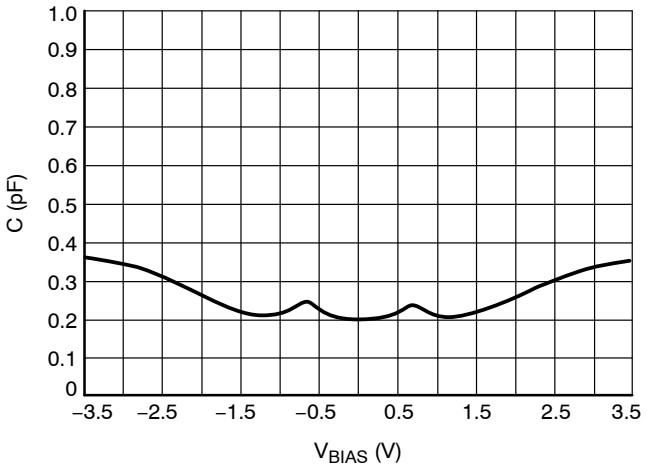


Figure 1. CV Characteristics

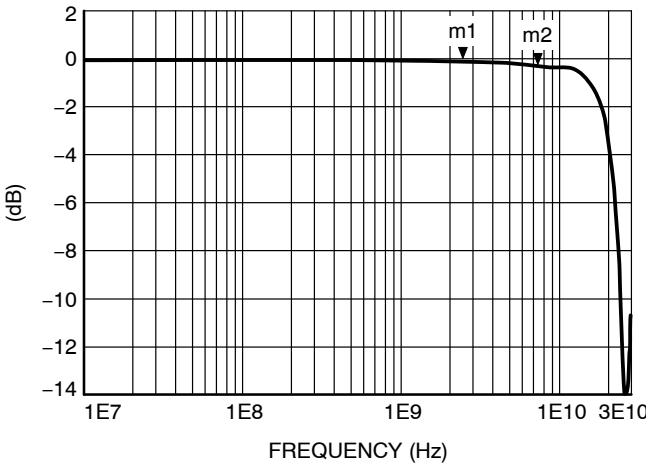


Figure 2. S21 Insertion Loss

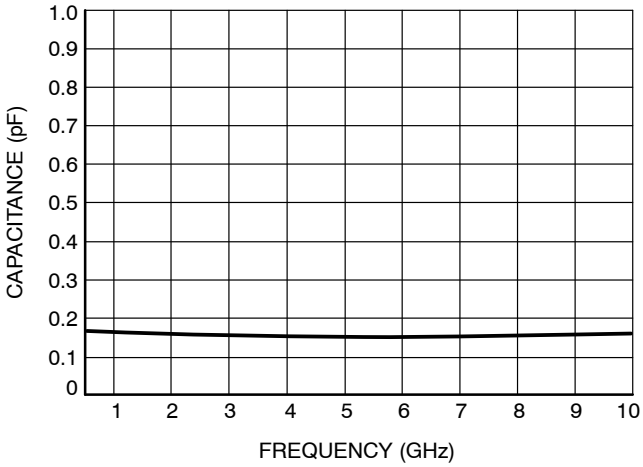


Figure 3. Capacitance over Frequency

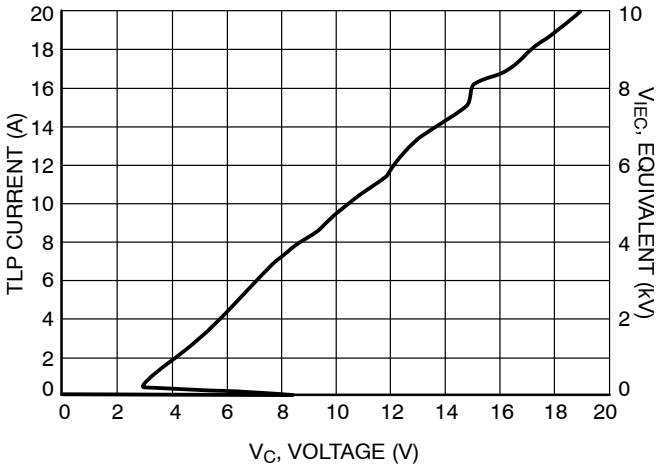


Figure 4. Positive TLP I−V Curve

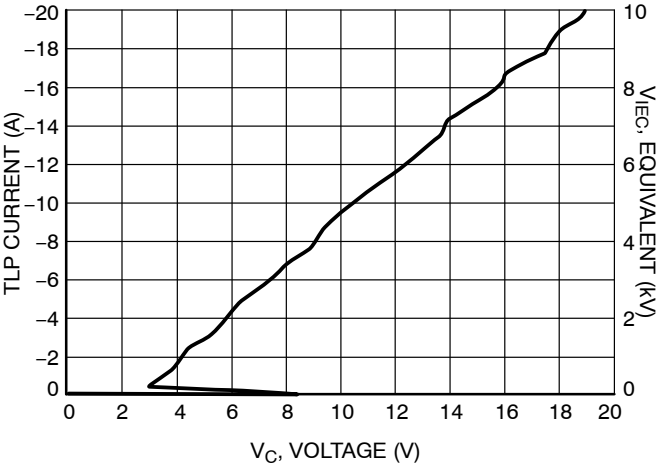
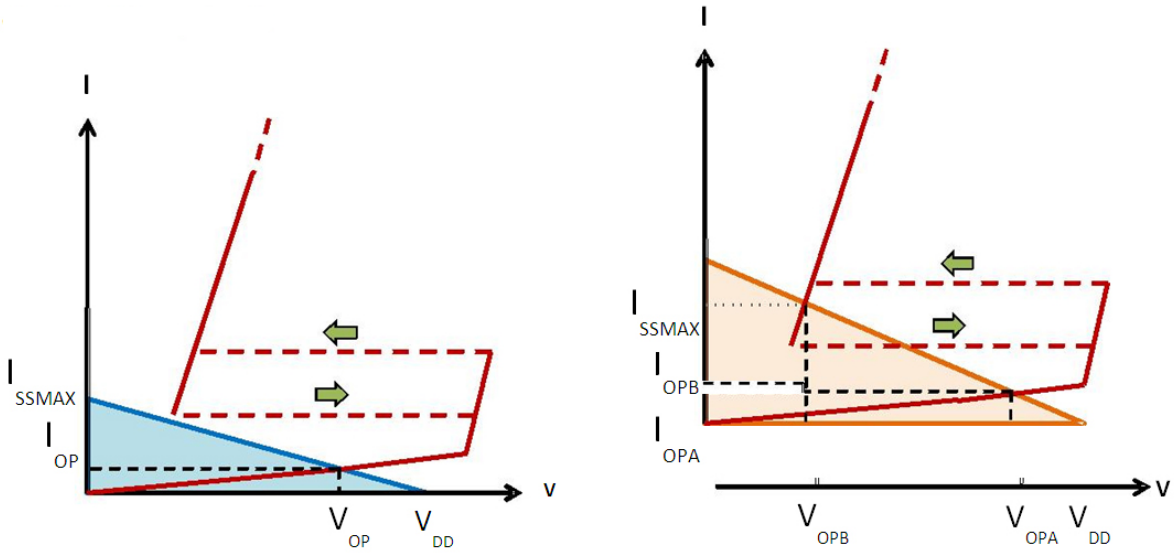


Figure 5. Negative TLP I−V Curve

Latch−Up Considerations

onsemi's 8000 series of ESD protection devices utilize a snap−back, SCR type structure. By using this technology, the potential for a latch−up condition was taken into account by performing load line analyses of common high speed serial interfaces. Example load lines for latch−up free applications and applications with the potential for latch−up are shown below with a generic IV characteristic of a snapback, SCR type structured device overlaid on each. In the latch−up free load line case, the IV characteristic of the snapback protection device intersects the load−line in one unique point (V_{OP}, I_{OP}). This is the only stable operating point of the circuit and the system is therefore latch−up free. In the non−latch up free load line case, the IV characteristic of the snapback protection device intersects the load−line in two points (V_{OPA}, I_{OPA}) and (V_{OPB}, I_{OPB}). Therefore in this case, the potential for latch−up exists if the system settles at (V_{OPB}, I_{OPB}) after a transient. Because of this, ESD8551 should not be used for HDMI applications − ESD8104 or ESD8040 have been designed to be acceptable for HDMI applications without latch−up. Please refer to Application Note AND9116/D for a more in−depth explanation of latch−up considerations using ESD8000 series devices.



ESD8551 Latch − up free:
USB 2.0 LS/FS, USB 2.0 HS,
USB 3.0 SS, DisplayPort

ESD8551 Potential Latch − up:
HDMI 1.4/1.3a TMDS

Figure 6. Example Load Lines for Latch−up Free Applications and Applications with the Potential for Latch−up

Table 1. SUMMARY OF SCR REQUIREMENTS FOR LATCH−UP FREE APPLICATIONS

Application	VBR (min) (V)	IH (min) (mA)	VH (min) (V)	onsemi ESD8000 Series Recommended PN
HDMI 1.4/1.3a TMDS	3.465	54.78	1.0	ESD8104, ESD8040
USB 2.0 LS/FS	3.301	1.76	1.0	ESD8004, ESD8551
USB 2.0 HS	0.482	N/A	1.0	ESD8004, ESD8551
USB 3.0 SS	2.800	N/A	1.0	ESD8004, ESD8006, ESD8551
DisplayPort	3.600	25.00	1.0	ESD8004, ESD8006, ESD8551

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

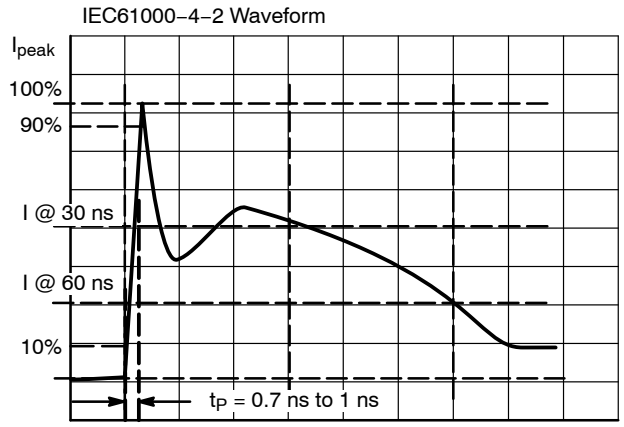


Figure 7. IEC61000−4−2 Spec

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 8. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 9 where an 8 kV IEC 61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I−V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

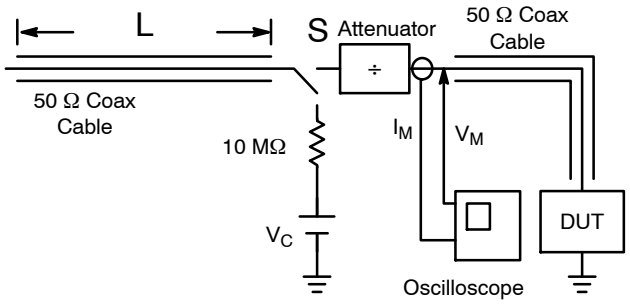


Figure 8. Simplified Schematic of a Typical TLP System

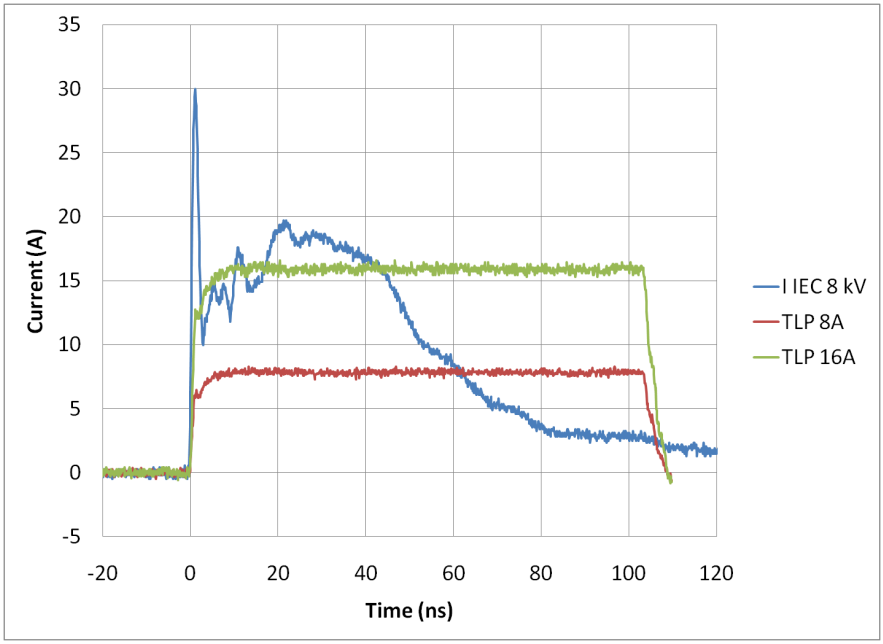
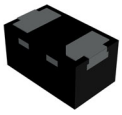


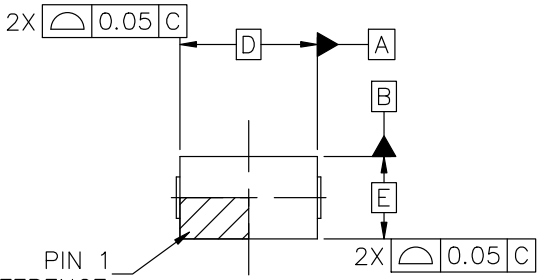
Figure 9. Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

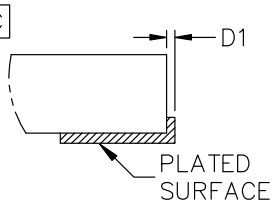


X2DFNW2 1.00x0.60x0.37, 0.65P
CASE 711BG
ISSUE D

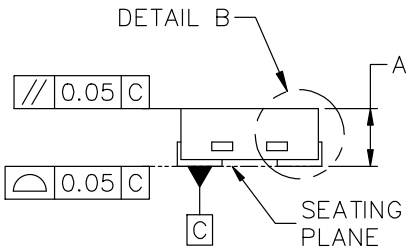
DATE 29 FEB 2024



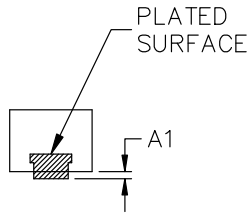
TOP VIEW



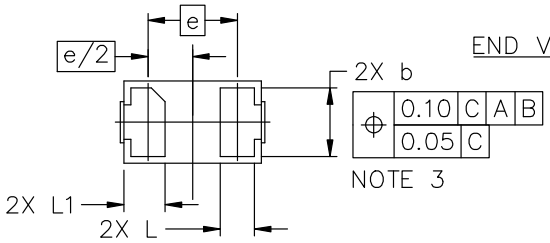
DETAIL "B"
SCALE 2:1



SIDE VIEW



END VIEW

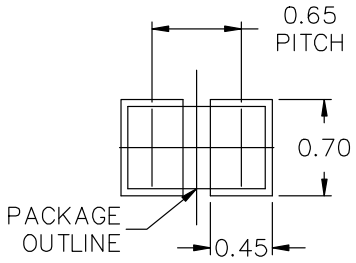


BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. DIMENSION b APPLIES TO THE PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 FROM THE TERMINAL TIP.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.34	0.37	0.40
A1	−−−	−−−	0.05
b	0.45	0.50	0.55
D	1.00 BSC		
D1	−−−	−−−	0.05
E	0.60 BSC		
e	0.65 BSC		
L	0.22 REF		
L1	0.24	0.28	0.34



RECOMMENDED MOUNTING FOOTPRINT*

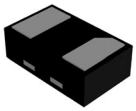
* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XX = Specific Device Code
M = Date Code

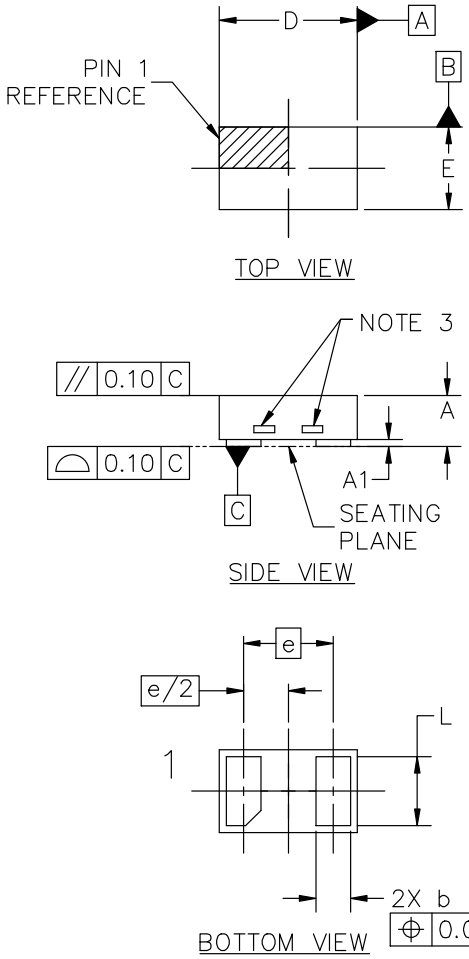
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G", may or not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON15241G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**X2DFNW2 1.00x0.60x0.37, 0.65P**	**PAGE 1 OF 1**



X2DFN2 1.00x0.60x0.37, 0.65P
CASE 714AB
ISSUE C

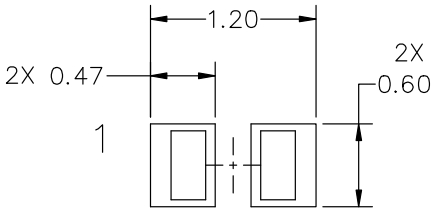
DATE 21 FEB 2024



NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. EXPOSED COPPER ALLOWED AS SHOW.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.34	0.37	0.40
A1	−−−	0.03	0.050
b	0.20	0.25	0.30
D	0.95	1.00	1.05
E	0.55	0.60	0.65
e	0.65 BSC		
L	0.45	0.50	0.55



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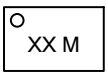

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*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**X2DFN2 1.00x0.60x0.37, 0.65P**	**PAGE 1 OF 1**

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