15-W Filter-Free Stereo Class-D Audio Power Amplifier with SpeakerGuard™

Check for Samples: TPA3117D2

FEATURES

- **15-W/ch into 8Ω Loads at 10% THD+N From a 16V Supply**
- **10-W/ch into 8Ω Loads at 10% THD+N From a 13V Supply**
- **90% Efficient Class-D Operation Eliminates Need for Heat Sinks**
- **Wide Supply Voltage Range Allows Operation from 8V to 26V**
- **Filter-Free Operation**
- **SpeakerGuard™ Speaker Protection Includes Adjustable Power Limiter**
- **Excellent THD+N / Pop-Free Performance**
- **Four Selectable, Fixed Gain Settings**
- **Differential Inputs**
- **Selectable Switching Frequency (290kHz or 390kHz) Allows Multiple Devices to be Used in One System**
- **Integrated 5V Regulator With up to 30 mA of Output Current for Powering External Data Converters**
- **5mm x 5mm QFN Packaging**

APPLICATIONS

- **Televisions**
- **Consumer Audio Equipment**
- **All-in-One Computers**

DESCRIPTION

The TPA3117D2 is a 15W (per channel) efficient, Class-D audio power amplifier for driving bridged-tied stereo speakers. Advanced EMI Suppression Technology enables the use of inexpensive ferrite bead filters at the outputs while meeting EMC requirements. SpeakerGuard™ speaker protection circuitry includes an adjustable power limiter. The adjustable power limiter allows the user to set a "virtual" voltage rail lower than the chip supply to limit the amount of current through the speaker.

The TPA3117D2 can drive stereo speakers as low as 4Ω. The high efficiency of the TPA3117D2, 90%, eliminates the need for an external heat sink when playing music.

The outputs are also fully protected against shorts to GND, V_{CC}, and output-to-output. The short-circuit protection and thermal protection includes an auto-recovery feature.

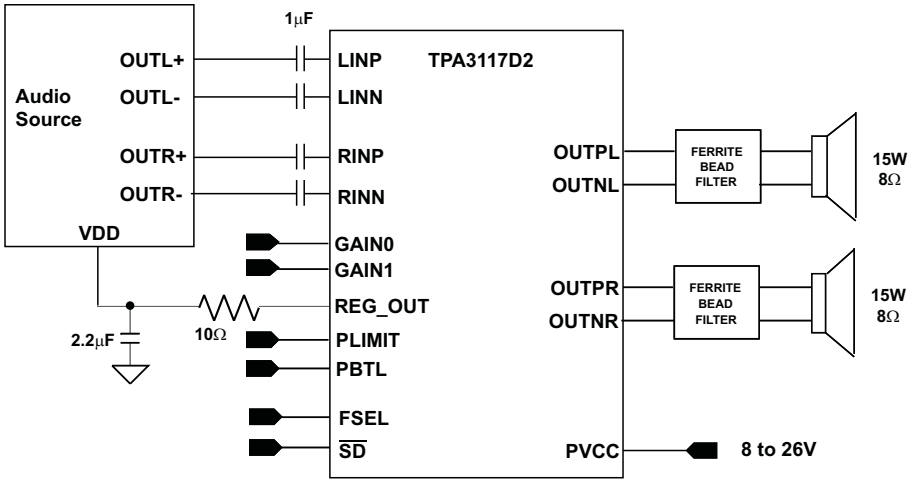


Figure 1. TPA3117D2 Simplified Application Schematic

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SpeakerGuard is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			UNIT
V_{CC}	Supply voltage	AVCC, PVCC	–0.3V to 30V
V_I	Interface pin voltage	$\overline{SD}$, GAIN0, GAIN1, PBTL, FSEL(2)	–0.3V to V_{CC} + 0.3V
		PLIMIT	–0.3V to REG_OUT + 0.3V
		RINN, RINP, LINN, LINP	–0.3V to 6.3V
	Continuous total power dissipation		See Dissipation Rating Table
T_A	Operating free-air temperature range		–40°C to 85°C
T_J	Operating junction temperature range(3)		–40°C to 150°C
T_{stg}	Storage temperature range		–65°C to 150°C
R_L	Minimum Load Resistance	BTL: PVCC > 15V	4.8
		BTL: PVCC ≤ 15V	3.2
		PBTL	3.2
ESD	Electrostatic discharge	Human body model (4) (all pins)	±2kV
		Charged-device model (5) (all pins)	±500V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operations of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For input voltage >6V, a series current limiting resistor of at least 100kΩ is recommended.
(3) The TPA3117D2 incorporates an exposed thermal pad on the underside of the chip. This acts as a heatsink, and it must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in the device going into thermal protection shutdown.
(4) In accordance with JEDEC Standard 22, Test Method A114-B.
(5) In accordance with JEDEC Standard 22, Test Method C101-A

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply voltage	PVCC, AVCC	8	26	V
V_{IH}	High-level input voltage	$\overline{SD}$, GAIN0, GAIN1, PBTL, FSEL	2		V
V_{IL}	Low-level input voltage	$\overline{SD}$, GAIN0, GAIN1, PBTL, FSEL		0.8	V
I_{IH}	High-level input current	$\overline{SD}$, GAIN0, GAIN1, PBTL, FSEL, V_I = 2V, V_{CC} = 18V		50	µA
I_{IL}	Low-level input current	$\overline{SD}$, GAIN0, GAIN1, PBTL, FSEL, V_I = 0.8V, V_{CC} = 18V		5	µA
T_A	Operating free-air temperature		–40	85	°C

THERMAL INFORMATION

THERMAL METRIC(1)		TPA3117D2 RHB (32 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	33.7	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	36.3	
θ_{JB}	Junction-to-board thermal resistance	9.8	
ψ_{JT}	Junction-to-top characterization parameter	0.6	
ψ_{JB}	Junction-to-board characterization parameter	9.5	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	3.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

DC CHARACTERISTICS

T_A = 25°C, V_{CC} = 24 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
| V_{OS} |	Class-D output offset voltage (measured differentially)	V_I = 0V, Gain = 18.2dB			1.5	15	mV
I_{CC}	Quiescent supply current	$\overline{SD}$ = 2V, no load, V_{CC} = 26V			25	50	mA
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	$\overline{SD}$ = 0.8V, no load, V_{CC} = 24V			2.5	5	mA
$r_{DS(on)}$	Drain-source on-state resistance	V_{CC} = 12V, I_O = 500mA, T_J = 25°C	High Side		240		mΩ
			Low side		240		
G	Gain	GAIN1 = 0.8V	GAIN0 = 0.8 V	8	9	10	dB
			GAIN0 = 2 V	11.1	12.1	13.1	
		GAIN1 = 2V	GAIN0 = 0.8 V	14.2	15.2	16.2	dB
			GAIN0 = 2 V	17.2	18.2	19.2	
t_{on}	Turn-on time	$\overline{SD}$ = 2V			14		ms
t_{OFF}	Turn-off time	$\overline{SD}$ = 0.8V			2		µs

DC CHARACTERISTICS

T_A = 25°C, V_{CC} = 12 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
| V_{OS} |	Class-D output offset voltage (measured differentially)	V_I = 0V, Gain = 18.2dB			1.5	15	mV
I_{CC}	Quiescent supply current	$\overline{SD}$ = 2V, no load, V_{CC} = 12V			15	35	mA
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	$\overline{SD}$ = 0.8V, no load, V_{CC} = 12V			2.5	5	mA
$r_{DS(on)}$	Drain-source on-state resistance	V_{CC} = 12V, I_O = 500mA, T_J = 25°C	High Side		240		mΩ
			Low side		240		
G	Gain	GAIN1 = 0.8V	GAIN0 = 0.8 V	8	9	10	dB
			GAIN0 = 2 V	11.1	12.1	13.1	
		GAIN1 = 2V	GAIN0 = 0.8 V	14.2	15.2	16.2	dB
			GAIN0 = 2 V	17.2	18.2	19.2	
t_{ON}	Turn-on time	$\overline{SD}$ = 2V			14		ms
t_{OFF}	Turn-off time	$\overline{SD}$ = 0.8V			2		µs

LDO CHARACTERISTICS

T_A = 25°C, V_{CC} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_I	Input voltage	V_{CC}		8	12	26	V
I_O	Continuous output current					30	mA
V_O	Output voltage	0 < I_O < 30mA, 10.8V < V_{IN} < 13.2			5		V
	Line regulation	I_L = 5mA, 10.8V < V_{IN} < 13.2V			6		µV
	Load regulation	I_L = 0 - 30mA, V_{IN} = 12V, Measurement taken with an external 10Ω series resistor			10.2		mV / mA
PSRR	Power supply ripple rejection	V_{CC} = 12V, I_L = 20mA	f = 100Hz		92		dB
			f = 1kHz		72		

AC CHARACTERISTICS

T_A = 25°C, V_{CC} = 24 V, R_L = 8 Ω (unless otherwise noted)

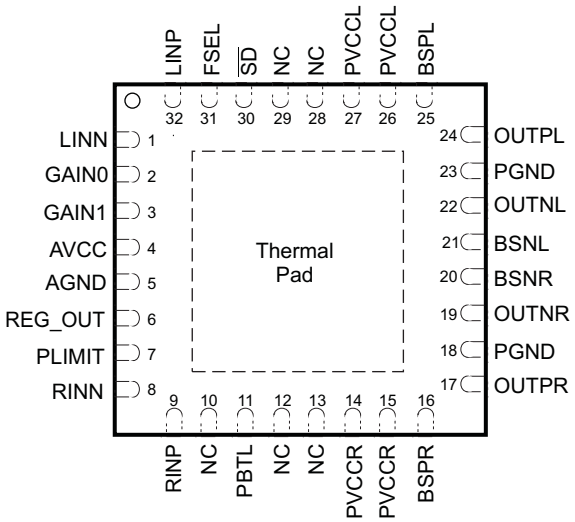
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
K_{SVR}	Power Supply ripple rejection	200mV_{PP} ripple at 1kHz, Gain = 18.2dB, Inputs ac-coupled to AGND		–70		dB
P_O	Continuous output power	THD+N = 10%, f = 1kHz, V_{CC} = 16V		15		W
THD+N	Total harmonic distortion + noise	V_{CC} = 16V, f = 1kHz, P_O = 7.5W (half-power)		0.1		%
V_n	Output integrated noise	20Hz to 22kHz, A-weighted filter, Gain = 9dB		55		µV
				–85		dBV
	Crosstalk	V_O = 1Vrms, Gain = 9dB, f = 1kHz		–100		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N < 1%, f = 1kHz, Gain = 9dB, A-weighted		102		dB
f_{OSC}	Oscillator frequency	FSEL = 0.8V		290		kHz
		FSEL = 2V		390		
	Thermal trip point			150		°C
	Thermal hysteresis			15		°C

AC CHARACTERISTICS

T_A = 25°C, V_{CC} = 12 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
K_{SVR}	Supply ripple rejection	200mV_{PP} ripple from 20Hz – 1kHz, Gain = 18.2dB, Inputs ac-coupled to AGND		–70		dB
P_O	Continuous output power	THD+N = 10%, f = 1kHz; V_{CC} = 13V		10		W
THD+N	Total harmonic distortion + noise	R_L = 8Ω, f = 1kHz, P_O = 5W (half-power)		0.06		%
V_n	Output integrated noise	20Hz to 22kHz, A-weighted filter, Gain = 9dB		48		µV
				–86		dBV
	Crosstalk	P_o = 1W, Gain = 9dB, f = 1kHz		–100		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N < 1%, f = 1kHz, Gain = 9dB, A-weighted		102		dB
f_{OSC}	Oscillator frequency	FSEL = 0.8V		290		kHz
		FSEL = 2V		390		
	Thermal trip point			150		°C
	Thermal hysteresis			15		°C

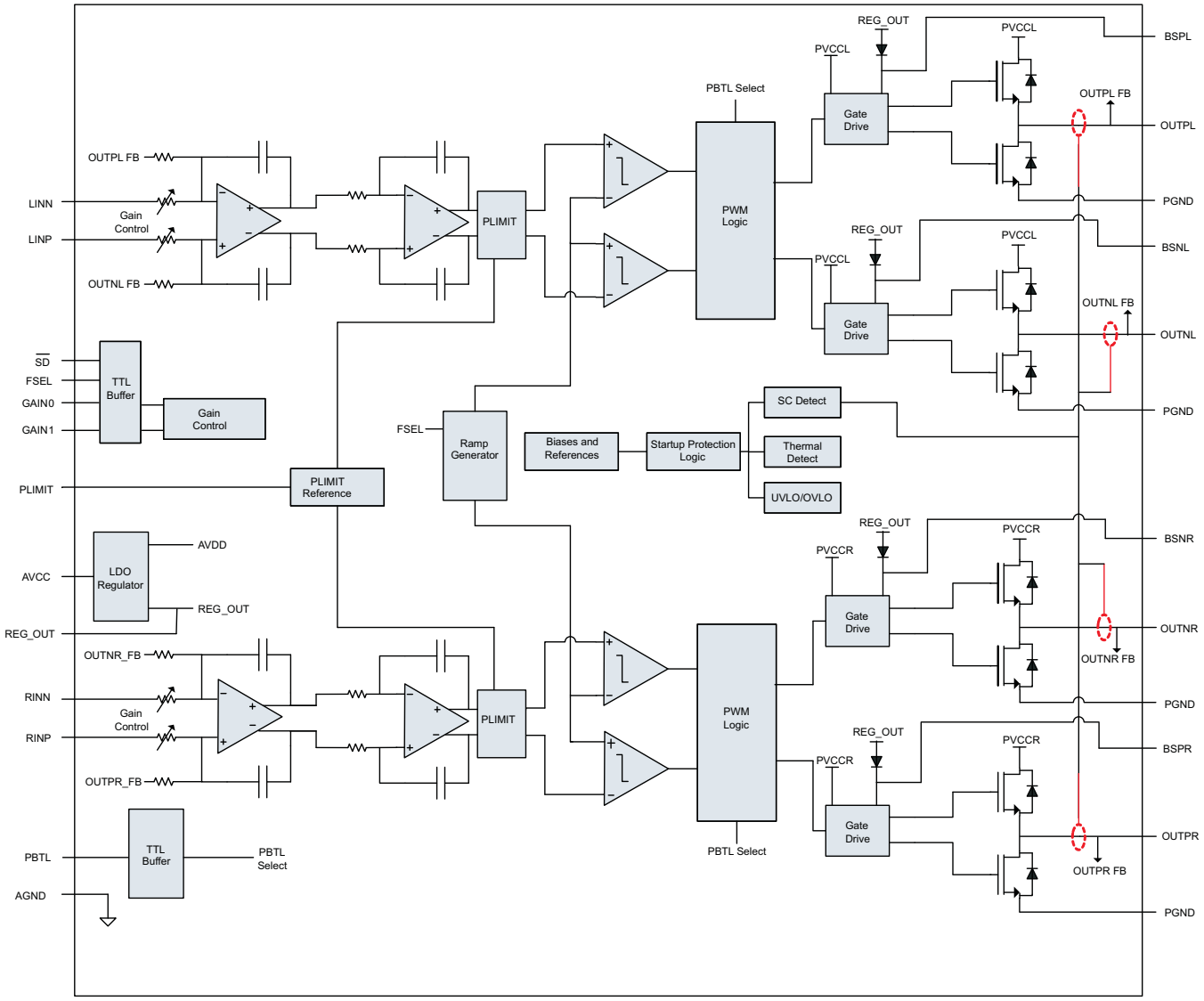
RHB (QFN) PACKAGE
(TOP VIEW)



PIN FUNCTIONS

PIN		I/O/P	DESCRIPTION
NAME	NUMBER		
LINN	1	I	Negative audio input for left channel. Biased at 3V.
GAIN0	2	I	Gain select least significant bit. TTL logic levels with compliance to AVCC.
GAIN1	3	I	Gain select most significant bit. TTL logic levels with compliance to AVCC.
AVCC	4	P	Analog supply
AGND	5		Analog signal ground. Connect to the thermal pad.
REG_OUT	6	O	5V regulated output. Connect 2.2µF to AGND after the series 10 Ω resistor.
PLIMIT	7	I	Power limit level adjust. Connect a resistor divider from REG_OUT to AGND to set power limit. Connect directly to REG_OUT for no power limit.
RINN	8	I	Negative audio input for right channel. Biased at 3V.
RINP	9	I	Positive audio input for right channel. Biased at 3V.
NC	10, 12, 13, 28, 29		Not connected
PBTL	11	I	Parallel BTL mode switch (low = BTL mode, high = PBTL mode)
PVCCR	14, 15	P	Power supply for right channel H-bridge. Right channel and left channel power supply inputs are connected internally. PVCCR and PVCCL must be connected together on the PCB.
BSPR	16	I	Bootstrap I/O for right channel, positive high-side FET.
OUTPR	17	O	Class-D H-bridge positive output for right channel.
PGND	18		Power ground for the H-bridges.
OUTNR	19	O	Class-D H-bridge negative output for right channel.
BSNR	20	I	Bootstrap I/O for right channel, negative high-side FET.
BSNL	21	I	Bootstrap I/O for left channel, negative high-side FET.
OUTNL	22	O	Class-D H-bridge negative output for left channel.
PGND	23		Power ground for the H-bridges.
OUTPL	24	O	Class-D H-bridge positive output for left channel.
BSPL	25	I	Bootstrap I/O for left channel, positive high-side FET.
PVCCL	26, 27	P	Power supply for left channel H-bridge. Right channel and left channel power supply inputs are connected internally. PVCCR and PVCCL must be connected together on the PCB.
$\overline{SD}$	30	I	Shutdown logic input for audio amp (LOW = outputs Hi-Z, HIGH = outputs enabled). TTL logic levels with compliance to AVCC.
FSEL	31	I	Frequency select input pin (low = 300kHz, high = 400kHz)
LINP	32	I	Positive audio input for left channel. Biased at 3V.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

(All Measurements taken at 1 kHz, unless otherwise noted. Measurements were made using the TPA3117D2 EVM which is available at ti.com.)

TOTAL HARMONIC DISTORTION vs FREQUENCY (BTL)

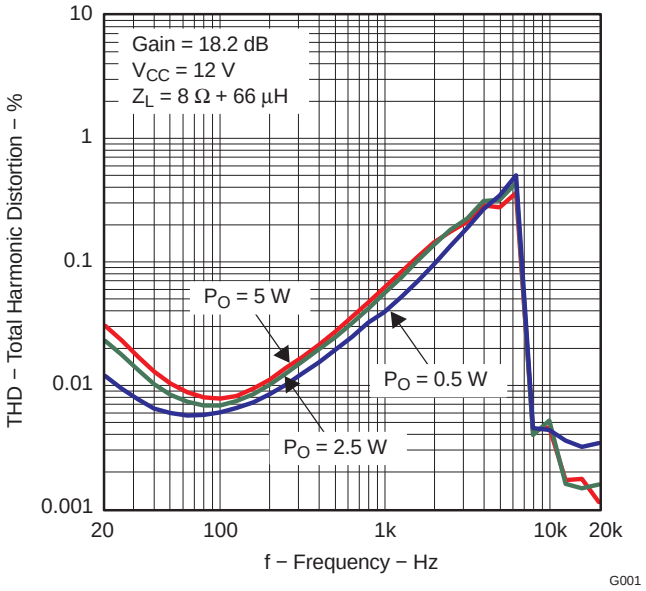


Figure 2.

TOTAL HARMONIC DISTORTION vs FREQUENCY (BTL)

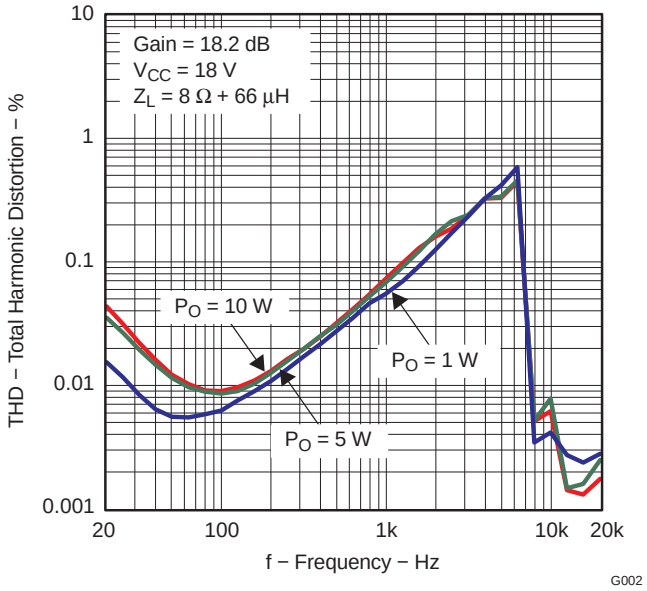


Figure 3.

TOTAL HARMONIC DISTORTION vs FREQUENCY (BTL)

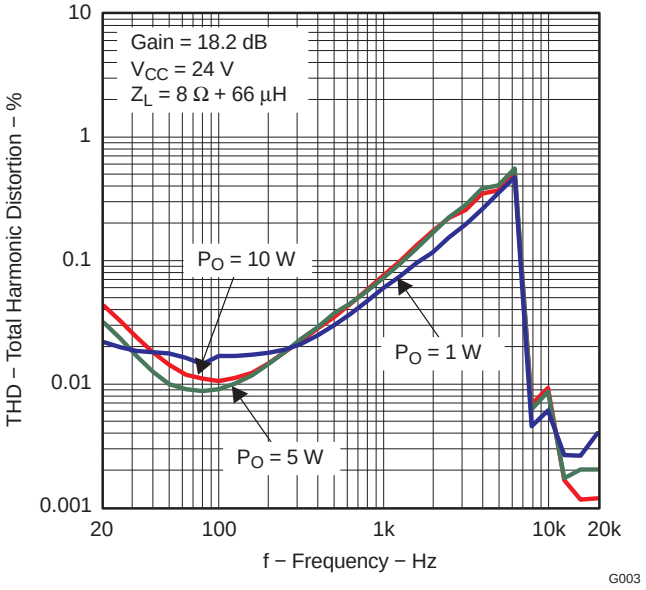


Figure 4.

TOTAL HARMONIC DISTORTION vs FREQUENCY (BTL)

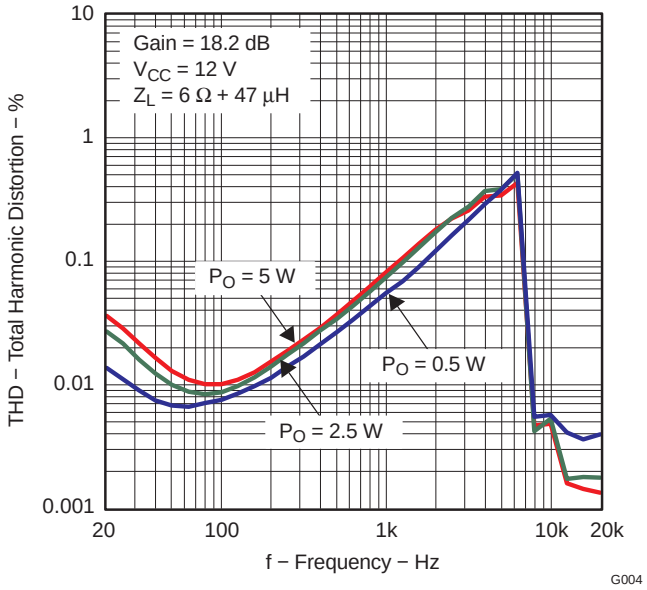


Figure 5.

TYPICAL CHARACTERISTICS (continued)

(All Measurements taken at 1 kHz, unless otherwise noted. Measurements were made using the TPA3117D2 EVM which is available at ti.com.)

TOTAL HARMONIC DISTORTION vs FREQUENCY (BTL)

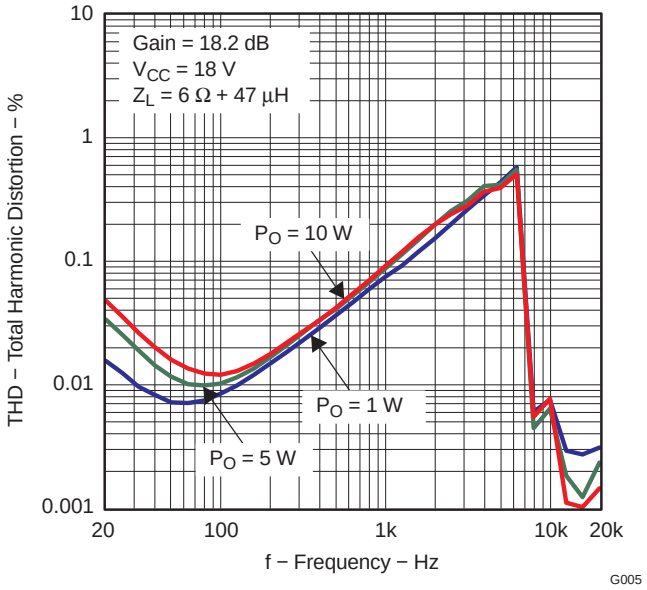


Figure 6.

TOTAL HARMONIC DISTORTION vs FREQUENCY (BTL)

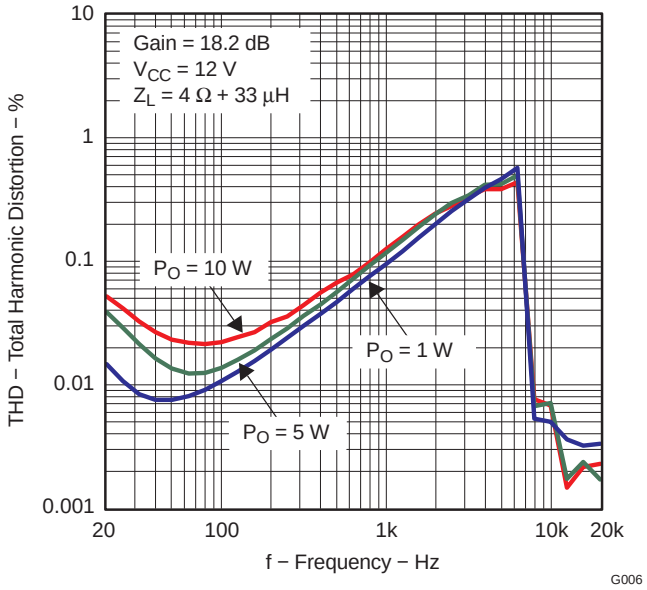


Figure 7.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER (BTL)

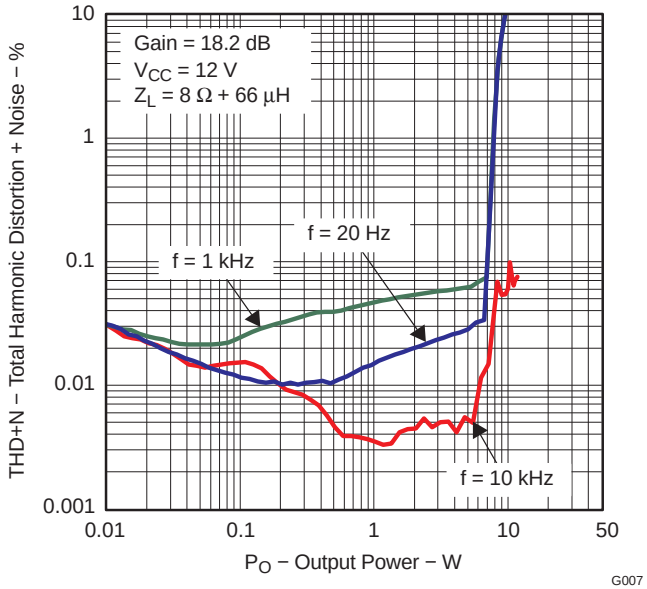


Figure 8.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER (BTL)

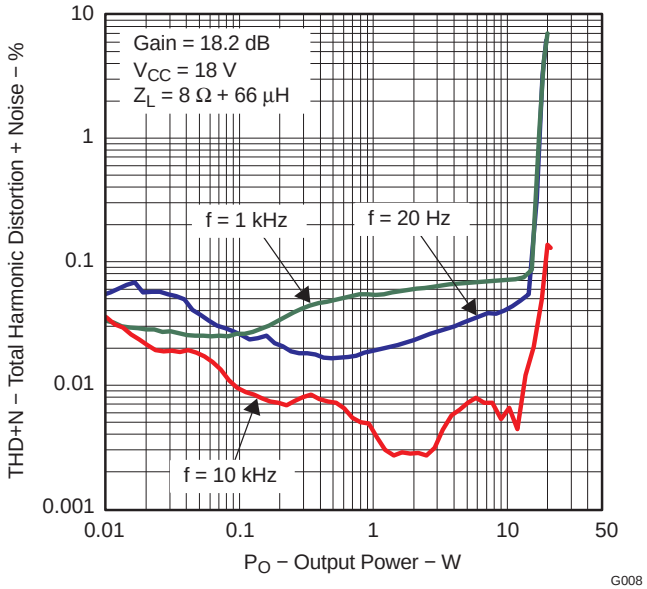


Figure 9.

TYPICAL CHARACTERISTICS (continued)

(All Measurements taken at 1 kHz, unless otherwise noted. Measurements were made using the TPA3117D2 EVM which is available at ti.com.)

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER (BTL)

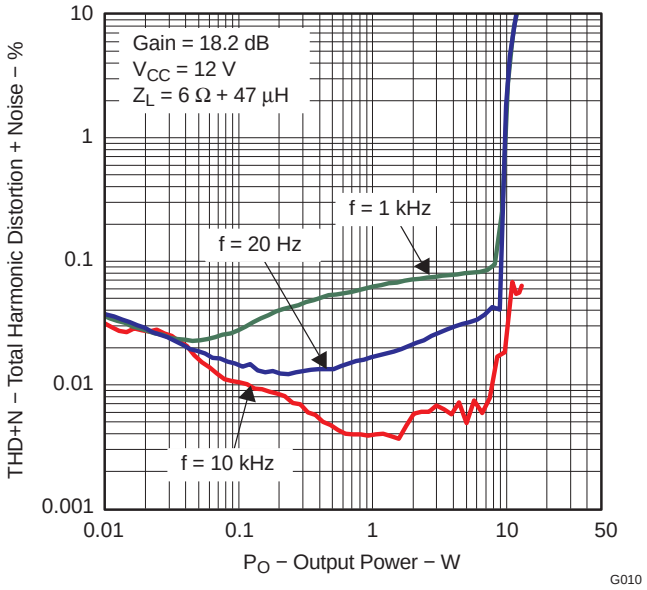


Figure 10.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER (BTL)

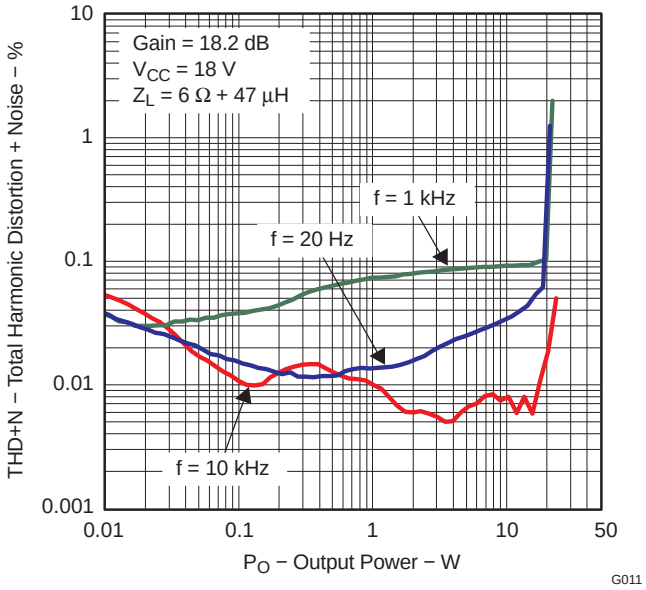


Figure 11.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER (BTL)

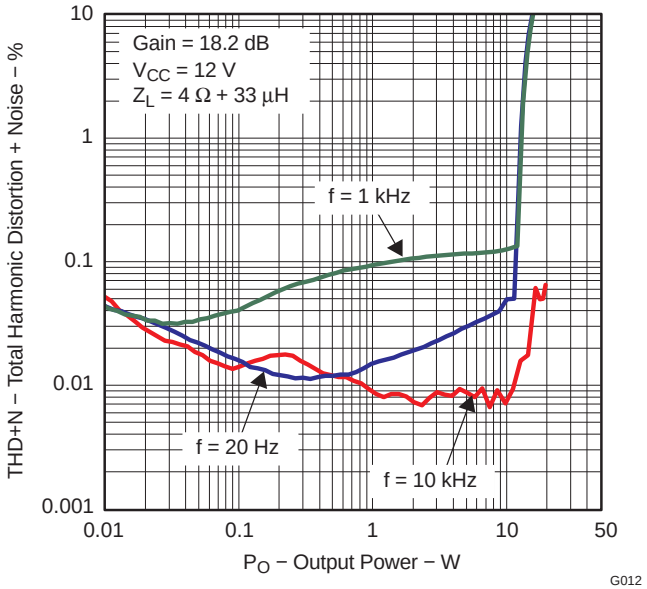


Figure 12.

MAXIMUM OUTPUT POWER vs PLIMIT VOLTAGE (BTL)

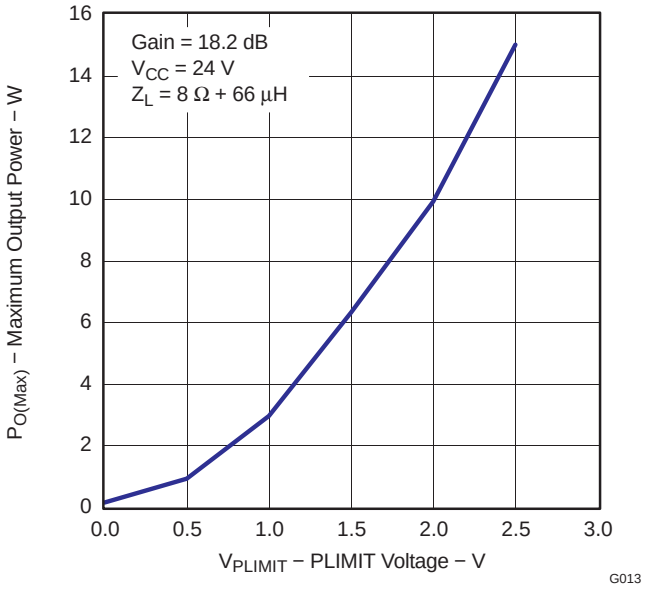
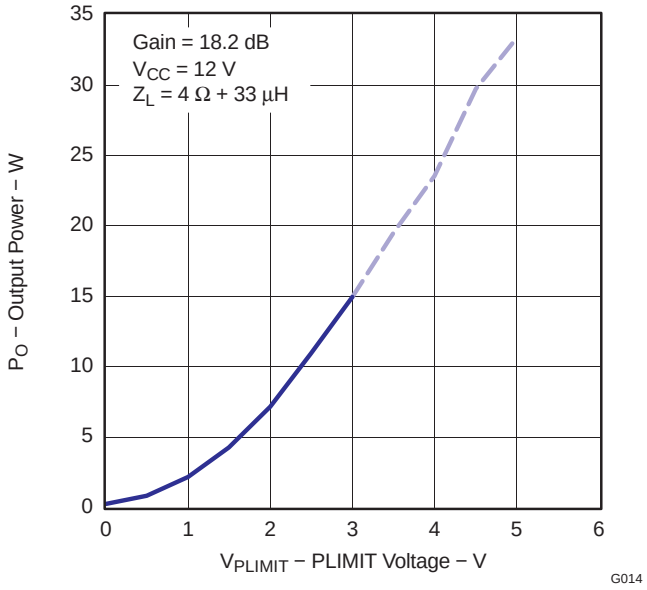


Figure 13.

TYPICAL CHARACTERISTICS (continued)

(All Measurements taken at 1 kHz, unless otherwise noted. Measurements were made using the TPA3117D2 EVM which is available at ti.com.)

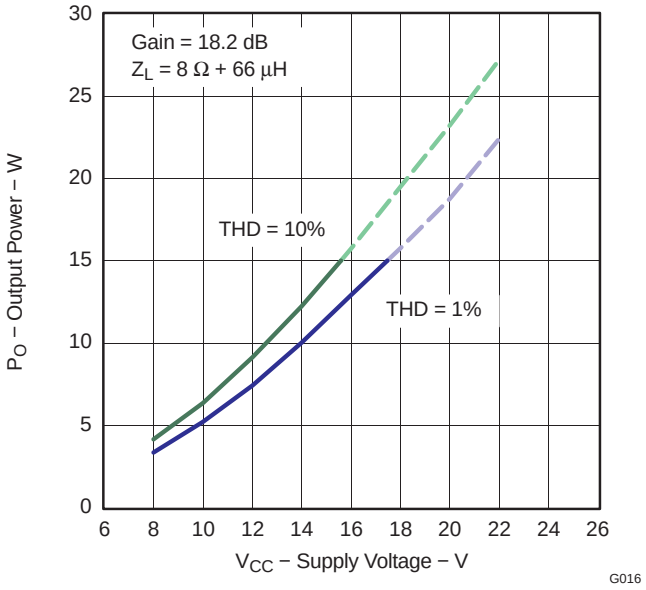
OUTPUT POWER vs PLIMIT VOLTAGE (BTL)



Note: Dashed Lines represent thermally limited regions.

Figure 14.

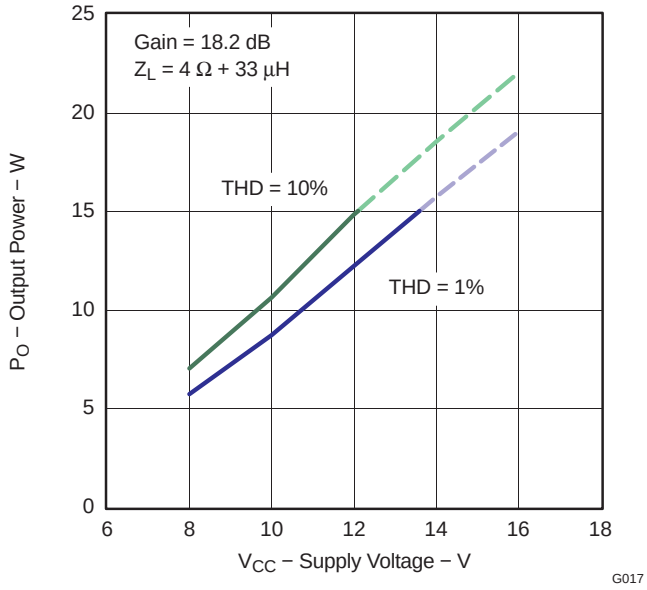
OUTPUT POWER vs SUPPLY VOLTAGE (BTL)



Note: Dashed Lines represent thermally limited regions.

Figure 15.

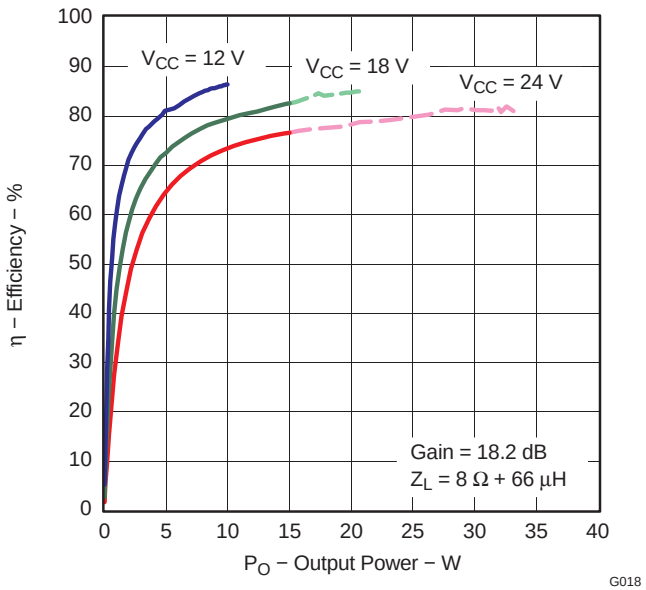
OUTPUT POWER vs SUPPLY VOLTAGE (BTL)



Note: Dashed Lines represent thermally limited regions.

Figure 16.

EFFICIENCY vs OUTPUT POWER (BTL)



Note: Dashed Lines represent thermally limited regions.

Figure 17.

TYPICAL CHARACTERISTICS (continued)

(All Measurements taken at 1 kHz, unless otherwise noted. Measurements were made using the TPA3117D2 EVM which is available at ti.com.)

EFFICIENCY vs OUTPUT POWER (BTL with LC FILTER)

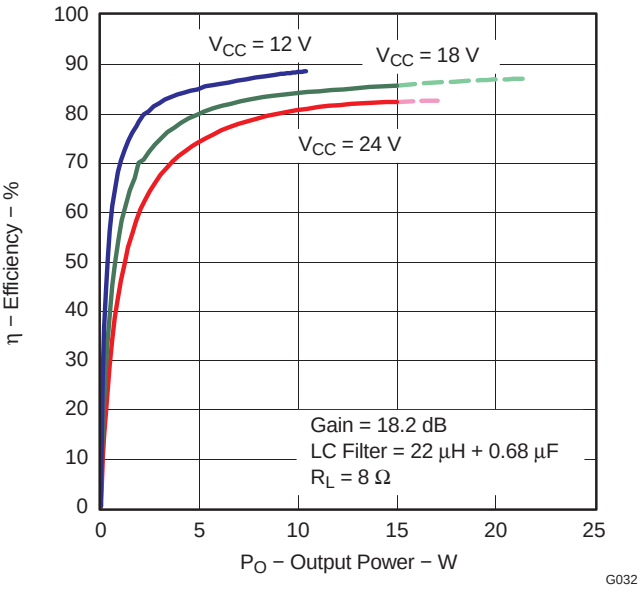
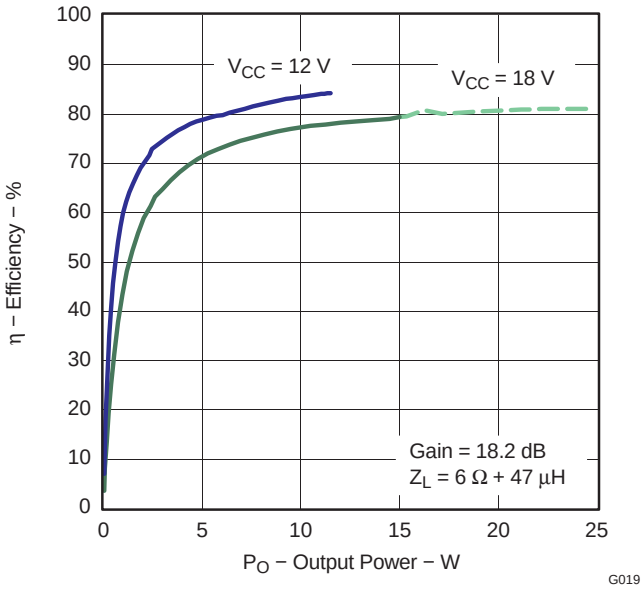


Figure 18.

EFFICIENCY vs OUTPUT POWER (BTL)



Note: Dashed Lines represent thermally limited regions.

Figure 19.

EFFICIENCY vs OUTPUT POWER (BTL with LC FILTER)

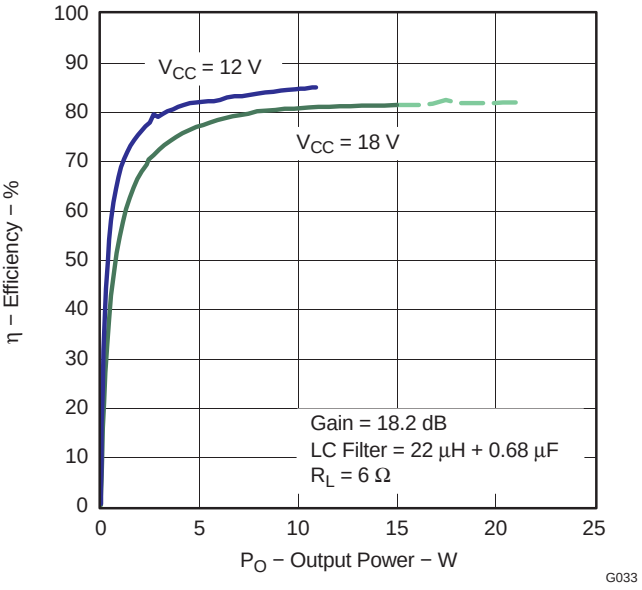


Figure 20.

EFFICIENCY vs OUTPUT POWER (BTL)

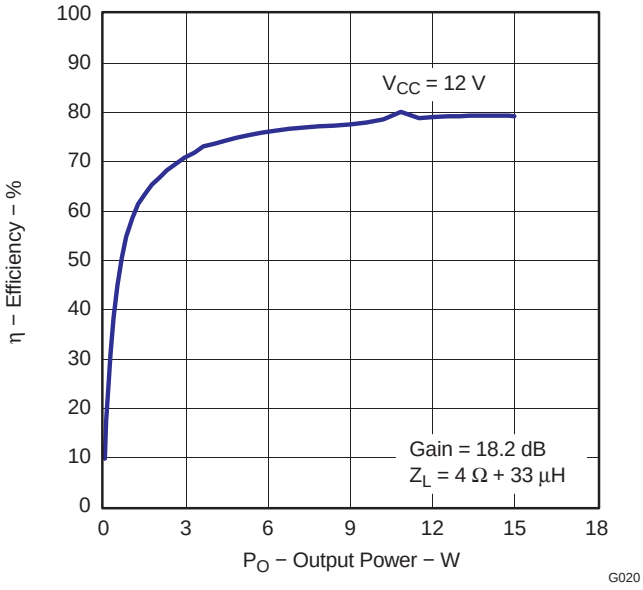


Figure 21.

TYPICAL CHARACTERISTICS (continued)

(All Measurements taken at 1 kHz, unless otherwise noted. Measurements were made using the TPA3117D2 EVM which is available at ti.com.)

EFFICIENCY vs OUTPUT POWER (BTL with LC FILTER)

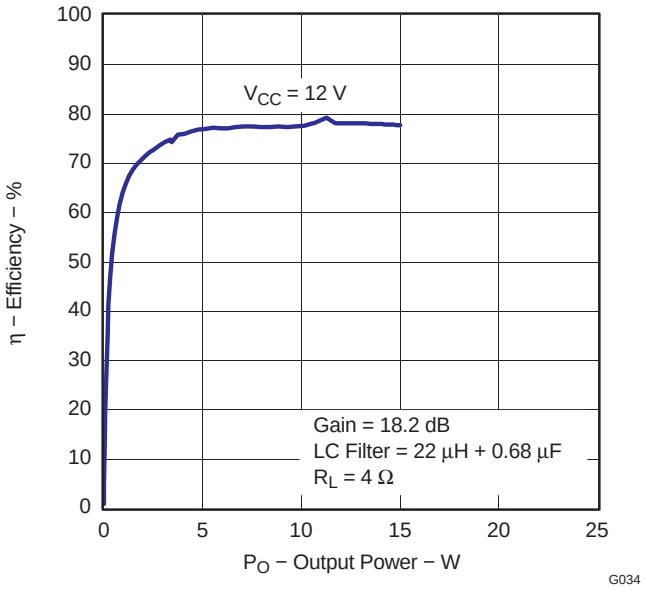
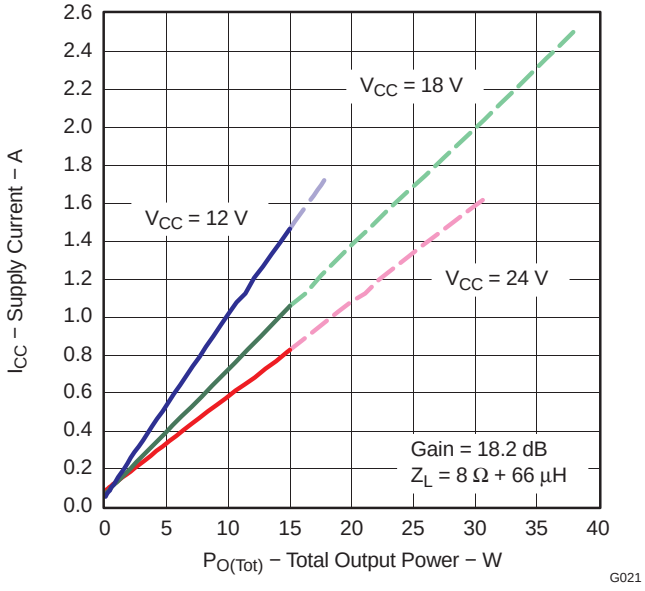


Figure 22.

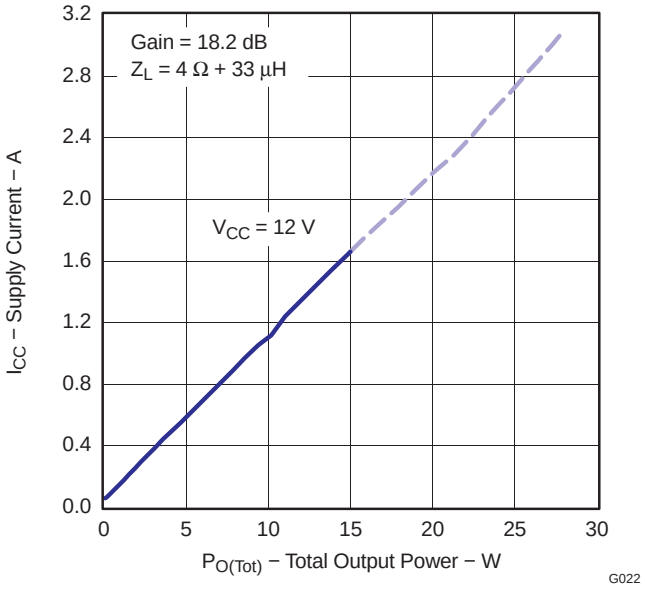
SUPPLY CURRENT vs TOTAL OUTPUT POWER (BTL)



Note: Dashed Lines represent thermally limited regions.

Figure 23.

SUPPLY CURRENT vs TOTAL OUTPUT POWER (BTL)



Note: Dashed Lines represent thermally limited regions.

Figure 24.

CROSSTALK vs FREQUENCY (BTL)

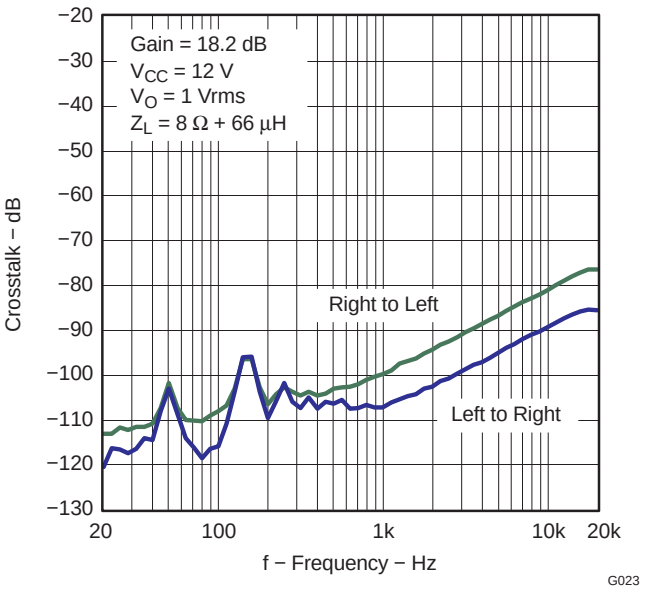


Figure 25.

TYPICAL CHARACTERISTICS (continued)

(All Measurements taken at 1 kHz, unless otherwise noted. Measurements were made using the TPA3117D2 EVM which is available at ti.com.)

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY (BTL)

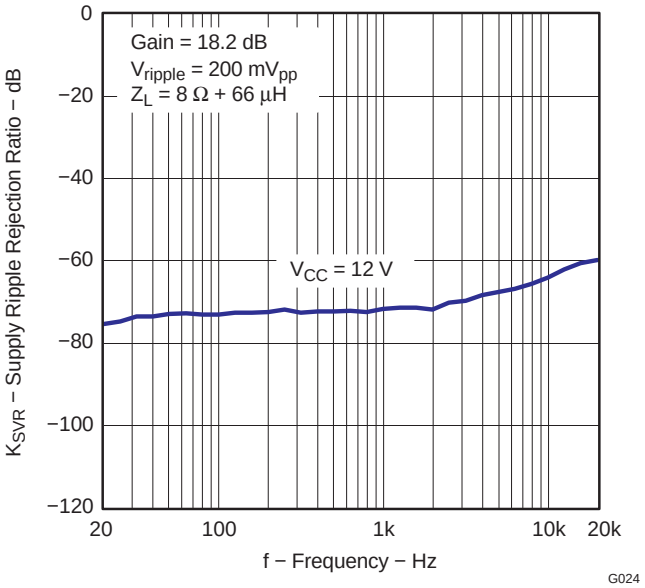


Figure 26.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY (PBTL)

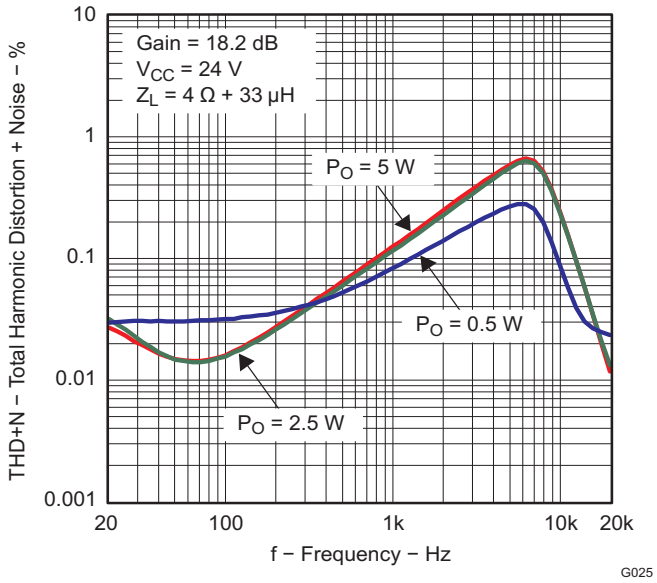


Figure 27.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER (PBTL)

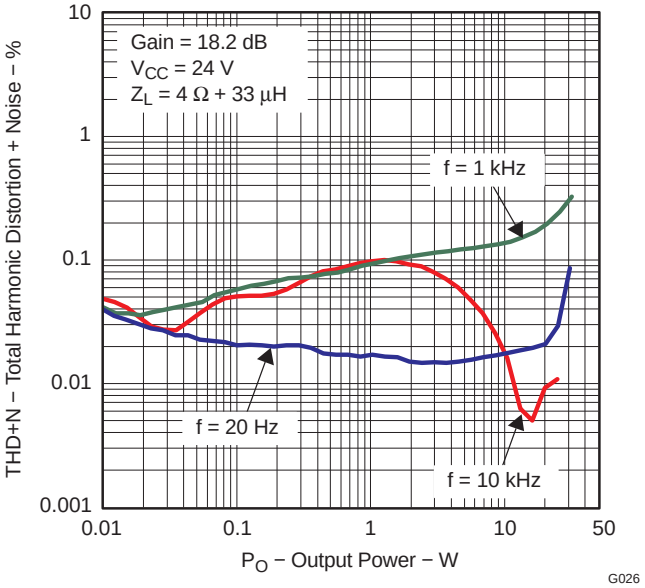
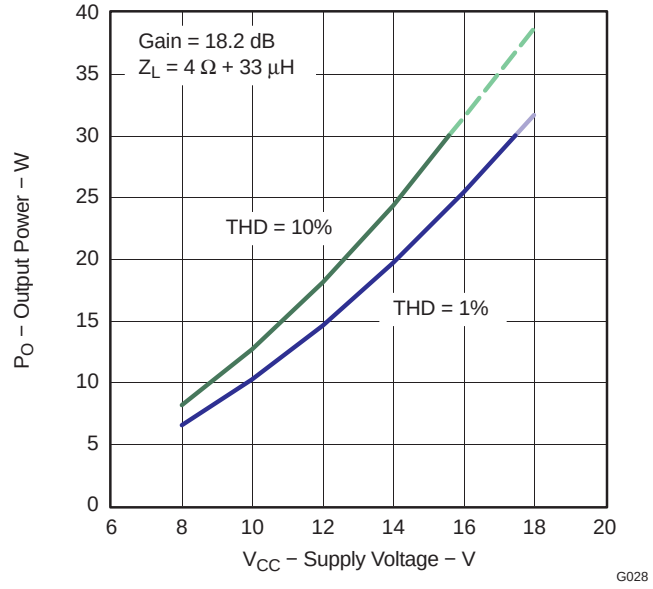


Figure 28.

OUTPUT POWER vs SUPPLY VOLTAGE (PBTL)



Note: Dashed Lines represent thermally limited regions.

Figure 29.

TYPICAL CHARACTERISTICS (continued)

(All Measurements taken at 1 kHz, unless otherwise noted. Measurements were made using the TPA3117D2 EVM which is available at ti.com.)

EFFICIENCY vs OUTPUT POWER (PBTL)

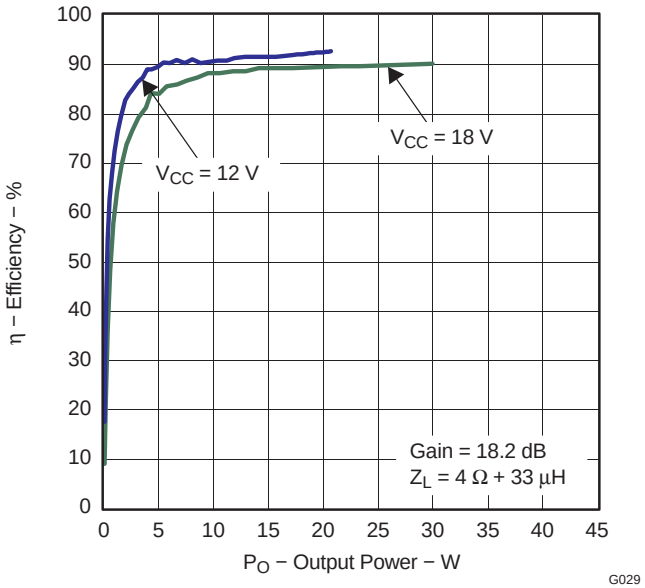


Figure 30.

SUPPLY CURRENT vs OUTPUT POWER (PBTL)

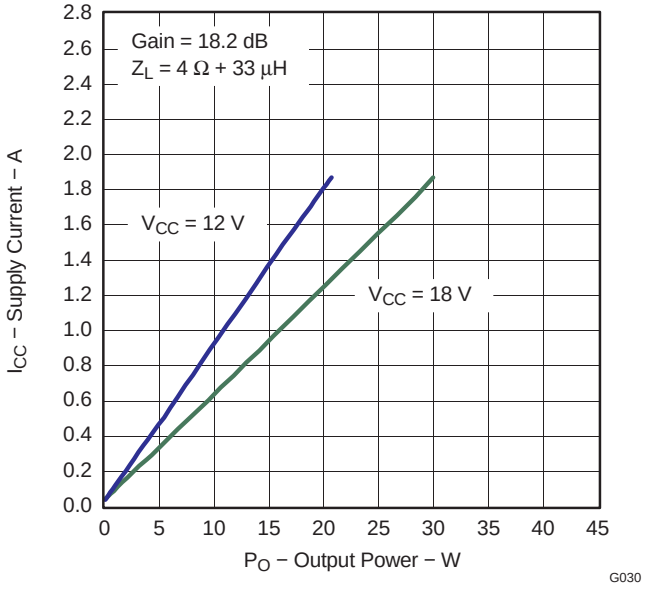


Figure 31.

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY (PBTL)

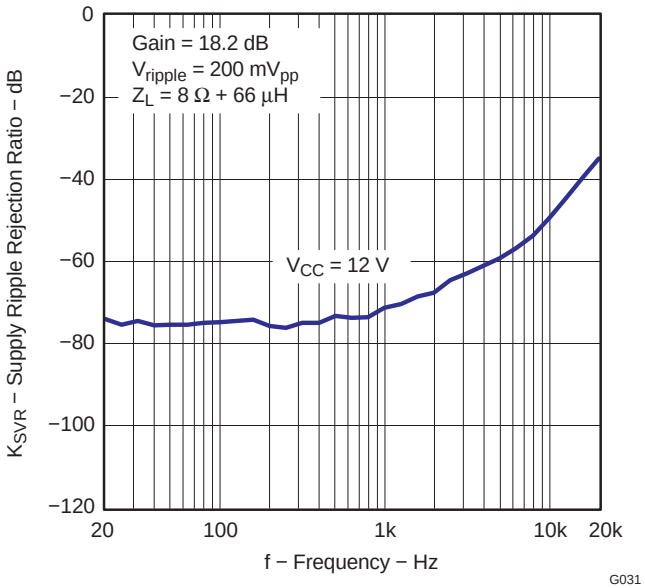


Figure 32.

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY (REG_OUT)

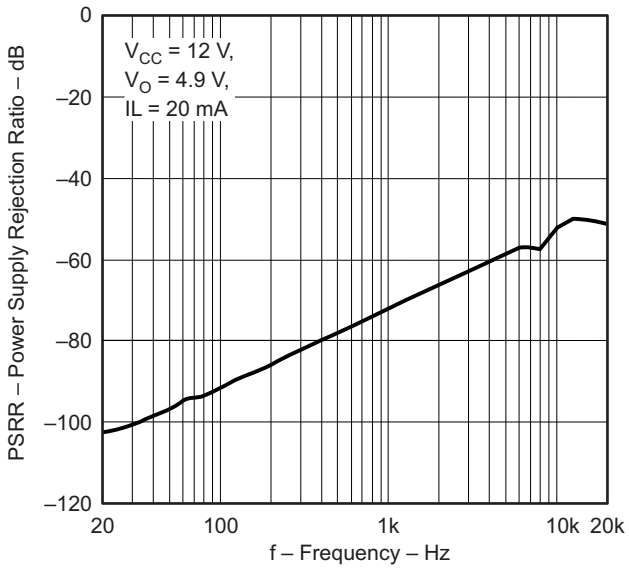


Figure 33.

DEVICE INFORMATION

Gain setting via GAIN0 and GAIN1 inputs

The gain of the TPA3117D2 is set by two input terminals, GAIN0 and GAIN1.

The gains listed in Table 1 are realized by changing the taps on the input resistors inside the amplifier. This causes the input impedance (Z_I) to be dependent on the gain setting. The actual gain settings are controlled by ratios of resistors, so the gain variation from part-to-part is small. However, the input impedance from part-to-part at the same gain may shift by ±20% due to shifts in the actual resistance of the input resistors.

For design purposes, the input network (discussed in the next section) should be designed assuming an input impedance of 60 kΩ, which is the absolute minimum input impedance of the TPA3117D2. At the lower gain settings, the input impedance could increase as high as 256 kΩ

Table 1. Gain Setting

GAIN1	GAIN0	AMPLIFIER GAIN (dB)	INPUT IMPEDANCE (kΩ)
		TYP	TYP
0	0	9	213
0	1	12.1	149
1	0	15.2	104
1	1	18.2	74

$\overline{SD}$ OPERATION

The TPA3117D2 employs a shutdown mode of operation designed to reduce supply current (I_{CC}) to the absolute minimum level during periods of nonuse for power conservation. The $\overline{SD}$ input terminal should be held high (see specification table for trip point) during normal operation when the amplifier is in use. Pulling $\overline{SD}$ low causes the outputs to mute and the amplifier to enter a low-current state. Never leave $\overline{SD}$ unconnected, because amplifier operation would be unpredictable.

For the best power-off pop performance, place the amplifier in the shutdown mode prior to removing the power supply voltage. 5V regulator (REG_OUT) is active in the shutdown state.

PLIMIT

The voltage at pin 7 can used to limit the power to levels below that which is possible based on the supply rail. Add a resistor divider from REG_OUT to ground to set the voltage at the PLIMIT pin. An external reference may also be used if tighter tolerance is required. Also add a 1μF capacitor from pin 7 to ground.

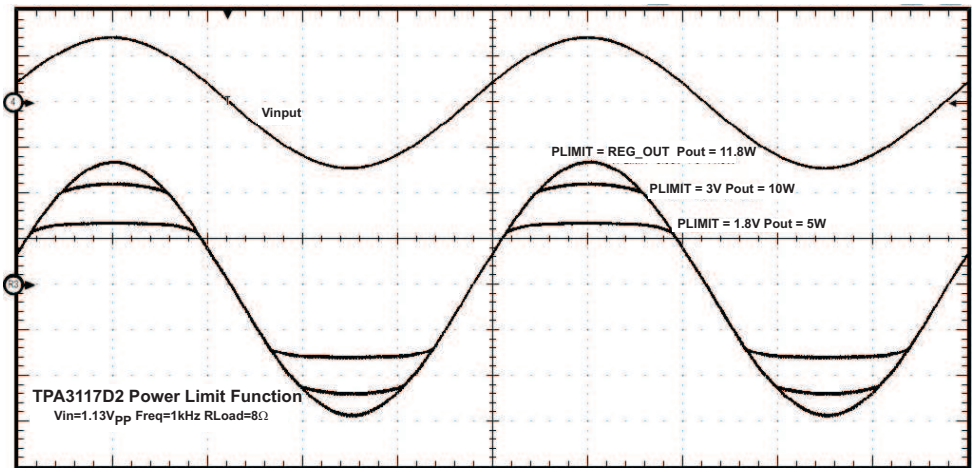


Figure 34. PLIMIT Circuit Operation

The PLIMIT circuit sets a limit on the output peak-to-peak voltage. The limiting is done by limiting the duty cycle to fixed maximum value. This limit can be thought of as a "virtual" voltage rail which is lower than the supply connected to PVCC. This "virtual" rail is 4 times the voltage at the PLIMIT pin. This output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L} \quad \text{for unclipped power} \tag{1}$$

Where:

R_S is the total series resistance including $R_{DS(on)}$, and any resistance in the output filter.

R_L is the load resistance.

V_P is the peak amplitude of the output possible within the supply rail.

V_P = 4 × PLIMIT voltage if PLIMIT < 4 × V_P

P_{OUT} (10% THD) = 1.25 × P_{OUT} (unclipped)

REG_OUT Regulator

The TPA3117D2 has an integrated 5V regulator for driving external circuitry. Maximum output current is 30mA. The regulator is always active when power is applied to the device. The $\overline{SD}$ pin does not disable operation. Connect a series 10Ω resister followed by a 2.2µF capacitor to AGND before routing to the external circuitry. When not used for powering external devices, a series 10Ω resistor with 2.2 µF of decoupling is still required.

PBTL Select

TPA3117D2 offers the feature of parallel BTL operation with two outputs of each channel connected directly. If the PBTL pin (pin 11) is tied high, the positive and negative outputs of each channel (left and right) are synchronized and in phase. To operate in this PBTL (mono) mode, apply the input signal to the RIGHT input and place the speaker between the LEFT and RIGHT outputs. Connect the positive and negative output together for best efficiency.

For normal BTL operation, connect the PBTL pin to local ground.

SHORT-CIRCUIT PROTECTION

TPA3117D2 has protection from overcurrent conditions caused by a short circuit on the output stage. Amplifier outputs are switched to a Hi-Z state when the short circuit protection latch is engaged. After a typical delay of 250ms, the outputs will resume normal operation until another short occurs. It is not necessary to cycle pin $\overline{SD}$ to restart the device operation after a short circuit event.

THERMAL PROTECTION

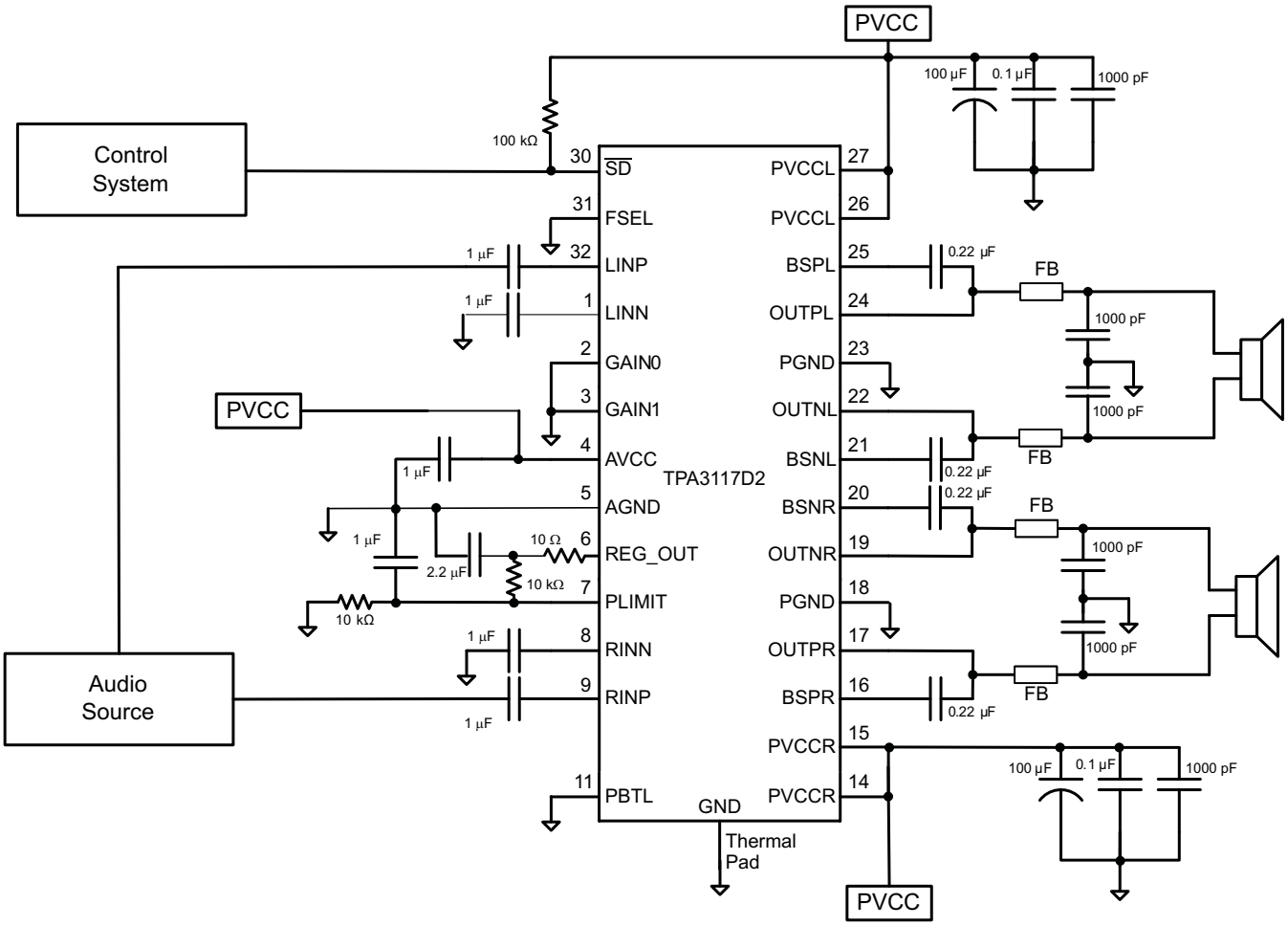
Thermal protection on the TPA3117D2 prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±15°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 15°C. The device begins normal operation at this point with no external system interaction.

It is not necessary to cycle $\overline{SD}$ terminal to restart device operation after a short circuit event.

FSEL FUNCTIONALITY

This terminal is used to select the switching frequency of the amplifier. In applications where more than one device is needed, configure one device with FSEL = LOW (290kHz switching) and the other device with FSEL = HIGH (390kHz switching).

APPLICATION INFORMATION



Note: Pins 10, 12, 13, 28 and 29 are NC (not internally connected)

Figure 35. Stereo Class-D Amplifier with BTL Output and Single-Ended Inputs

TPA3117D2 Modulation Scheme

The TPA3117D2 uses a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load. Each output is switching from 0 volts to the supply voltage. The OUTP and OUTN are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUTP is greater than 50% and OUTN is less than 50% for positive output voltages. The duty cycle of OUTP is less than 50% and OUTN is greater than 50% for negative output voltages. The voltage across the load sits at 0V throughout most of the switching period, reducing the switching current, which reduces any I^2R losses in the load.

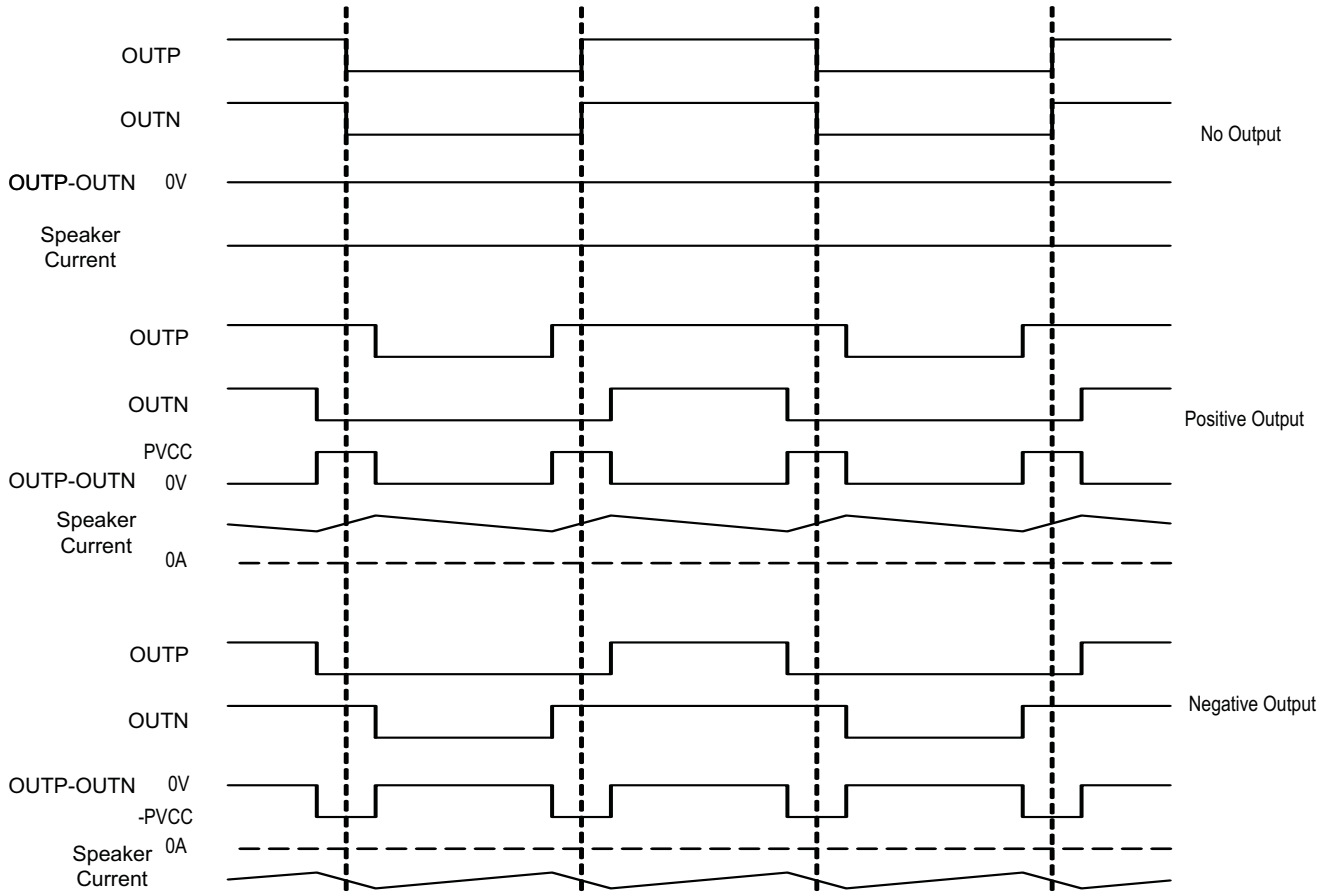


Figure 36. The TPA3117D2 Output Voltage and Current Waveforms Into an Inductive Load

Ferrite Bead Filter Considerations

Using the Advanced Emissions Suppression Technology in the TPA3117D2 amplifier it is possible to design a high efficiency Class-D audio amplifier while minimizing interference to surrounding circuits. It is also possible to accomplish this with only a low-cost ferrite bead filter. In this case it is necessary to carefully select the ferrite bead used in the filter.

One important aspect of the ferrite bead selection is the type of material used in the ferrite bead. Not all ferrite material is alike, so it is important to select a material that is effective in the 10 to 100 MHz range which is key to the operation of the Class D amplifier. Many of the specifications regulating consumer electronics have emissions limits as low as 30 MHz. It is important to use the ferrite bead filter to block radiation in the 30 MHz and above range from appearing on the speaker wires and the power supply lines which are good antennas for these signals. The impedance of the ferrite bead can be used along with a small capacitor with a value in the range of 1000 pF to reduce the frequency spectrum of the signal to an acceptable level. For best performance, the resonant frequency of the ferrite bead/ capacitor filter should be less than 10 MHz.

Also, it is important that the ferrite bead is large enough to maintain its impedance at the peak currents expected for the amplifier. Some ferrite bead manufacturers specify the bead impedance at a variety of current levels. In this case it is possible to make sure the ferrite bead maintains an adequate amount of impedance at the peak current the amplifier will see. If these specifications are not available, it is also possible to estimate the bead current handling capability by measuring the resonant frequency of the filter output at low power and at maximum power. A change of resonant frequency of less than fifty percent under this condition is desirable. Examples of ferrite beads which have been tested and work well with the TPA3117D2 include 28L0138-80R-10 and HI1812V101R-10 from Steward and the 742792510 from Wurth Electronics.

A high quality ceramic capacitor (x5R or better) is also needed for the ferrite bead filter. A low ESR capacitor with good temperature and voltage characteristics will work best.

Additional EMC improvements may be obtained by adding snubber networks from each of the class D outputs to ground. Suggested values for a simple RC series snubber network would be 10 Ω in series with a 330 pF capacitor although design of the snubber network is specific to every application and must be designed taking into account the parasitic reactance of the printed circuit board as well as the audio amp. Take care to evaluate the stress on the component in the snubber network especially if the amplifer is running at high PVCC. Also, make sure the layout of the snubber network is tight and returns directly to the PGND or the thermal pad beneath the chip.

Efficiency: LC Filter Required With the Traditional Class-D Modulation Scheme

The main reason that the traditional class-D amplifier needs an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme, because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is $2 \times V_{CC}$, and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is needed to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The TPA3117D2 modulation scheme has little loss in the load without a filter because the pulses are short and the change in voltage is V_{CC} instead of $2 \times V_{CC}$. As the output power increases, the pulses widen, making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not needed.

An LC filter with a cutoff frequency less than the class-D switching frequency allows the switching current to flow through the filter instead of the load. The filter has less resistance but higher impedance at the switching frequency than the speaker, which results in less power dissipation, therefore increasing efficiency.

When to Use an Output Filter for EMI Suppression

The TPA3117D2 has been tested with a simple ferrite bead filter for a variety of applications including long speaker wires up to 125 cm and high power. The TPA3117D2 EVM passes FCC Class B specifications under these conditions using twisted speaker wires. The size and type of ferrite bead can be selected to meet application requirements. Also, the filter capacitor can be increased if necessary with some impact on efficiency.

There may be a few circuit instances where it is necessary to add a complete LC reconstruction filter. These circumstances might occur if there are nearby circuits which are sensitive to noise. In these cases a classic second order Butterworth filter similar to those shown in the figures below can be used.

Some systems have little power supply decoupling from the AC line but are also subject to line conducted interference (LCI) regulations. These include systems powered by "wall warts" and "power bricks." In these cases, an LC reconstruction filter can be the lowest cost means to pass LCI tests. Common mode chokes using low frequency ferrite material can also be effective at preventing line conducted interference.

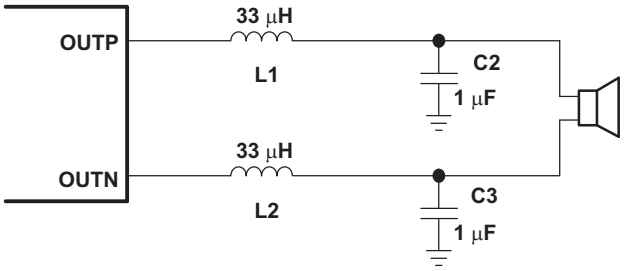


Figure 37. Typical LC Output Filter, Cutoff Frequency of 27 kHz, Speaker Impedance = 8 Ω

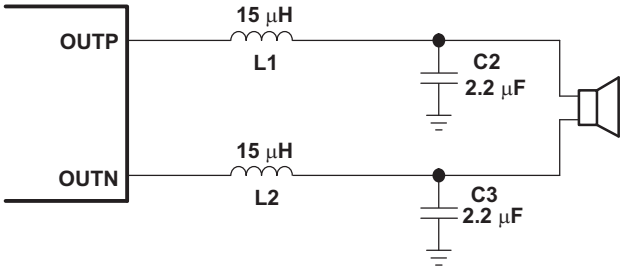


Figure 38. Typical LC Output Filter, Cutoff Frequency of 27 kHz, Speaker Impedance = 4 Ω

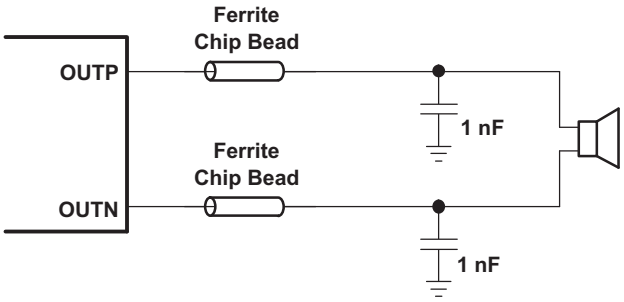
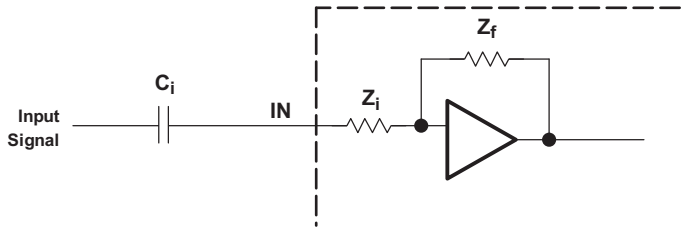


Figure 39. Typical Ferrite Chip Bead Filter (Chip Bead Example:)

INPUT RESISTANCE

Changing the gain setting can vary the input resistance of the amplifier from its smallest value, ±20%, to the largest value, ±20%. As a result, if a single capacitor is used in the input high-pass filter, the -3 dB or cutoff frequency may change when changing gain steps.



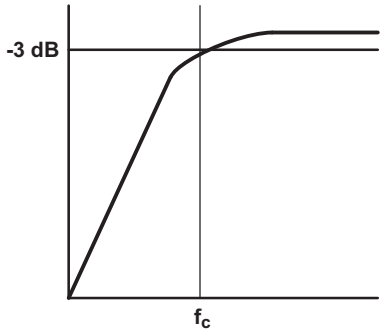
The -3-dB frequency can be calculated using Equation 2. Use the Z_I values given in Table 1.

$$f = \frac{1}{2\pi Z_i C_i} \tag{2}$$

INPUT CAPACITOR, C_I

In the typical application, an input capacitor (C_I) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and the input impedance of the amplifier (Z_I) form a high-pass filter with the corner frequency determined in Equation 3.

$$f_c = \frac{1}{2\pi Z_i C_i} \tag{3}$$



The value of C_I is important, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where Z_I is 60 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 3 is reconfigured as Equation 4.

$$C_i = \frac{1}{2\pi Z_i f_c} \tag{4}$$

In this example, C_I is 0.13 µF; so, one would likely choose a value of 0.15 µF as this value is commonly used. If the gain is known and is constant, use Z_I from Table 1 to calculate C_I. A further consideration for this capacitor is the leakage path from the input source through the input network (C_I) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at 3 V, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application. Additionally, lead-free solder can create dc offset voltages and it is important to ensure that boards are cleaned properly.

POWER SUPPLY DECOUPLING, C_S

The TPA3117D2 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. Optimum decoupling is achieved by using a network of capacitors of different types that target specific types of noise on the power supply leads. For higher frequency transients due to parasitic circuit elements such as bond wire and copper trace inductances as well as lead frame capacitance, a good quality low equivalent-series-resistance (ESR) ceramic capacitor of value between 220 pF and 1000 pF works well. This capacitor should be placed as close to the device PVCC pins and system ground (either PGND pins or PowerPad) as possible. For mid-frequency noise due to filter resonances or PWM switching transients as well as digital hash on the line, another good quality capacitor typically 0.1 μF to 1 μF placed as close as possible to the device PVCC leads works best For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 220 μF or greater placed near the audio power amplifier is recommended. The 220 μF capacitor also serves as a local storage capacitor for supplying current during large signal transients on the amplifier outputs. The PVCC terminals provide the power to the output transistors, so a 220 μF or larger capacitor should be placed on each PVCC terminal. A 10 μF capacitor on the AVCC terminal is adequate. Also, a small decoupling resistor between AVCC and PVCC can be used to keep high frequency class D noise from entering the linear input amplifiers.

BSN and BSP CAPACITORS

The full H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 0.22 μF ceramic capacitor, rated for at least 25 V, must be connected from each output to its corresponding bootstrap input. Specifically, one 0.22 μF capacitor must be connected from OUTPx to BSPx, and one 0.22 μF capacitor must be connected from OUTNx to BSNx. (See the application circuit diagram in Figure 1.)

The bootstrap capacitors connected between the BSxx pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

DIFFERENTIAL INPUTS

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the TPA3117D2 with a differential source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input. To use the TPA3117D2 with a single-ended source, ac ground the INP or INN input through a capacitor equal in value to the input capacitor on INN or INP and apply the audio source to either input. In a single-ended input application, the unused input should be ac grounded at the audio source instead of at the device input for best noise performance. For good transient performance, the impedance seen at each of the two differential inputs should be the same.

The impedance seen at the inputs should be limited to an RC time constant of 1 ms or less if possible. This is to allow the input dc blocking capacitors to become completely charged during the 14 ms power-up time. If the input capacitors are not allowed to completely charge, there will be some additional sensitivity to component matching which can result in pop if the input components are not well matched.

USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this application section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

PRINTED-CIRCUIT BOARD (PCB) LAYOUT

The TPA3117D2 can be used with a small, inexpensive ferrite bead output filter for most applications. However, since the Class-D switching edges are fast, it is necessary to take care when planning the layout of the printed circuit board. The following suggestions will help to meet EMC requirements.

- Decoupling capacitors—The high-frequency decoupling capacitors should be placed as close to the PVCC and AVCC terminals as possible. Large (220 μF or greater) bulk power supply decoupling capacitors should be placed near the TPA3117D2 on the PVCCL and PVCCR supplies. Local, high-frequency bypass capacitors should be placed as close to the PVCC pins as possible. These caps can be connected to the thermal pad directly for an excellent ground connection. Consider adding a small, good quality low ESR ceramic capacitor between 220 pF and 1000 pF and a larger mid-frequency cap of value between 0.1μF and 1μF also of good quality to the PVCC connections at each end of the chip.
- Keep the current loop from each of the outputs through the ferrite bead and the small filter cap and back to PGND as small and tight as possible. The size of this current loop determines its effectiveness as an antenna.
- Grounding—The AVCC (pin 4) decoupling capacitor should be grounded to analog ground (AGND). The PVCC decoupling capacitors should connect to PGND. Analog ground and power ground should be connected at the thermal pad, which should be used as a central ground connection or star ground for the TPA3117D2.
- Output filter—The ferrite EMI filter (Figure 39) should be placed as close to the output terminals as possible for the best EMI performance. The LC filter (Figure 37 and Figure 38) should be placed close to the outputs. The capacitors used in both the ferrite and LC filters should be grounded to power ground.
- Thermal Pad—The thermal pad must be soldered to the PCB for proper thermal performance and optimal reliability. For recommended PCB footprints, see figures at the end of this data sheet.

For an example layout, see the TPA3117D2 Evaluation Module (TPA3117D2EVM) User Manual. Both the EVM user manual and the thermal pad application report are available on the TI Web site at http://www.ti.com.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA3117D2RHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA3117	Samples
TPA3117D2RHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA3117	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

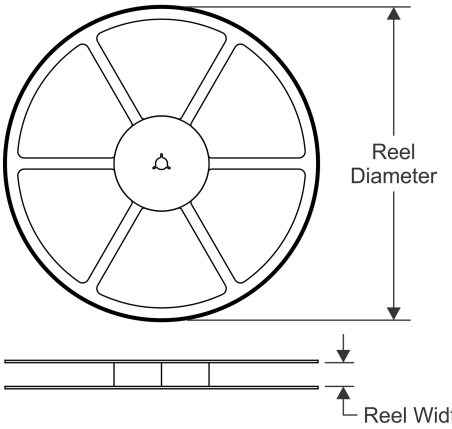
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

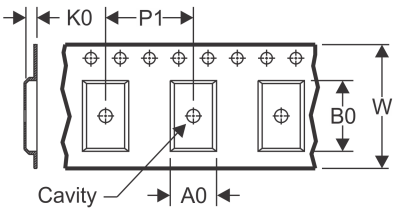
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

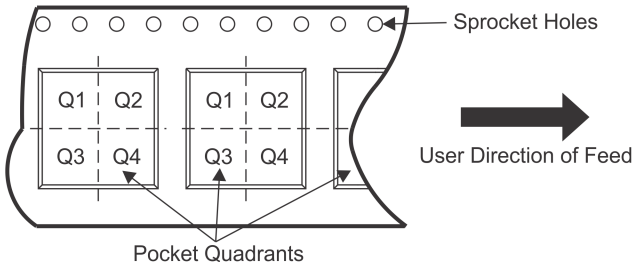


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

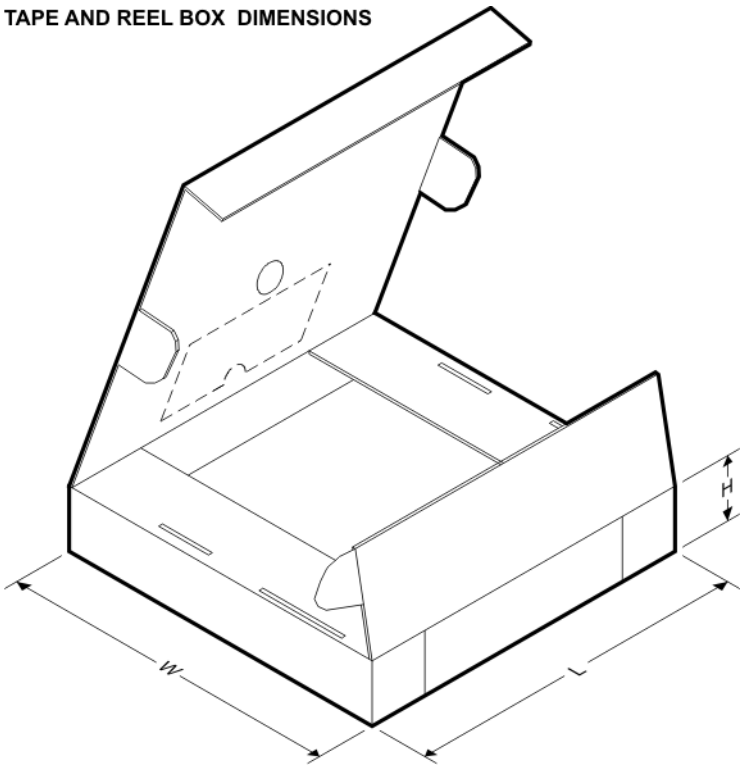
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA3117D2RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPA3117D2RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA3117D2RHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
TPA3117D2RHBT	VQFN	RHB	32	250	210.0	185.0	35.0

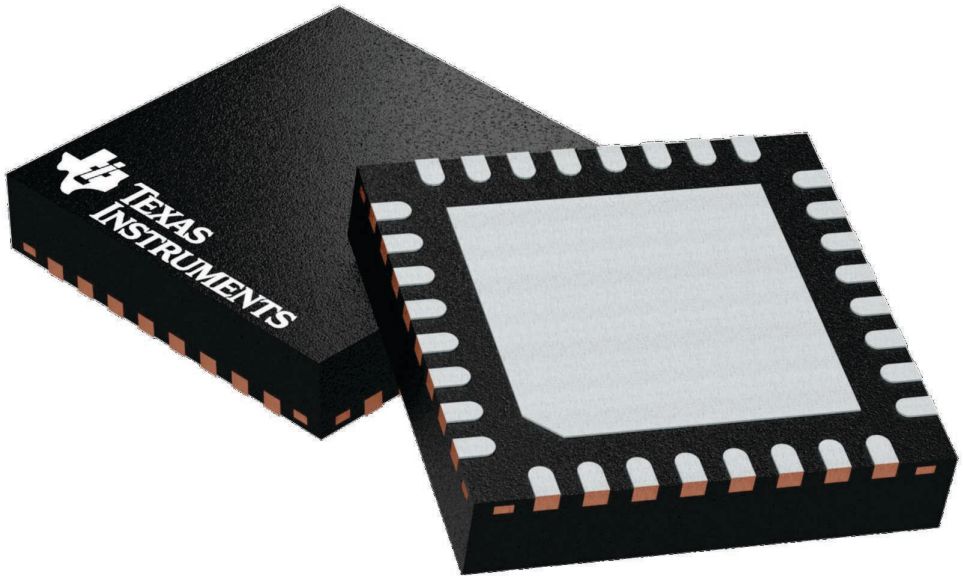
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

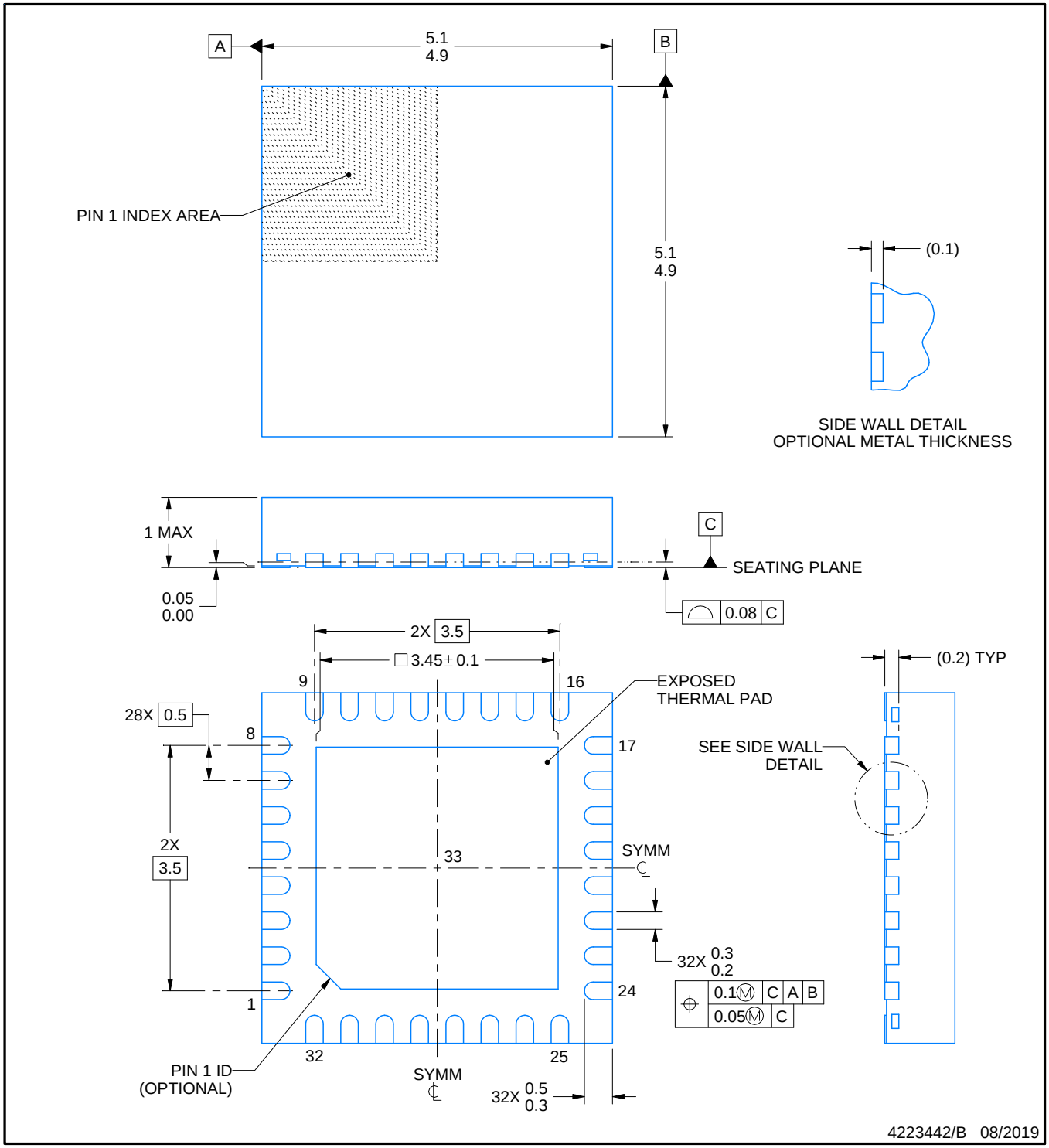
4224745/A

RHB0032E

PACKAGE OUTLINE

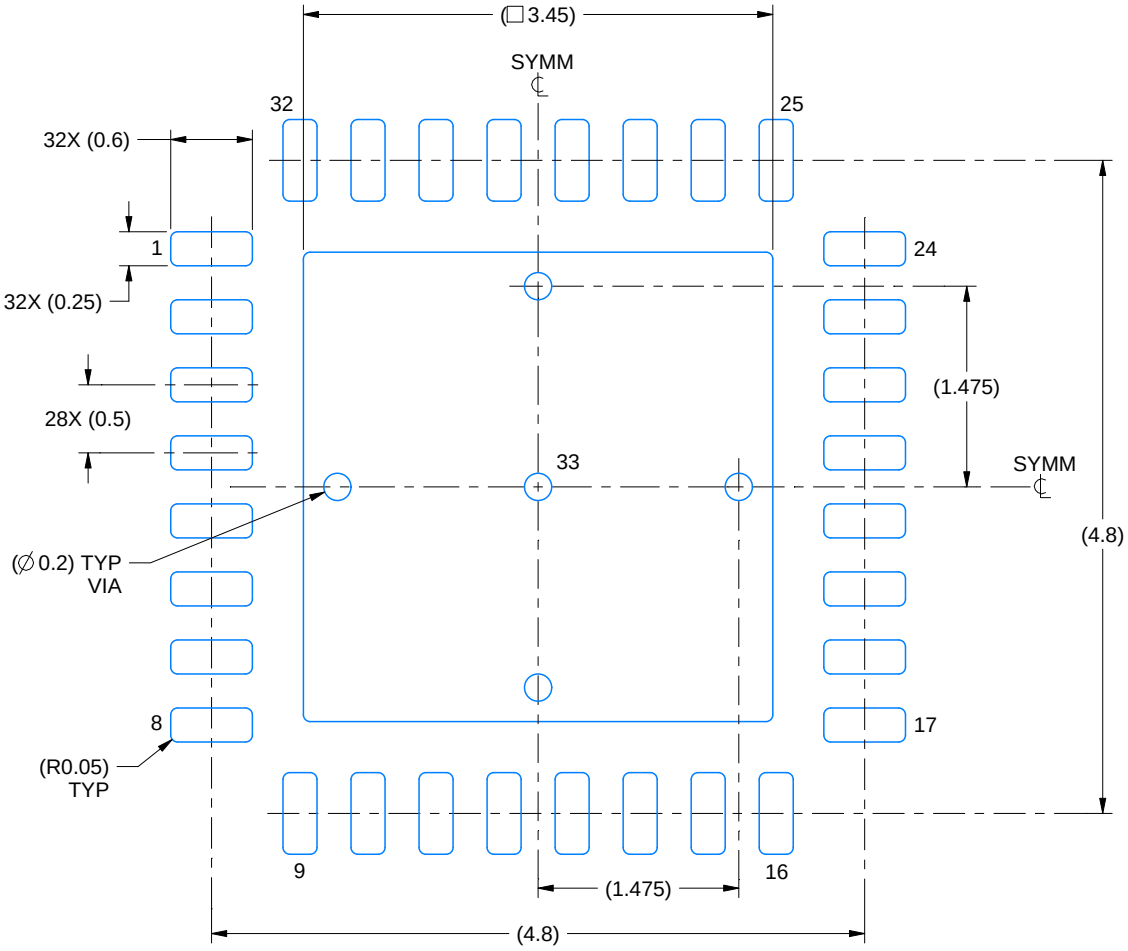
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

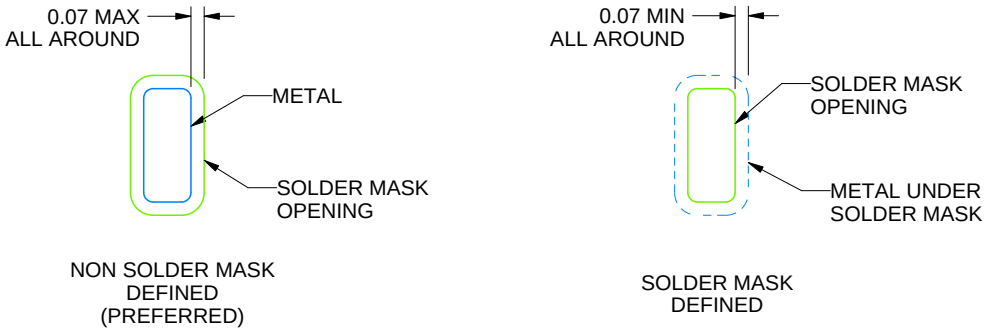


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

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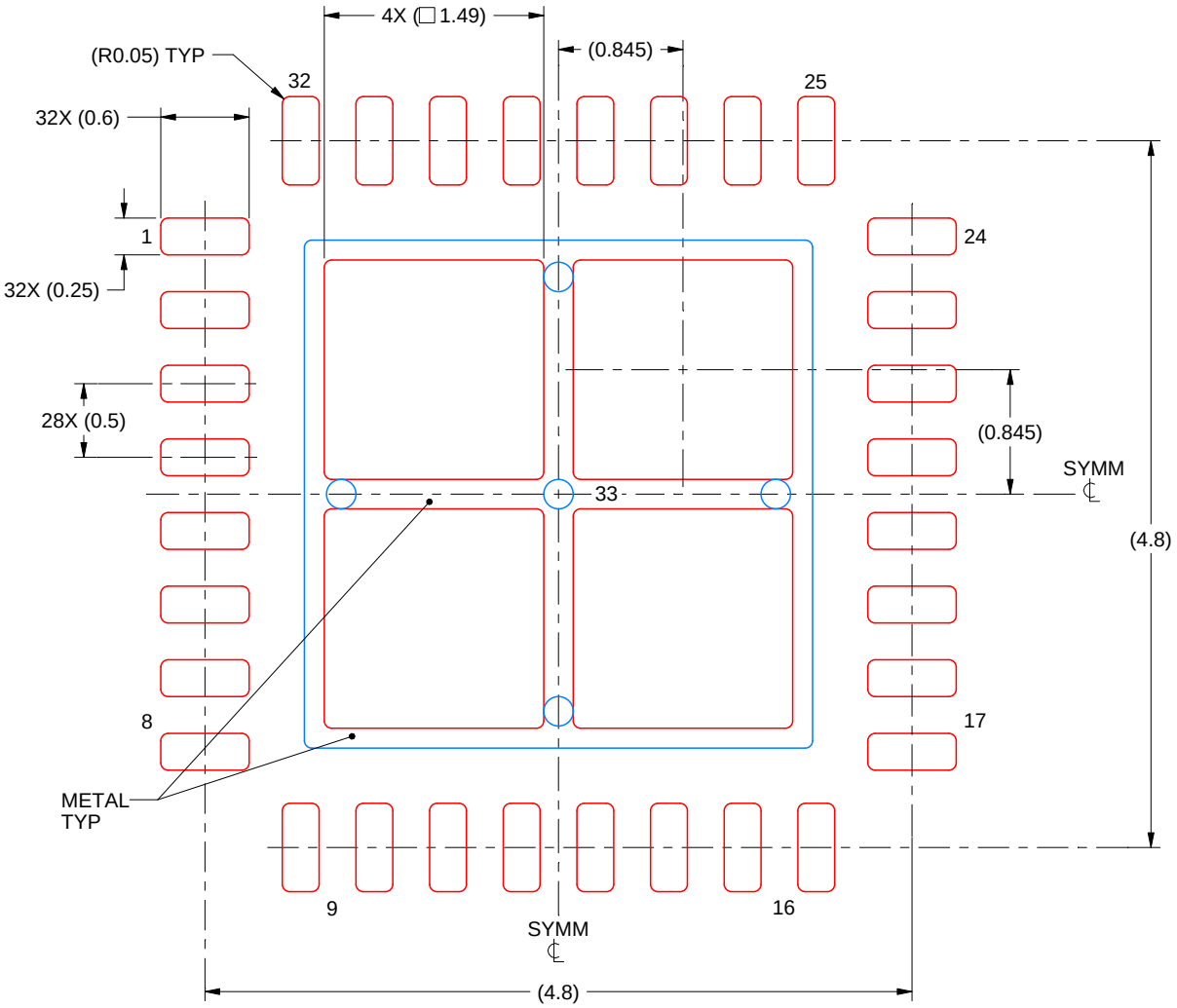
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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