



CrossLinkPlus Family

Data Sheet

FPGA-DS-02054-1.2

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
AR	Augmented Reality
ASIC	Application-Specific Integrated Circuit
CMOS	Complementary Metal Oxide Semiconductor
CSI	Camera Serial Interface
DBI	Display Bus Interface
DDR	Double Data Rate
DPI	Display Pixel Interface
DSI	Display Serial Interface
EBR	Embedded Block RAM
ECLK	Edge Clock
ESD	Electro-Static Discharge
FPGA	Field-Programmable Gate Array
FPD	Flat Panel Display
GPIO	General-Purpose Input/Output
HFOSC	High Frequency Oscillator
HISPI	High-Speed Pixel Interface
HMI	Human Machine Interface
I2C	Inter-Integrated Circuit
ISM	Industrial, Scientific, Medical
LFOSC	Low Frequency Oscillator
LUT	Look Up Table
LVC MOS	Low-Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
LVTTL	Low Voltage Transistor-Transistor Logic
MIPI	Mobile Industry Processor Interface
OpenLDI	Open LVDS Display Interface
OTP	One Time Programmable
PCLK	Primary Clock
PFU	Programmable Functional Unit
PLL	Phase Locked Loops
PMU	Power Management Unit
RAM	Random Access Memory
Rx	Receive
SDR	Single Data Rate
SLVS	Scalable Low-Voltage Signaling
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
TransFR	Transparent Field Reconfiguration
Tx	Transmit
UHD	Ultra-High-Definition, 3840 x 2160
VR	Virtual Reality

1. General Description

CrossLinkPlus™ from Lattice Semiconductor is a programmable video bridging device that supports a variety of protocols and interfaces for mobile image sensors and displays. The device is based on Lattice mobile FPGA 40-nm technology with embedded flash. It is a low power FPGA with small footprint and instant boot up time (< 10 ms).

CrossLinkPlus supports video interfaces including MIPI® DPI, MIPI DBI, CMOS camera, and display interfaces, OpenLDI, FPD-Link, FLATLINK, MIPI D-PHY, MIPI CSI-2, MIPI DSI, SLVS200, subLVDS, HiSPi, and more.

Lattice Semiconductor provides many pre-engineered Intellectual Property (IP) modules for CrossLinkPlus. By using these configurable soft-core IPs as standardized blocks, you are free to concentrate on the unique aspects of your design, increasing the productivity.

The Lattice Diamond® design software allows large complex designs to be efficiently implemented using CrossLinkPlus. Synthesis library support for CrossLinkPlus devices is available for popular logic synthesis tools. The Diamond tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the CrossLinkPlus device. The tools extract the timing from the routing and back-annotate it into the design for timing verification.

Interfaces on CrossLinkPlus provide a variety of bridging solutions for smart phone, tablets, wearables, VR, AR, Drone, Smart Home, HMI as well as adjacent ISM markets. The device is capable of supporting high-resolution, high-bandwidth content for mobile cameras and displays at UHD and beyond.

1.1. Features

- Ultra-low power
 - Sleep mode support
 - Normal Operation – from 5 mW to 150 mW
- Ultra small footprint packages
 - 64-ball ucfBGA (12 mm²)
 - 80-ball ckfBGA (49 mm²)
- Programmable architecture
 - 5936 LUTs
 - 180 kb block RAM
 - 47 kb distributed RAM
- Two hardened 4-lane MIPI D-PHY interfaces
 - Transmit and receive
 - 6 Gb/s per D-PHY interface
- Programmable source synchronous I/O
 - MIPI D-PHY Rx, LVDS Rx, LVDS Tx, subLVDS Rx, SLVS200 Rx, HiSPi Rx
 - Up to 1200 Mb/s per I/O
 - Four high-speed clock inputs
- Programmable CMOS I/O
 - LVTTTL and LVCMOS
 - 3.3 V, 2.5 V, 1.8 V and 1.2 V (outputs)
 - LVCMOS differential outputs
- Flexible device configuration
 - On-chip reconfigurable Flash
 - Master SPI boot from external flash
 - Dual image booting supported
 - I²C programming
 - SPI programming
 - TransFR™ I/O for simple field updates
- Enhanced system level support
 - Reveal logic analyzer
 - TraceID for system tracking
 - On-chip hardened I²C block
- Applications examples
 - Dual MIPI CSI-2 to Single MIPI CSI-2 Aggregation
 - Quad MIPI CSI-2 to Single MIPI CSI-2 Aggregation
 - Single MIPI DSI to Single MIPI DSI Repeater
 - Single MIPI CSI-2 to Single MIPI CSI-2 Repeater
 - Single MIPI DSI to Dual MIPI DSI Splitter
 - Single MIPI CSI-2 to Dual MIPI CSI-2 Splitter
 - MIPI DSI to OpenLDI/FPD-Link/LVDS Translator
 - OpenLDI/FPD-Link/LVDS to MIPI DSI Translator
 - MIPI DSI/CSI-2 to CMOS Translator
 - CMOS to MIPI DSI/CSI-2 Translator
 - subLVDS to MIPI CSI-2 Translator

2. Product Feature Summary

Table 2.1 lists CrossLinkPlus device information and packages.

Table 2.1. CrossLinkPlus Feature Summary

Device	CrossLinkPlus
LUTs	5936
sysMEM Blocks (9 kb)	20
Embedded Memory (kb)	180
Distributed RAM Bits (kb)	47
General Purpose PLL	1
Flash (Mb)	2
Embedded I ² C	2
Oscillator (10 kHz)	1
Oscillator (48 MHz)	1
Hardened MIPI D-PHY	2 ¹
Packages (Footprint, Pitch)	I/O
64 ucfBGA (3.5 mm × 3.5 mm, 0.4 mm)	29
80 ckfBGA (7.0 mm x 7.0 mm, 0.65 mm)	37

Note:

1. Additional D-PHY Rx interfaces are available using programmable I/O.

3. Architecture Overview

CrossLinkPlus is designed as a flexible, chip-to-chip bridging solution which supports a wide variety of applications. The device provides three key building blocks for these bridging applications:

- Two embedded Hard D-PHY blocks
- Two banks of flexible programmable I/O supporting a variety of standards including D-PHY Rx, subLVDS, SLVS200, LVDS, and CMOS
- A programmable logic core providing the LUTs, memory, and system resources to implement a wide range of bridging operations

In addition to these blocks, CrossLinkPlus also provides key system resources including a Power Management Unit, flexible configuration interface, additional CMOS GPIO, user I²C blocks, and internal Flash.

The block diagram for the device is shown in [Figure 3.1](#).

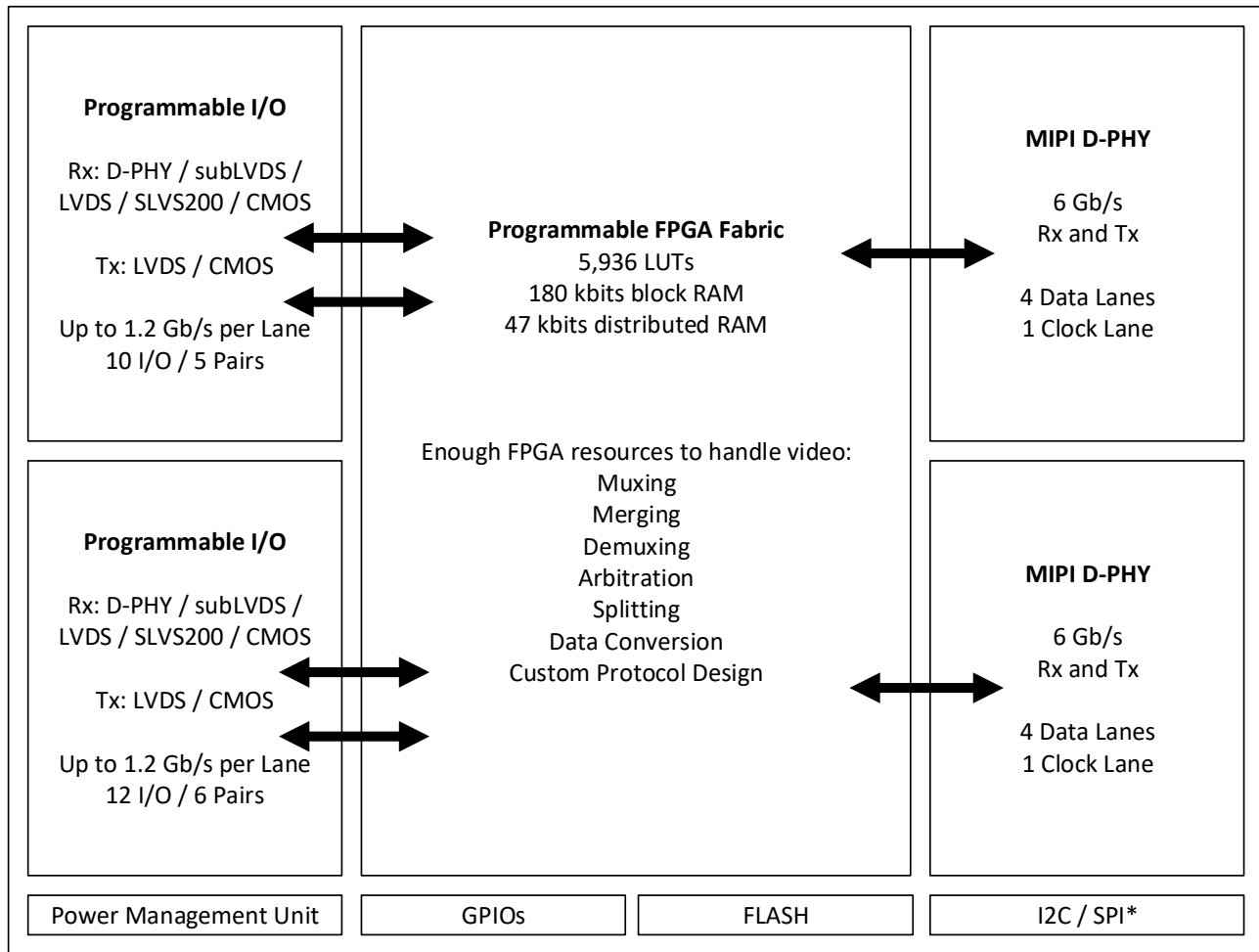


Figure 3.1. CrossLinkPlus Device Block Diagram

***Note:** I²C and SPI configuration modes are supported. User mode hardened I²C is also supported.

3.1. MIPI D-PHY Blocks

The top side of the device, as shown in [Figure 3.2](#), includes two hard MIPI D-PHY quads. The D-PHY can be configured to support both camera interface (CSI-2) and display interface (DSI) applications. Below is a summary of the features supported by the hard D-PHY quads.

- Transmit and receive compliant to MIPI Alliance Specification for D-PHY Revision 1.1
- High-Speed (HS) and Low-Power (LP) mode support (including built-in contention detect)
- Supports continuous clock mode or low power clock mode
- Up to 6 Gb/s per quad (1500 Mb/s data rate per lane)
- Dedicated PLL for Transmit Frequency Synthesis
- Dedicated Serializer and De-Serializer blocks for fabric interfacing.

Lattice Semiconductor provides a set of pre-engineered IP modules which include the full implementation and control of the hard D-PHY blocks to enable designers to focus on unique aspects of their design.

[Figure 3.3](#) to [Figure 3.6](#) show the signals connected to the fabric and the automatic settings when the hardened D-PHY is configured for the DSI/CSI-2 transmit and receive modes. Refer to [CrossLinkPlus High-Speed I/O Interface \(FPGA-TN-02102\)](#) for more information on the Hard D-PHY quads.

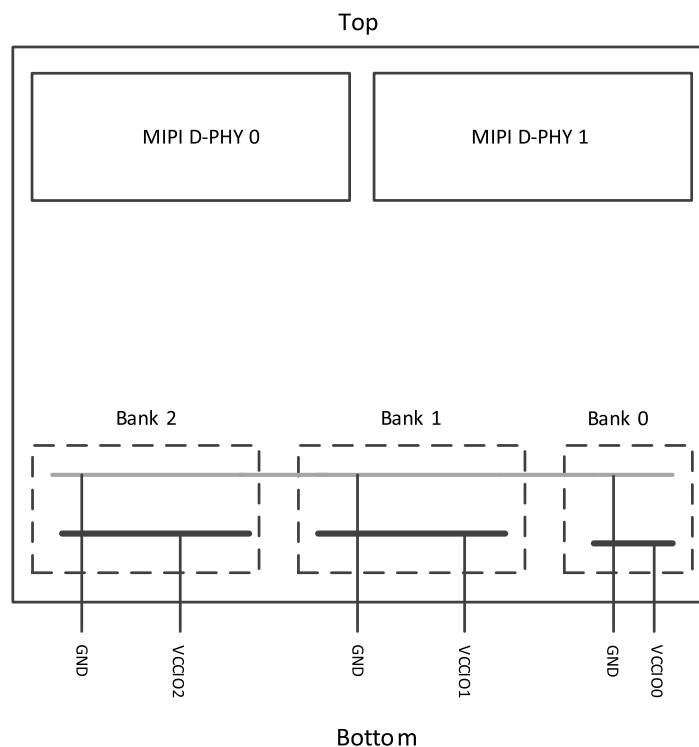


Figure 3.2. CrossLinkPlus sys/I/O Banking

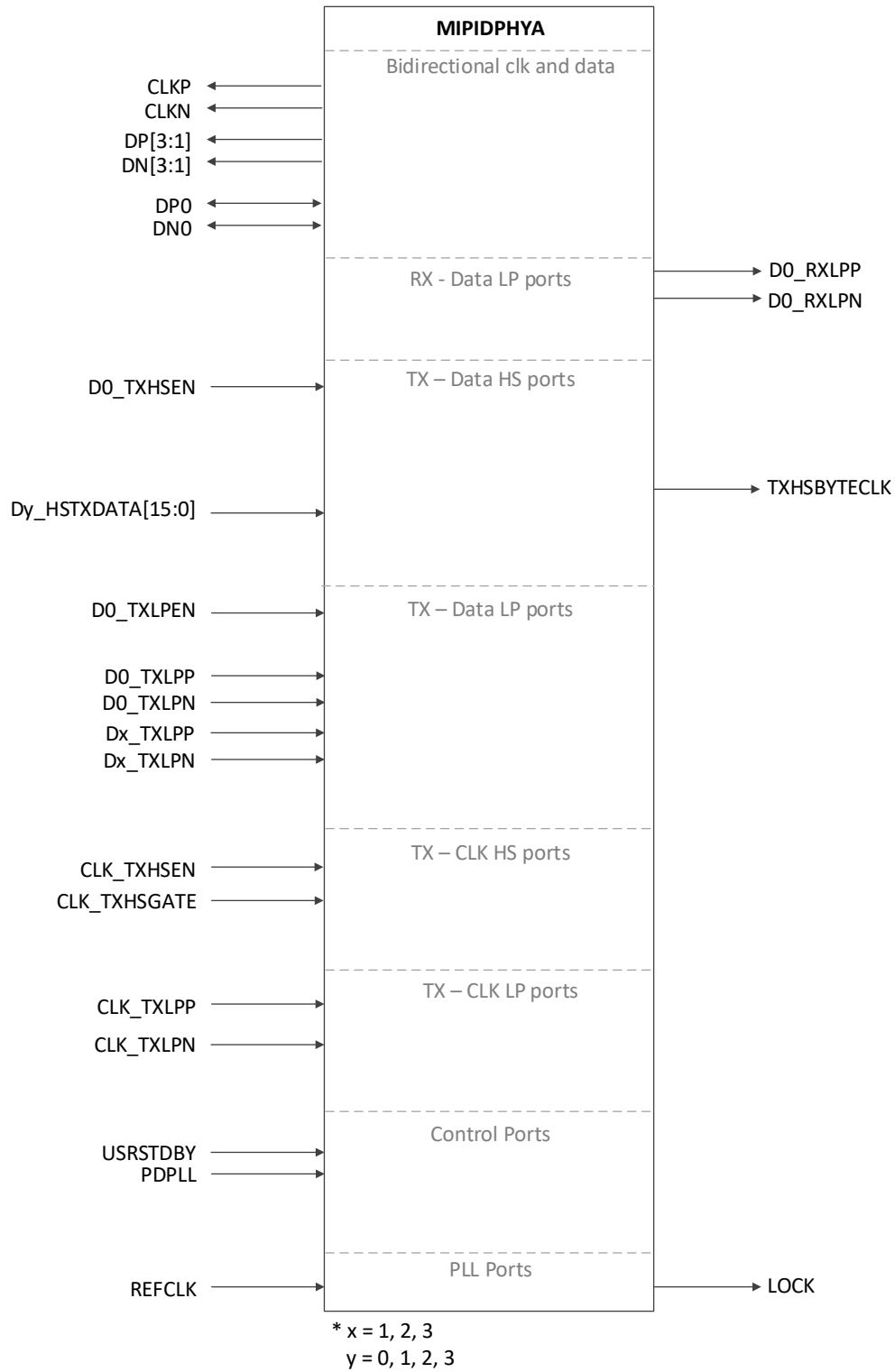


Figure 3.3. MIPI DSI Transmit Interface with Hard D-PHY Module

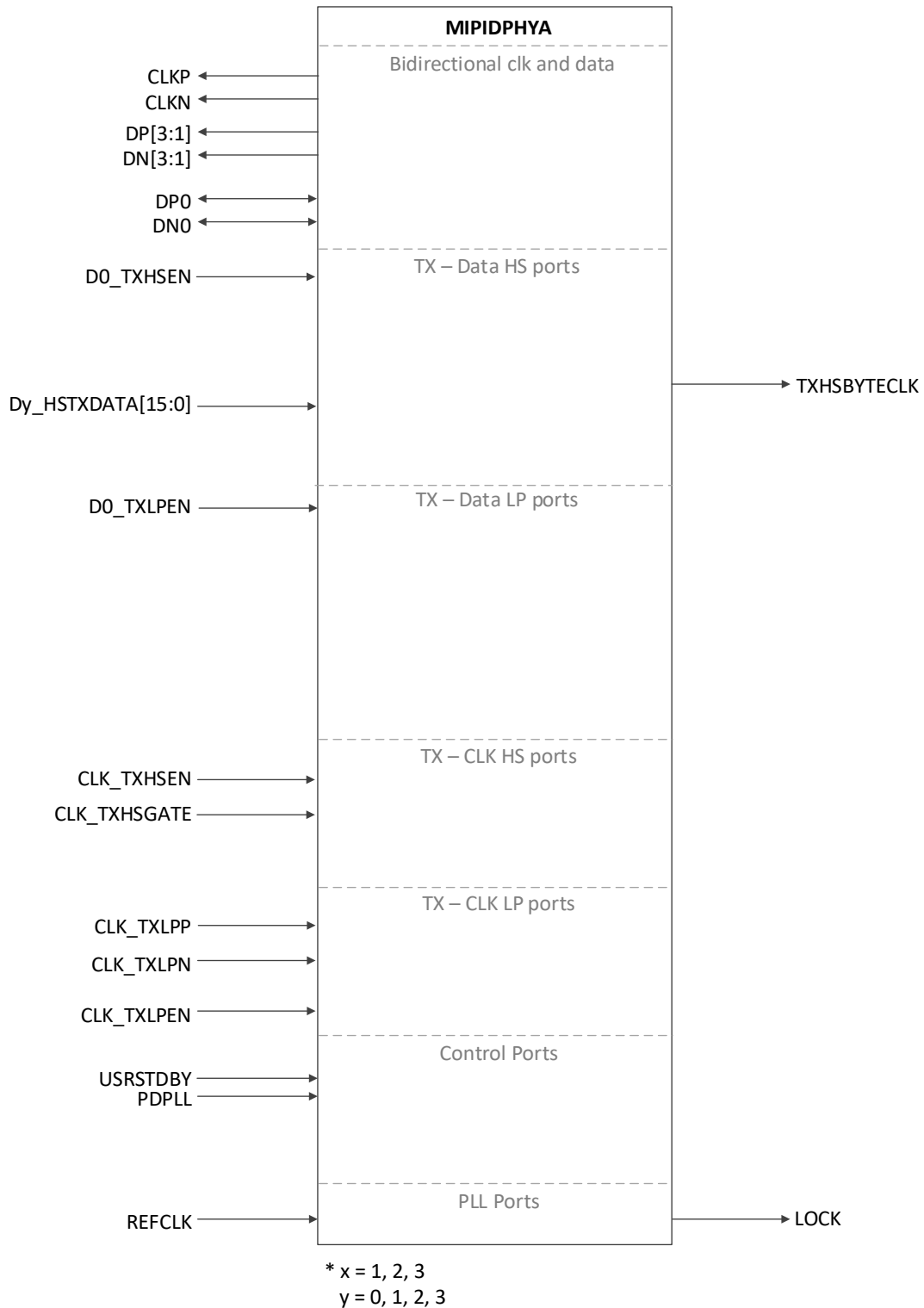


Figure 3.4. MIPI CSI-2 Transmit Interface with Hard D-PHY Module

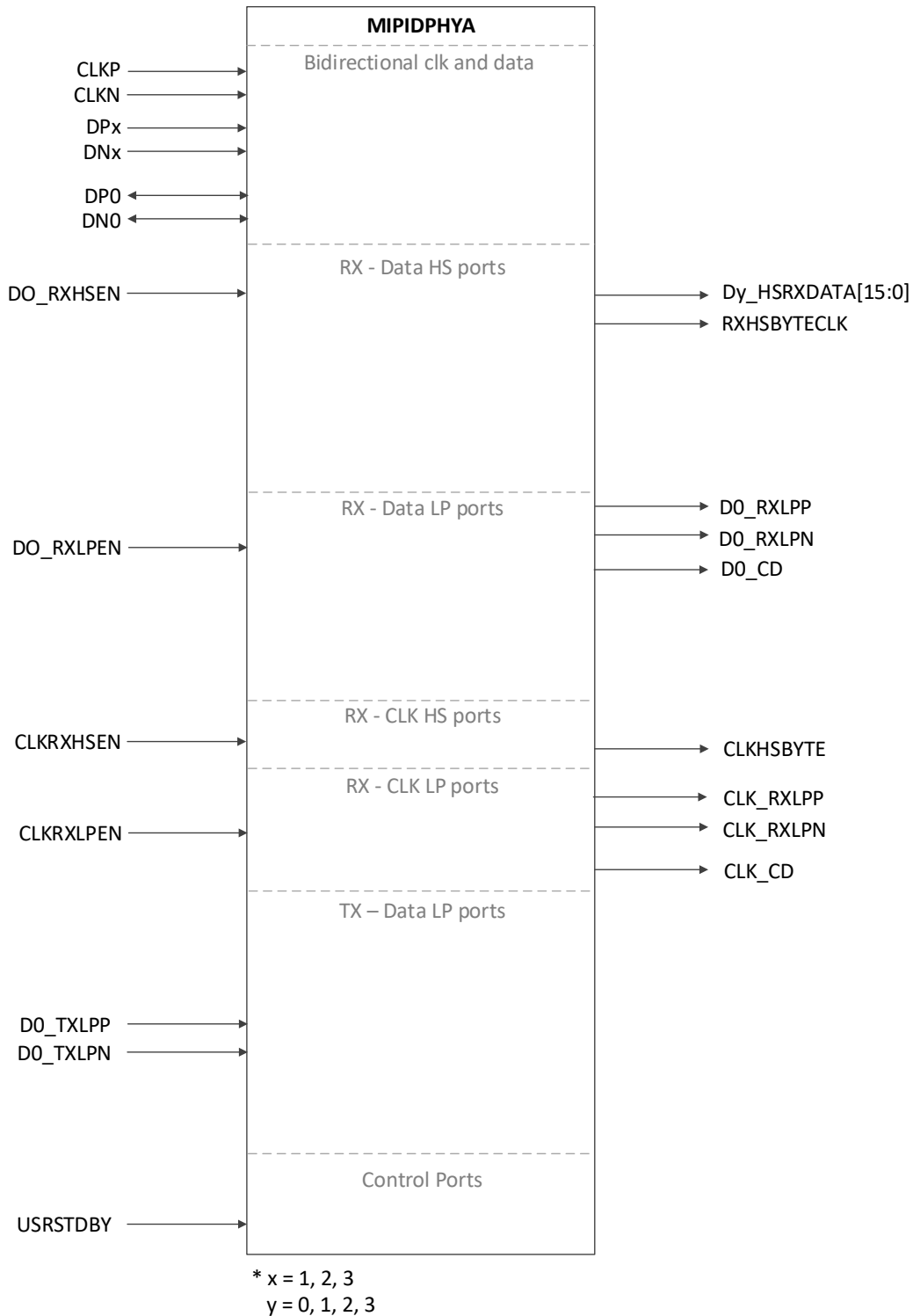


Figure 3.5. MIPI DSI Receive Interface with Hard D-PHY Module

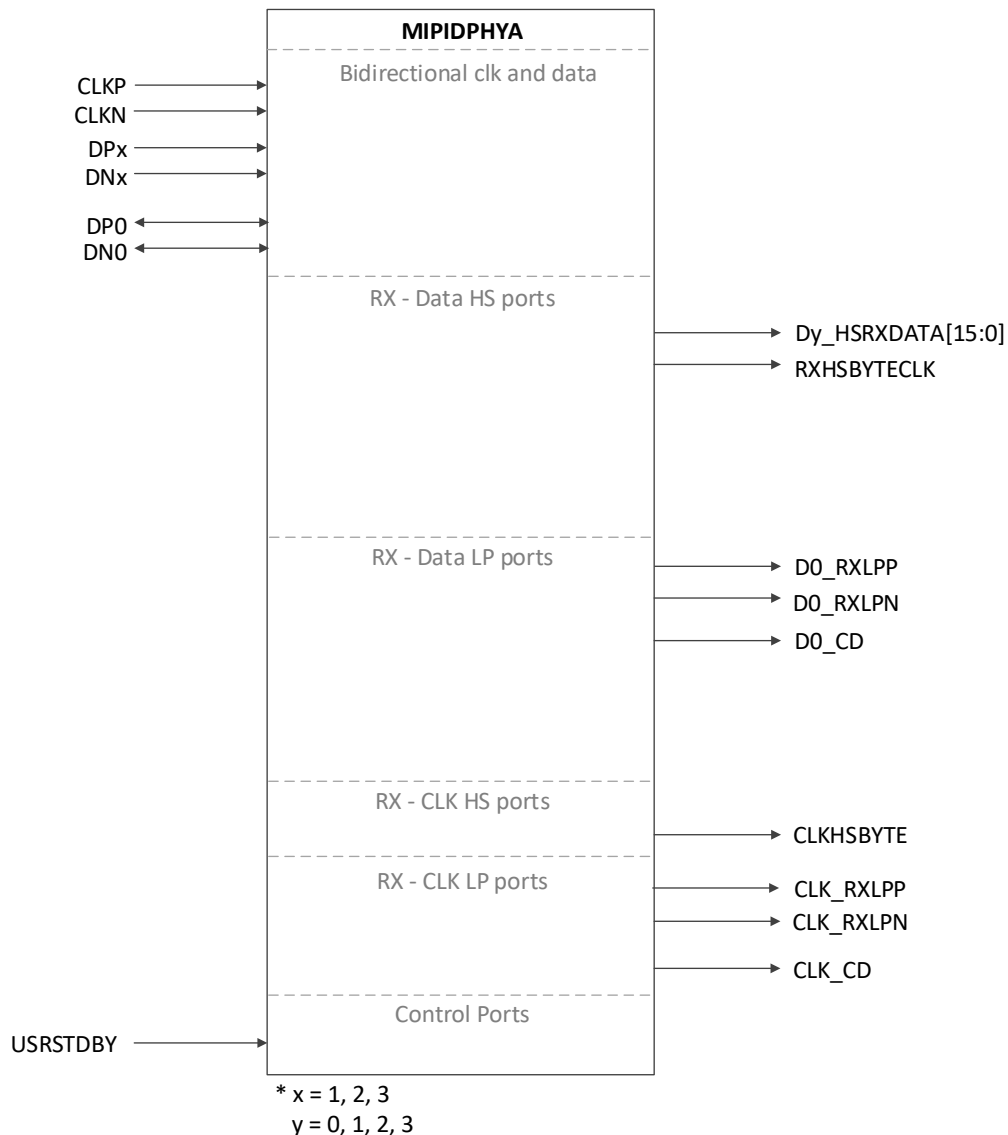


Figure 3.6. MIPI CSI-2 Receive Interface with Hard D-PHY Module

3.2. Programmable I/O Banks

CrossLinkPlus devices provide programmable I/O which can be used to interface to a variety of external standards on Banks 1 and Bank 2. CrossLinkPlus devices also provide dedicated CMOS GPIOs on Bank 0. Bank 0 GPIOs only support Single Data Rate (SDR) interfaces, while Bank 1 and Bank 2 support both SDR and Double Data Rate (DDR) interfaces. The GPIOs on Bank 0 do not include differential signaling capabilities. The location of the three Banks and their associated supplies are shown in [Figure 3.2](#).

Bank 0 features:

- Support for the following single ended standards
 - LVCMOS33
 - LVCMOS25
 - LVCMOS18
 - LVTTTL33

- Tri-state control for output
- Input/output register blocks
- Open-drain option and programmable input hysteresis
- Internal pull-up resistors with configurable values of 3.3 k Ω , 6.8 k Ω , and 10 k Ω

Bank 1 and Bank 2 features:

- Built-in support for the following differential standards
 - LVDS – Tx and Rx
 - SLVS200 – Rx
 - subLVDS – Rx
 - MIPI – Rx (both LP and HS receive on a single differential pair)
- Support for the following single ended standards
 - LVCMOS33
 - LVCMOS25
 - LVCMOS18
 - LVCMOS12 (Outputs Only)
 - LVTTTL33
- Independent voltage levels per bank based on VCCIO supply
- Input/output gearboxes per LVDS pair supporting several ratios for video interface applications
 - DDRX1, DDRX2, DDRX4, DDRX8 and DDRX71, DDRX141
 - Programmable delay cells to support edge-aligned and center-aligned interfaces
- Programmable differential termination (~ 100 Ω) with dynamic enable control
- Tri-state control for output
- Input/output register blocks
- Single-ended standards support open-drain and programmable input hysteresis
- Optional weak pull-up resistors

Table 3.1. CrossLinkPlus Output Support per Bank Basis

OUTPUT	BANK 0	BANK 1	BANK 2
LVCMOS12	—	✓	✓
LVCMOS18	✓	✓	✓
LVCMOS25	✓	✓	✓
LVCMOS33	✓	✓	✓
LVTTTL33	✓	✓	✓
LVDS25	—	✓	✓

Table 3.2. CrossLinkPlus Input Support per Bank Basis

INPUT	BANK 0	BANK 1	BANK 2
LVCMOS12	—	—	—
LVCMOS18	✓	✓	✓
LVCMOS25	✓	✓	✓
LVCMOS33	✓	✓	✓
LVTTTL33	✓	✓	✓
LVDS25	—	✓	✓
MIPI D-PHY	—	✓	✓
SLVS200	—	✓	✓
subLVDS	—	✓	✓

3.3. sysI/O Buffers

The CrossLinkPlus sysI/O buffers are distributed across three banks located at the bottom of the CrossLinkPlus device as shown in [Figure 3.2](#). The sysI/O buffers support a wide variety of standards to interface to a range of systems including LVDS, subLVDS, LVCMOS, LVTTTL, SLVS200, and MIPI. CrossLinkPlus supports single-ended buffers on all three banks. Differential I/O is supported on Bank 1 and Bank 2.

3.3.1. Programmable PULLMODE Settings

The CrossLinkPlus sysI/O buffers offer multiple programmable value pull-up resistors on the three banks. The pull-up values are programmable on a *per-pin* basis. The default state of the I/O pins prior to configuration is tri-stated with a weak pull-up to V_{CCIOx} . The I/O pins convert to the software user-defined settings after the configuration bitstream has been successfully downloaded to the device. Each sysI/O buffer can be programmed with a 100 k Ω (weak pull-up), 3.3 k Ω , 6.8 k Ω , 10 k Ω , or no pull-up. These pull-up options allow an I²C interface to be placed on the majority of the pins on the device. These options are not exclusively for I²C protocol and may be used for other functions.

3.3.2. Output Drive Strength

Each CrossLinkPlus output can have its own individual drive strength setting, but is predefined based on the V_{CCIOx} setting. [Table 3.3](#) lists the drive settings for the corresponding I/O type.

Table 3.3. Drive Strength Values

VCCIOx (V)	I/O Type	Drive Strength (mA)
3.3	LVTTTL33	8
3.3	LVCMOS33	8
2.5	LVCMOS25	6
1.8	LVCMOS18	4
1.2	LVCMOS12	2

3.3.3. On-Chip Termination

Bank 1 and Bank 2 of CrossLinkPlus support LVDS, SLVS200 subLVDS and MIPI D-PHY inputs. These two banks support on-chip 100 Ω input differential termination between LVDS, SLVS200, and subLVDS pairs. For MIPI D-PHY inputs, the on-chip 100 Ω termination is dynamically enabled based on the High Speed Select (HSSEL) signal.

Refer to the [CrossLinkPlus High-Speed I/O Interface \(FPGA-TN-02102\)](#) and [CrossLinkPlus sysI/O Usage Guide \(FPGA-TN-02108\)](#) for details.

3.4. Programmable FPGA Fabric

CrossLinkPlus is built around a programmable logic fabric consisting of 5936 four input lookup tables (LUT4) arranged alongside dedicated registers in Programmable Functional Units (PFU). These PFU blocks are the building blocks for logic, arithmetic, RAM, and ROM functions. The PFU blocks are connected via a programmable routing network. The Lattice Diamond design software configures the PFU blocks and the programmable routing for each unique design. Interspersed between rows of PFU are rows of sysMEM™ Embedded Block RAM (EBR), with programmable I/O banks, embedded I²C and embedded MIPI D-PHY arranged on the top and bottom of the device as shown in Figure 3.7.

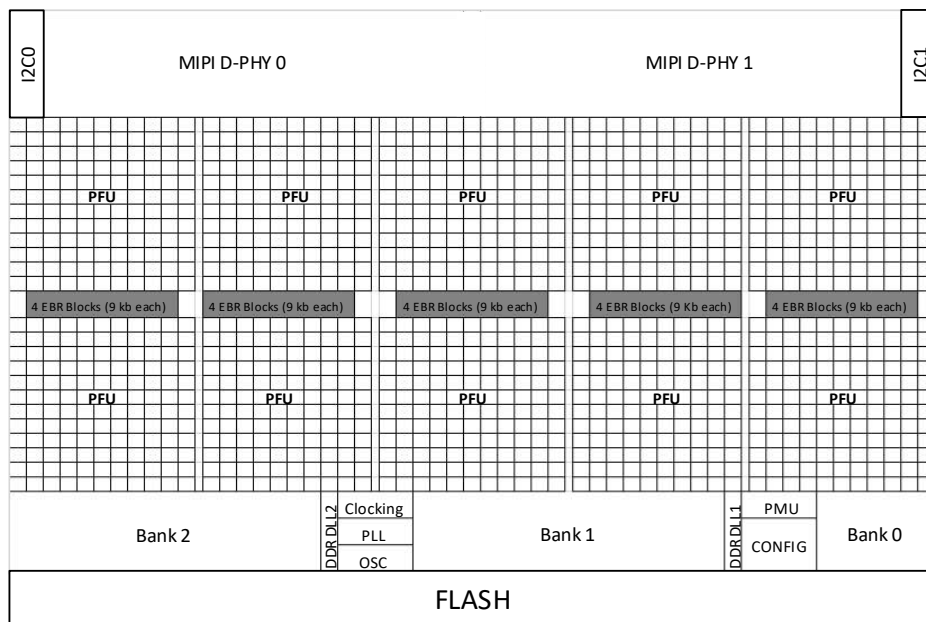


Figure 3.7. CrossLinkPlus Device Simplified Block Diagram (Top Level)

3.4.1. PFU Blocks

The core of the CrossLinkPlus device consists of PFU blocks. Each PFU block consists of four interconnected slices numbered 0–3 as shown in Figure 3.8. Each slice contains two LUTs. All the interconnections to and from PFU blocks are from routing. The PFU block can be used in Distributed RAM or ROM function, or used to perform Logic, Arithmetic, or ROM functions.

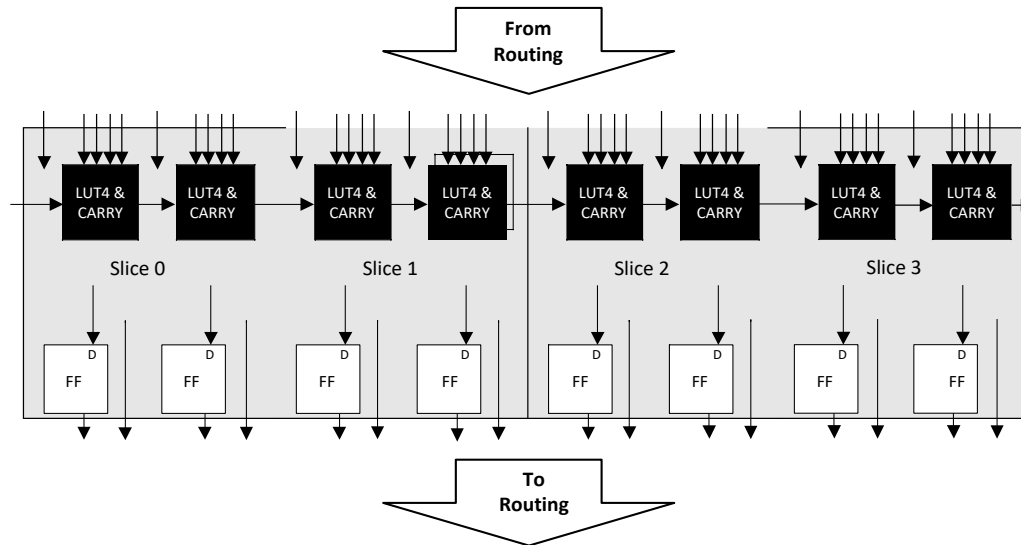
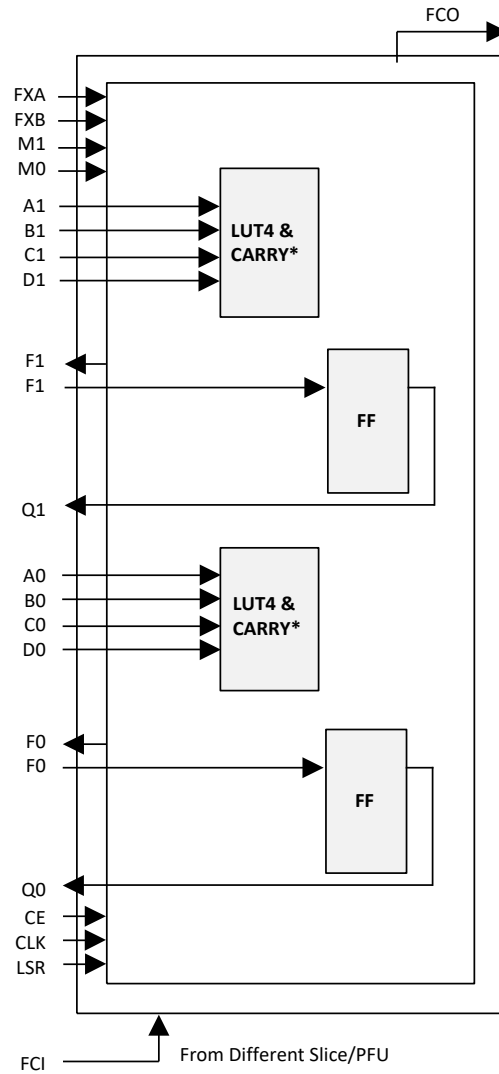


Figure 3.8. CrossLinkPlus PFU Diagram

3.4.2. Slice

Each slice contains two LUT4s feeding two registers. Each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7, and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select, and wider RAM/ROM functions. [Figure 3.9](#) shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks.

Each slice has 14 input signals: 13 signals from routing and 1 signal from the carry-chain routed from the adjacent slice or PFU. There are five outputs: four to routing and one to carry-chain (to the adjacent PFU). There are two inter slice/PFU output signals that are used to support wider LUT functions, such as LUT6, LUT7, and LUT8. [Table 3.4](#) and [Figure 3.10](#) list the signals associated with all the slices. [Figure 3.8](#) shows the connectivity of the inter-slice/PFU signals that support LUT5, LUT6, LUT7, and LUT8.



Notes: For Slices 0 and 1, memory control signals are generated from Slice 2 as follows:
 WCK is CLK
 WRE is from LSR
 DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2
 WAD [A:D] is a 4-bit address from slice 2 LUT input

Figure 3.9. Slice Diagram

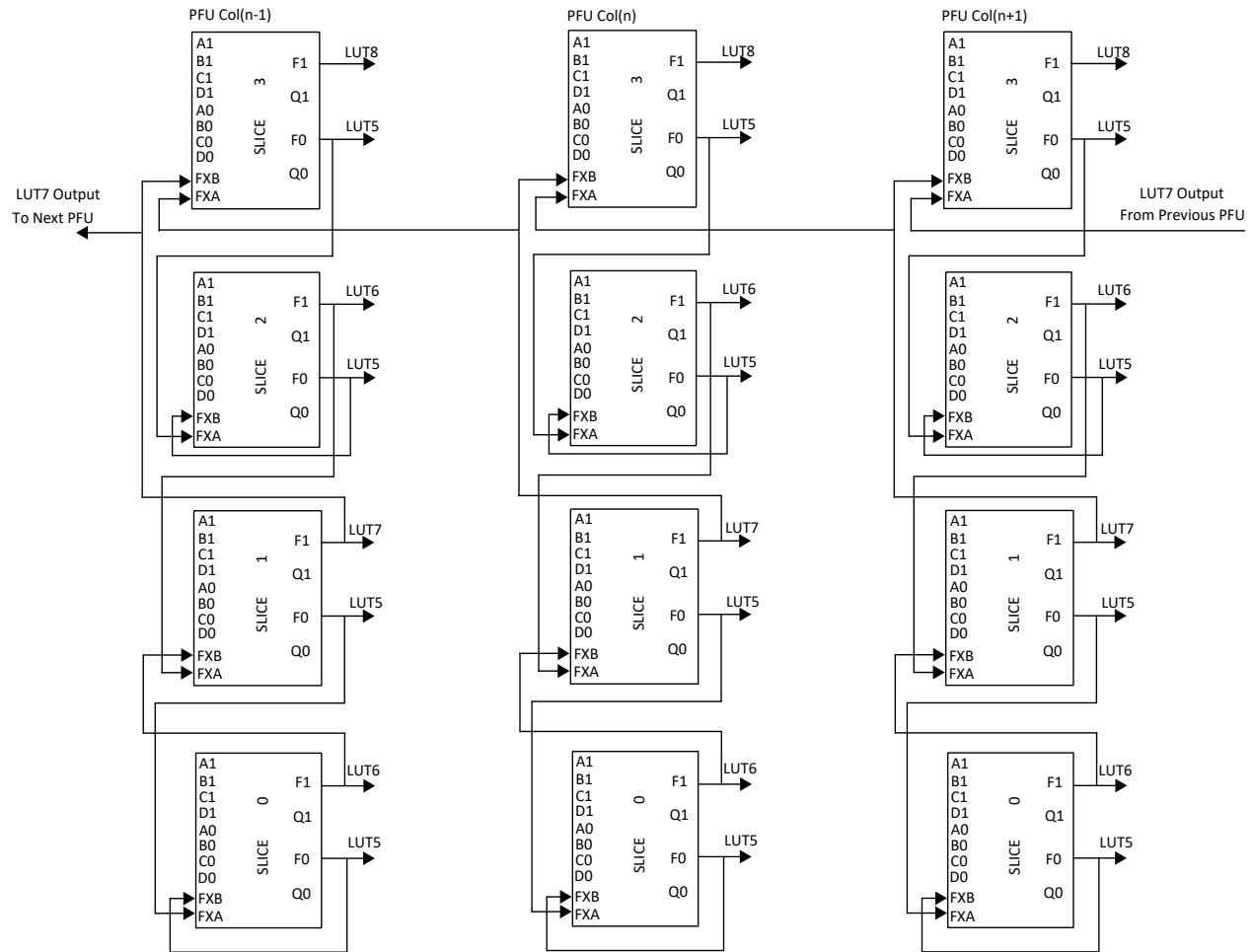


Figure 3.10. Connectivity Supporting LUT5, LUT6, LUT7, and LUT8

Table 3.4. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCI	Fast Carry-in ¹
Input	Inter-slice signal	FXA	Intermediate signal to generate LUT6, LUT7 and LUT8 ²
Input	Inter-slice signal	FXB	Intermediate signal to generate LUT6, LUT7 and LUT8 ²
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Inter-PFU signal	FCO	Fast carry chain output ¹

Notes:

1. See Figure 3.9 for connection details.
2. Requires two adjacent PFUs.

3.5. Clocking Structure

The CrossLinkPlus device family provides resources to support a wide range of clocking requirements for programmable video bridging. These resources are described below. For details, refer to [CrossLinkPlus sysCLOCK PLL/DLL Design and Usage Guide \(FPGA-TN-02109\)](#).

3.5.1. sysCLK PLL

The CrossLinkPlus sysCLK PLL provides the ability to synthesize clock frequencies. See [Table 4.14](#) for input frequency range. The PLL provides features such as dynamic selectable clock input, clock injection delay removal, independent dynamic output enable control, and programmable output phase adjustment. The architecture of the PLL is shown in [Figure 3.11](#).

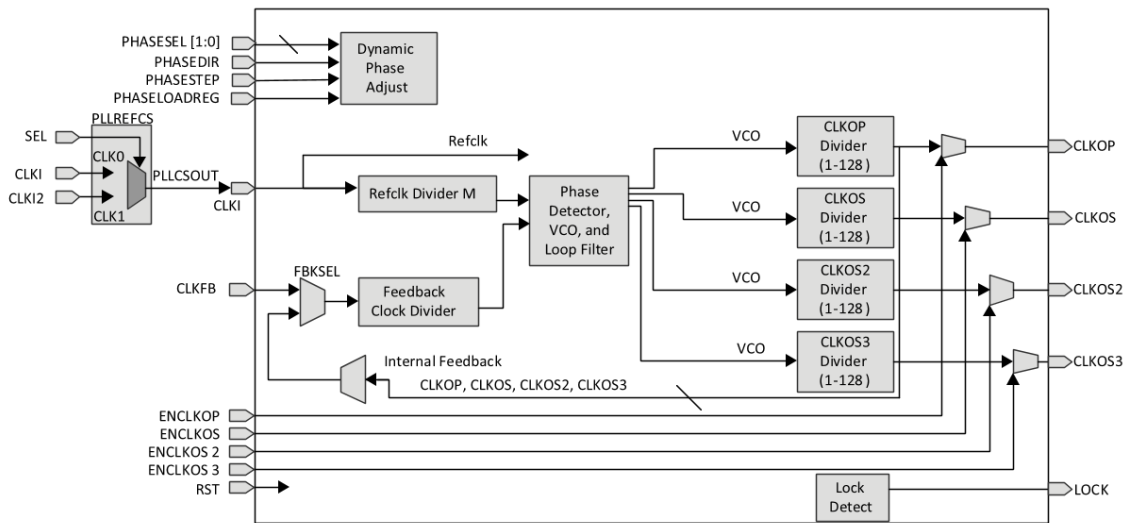


Figure 3.11. CrossLinkPlus PLL Block Diagram

Table 3.5 provides a description of the signals in the PLL block.

Table 3.5. CrossLinkPlus PLL Port Definition

Signal	I/O	Description
CLKI	I	Input clock to PLL
CLKFB	I	Feedback clock
USRSTDBY	I	User port to put the PLL to sleep mode
PHASESEL[1:0]	I	Select the output affected by Dynamic Phase adjustment
PHASEDIR	I	Dynamic phase adjustment direction
PHASESTEP	I	Dynamic phase adjustment step
PHASELOADREG	I	Load dynamic phase adjustment values into PLL
RST	I	Resets the whole PLL
ENCLKOP	I	Enable PLL output CLKOP
ENCLKOS	I	Enable PLL output CLKOS
ENCLKOS2	I	Enable PLL output CLKOS2
ENCLKOS3	I	Enable PLL output CLKOS3
PLLWAKESYNC	I	Enable PLL switching from internal to user feedback path when PLL wake up
CLKOP	O	PLL main output clock
CLKOS	O	PLL output clock
CLKOS2	O	PLL output clock
CLKOS3	O	PLL output clock
LOCK	O	PLL LOCK to CLKI, asynchronous signal. Active high indicates PLL lock

3.5.2. Primary Clocks

The primary clock routing network is made up of low skew clock routing resources with connectivity to every synchronous element of the device. Primary clock sources are selected in the center mux and distributed on the primary clock routing to clock the synchronous elements in the FPGA fabric. CrossLinkPlus family of devices provide up to eight unique global primary clocks. Primary clock sources are:

- LVDS PIO pins
- GPIO pins
- PLL outputs
- Clock dividers
- Fabric internally generated clock signal
- Divided down clock from DPHY
- OSCI
- The routing clock structure is shown in [Figure 3.12](#).

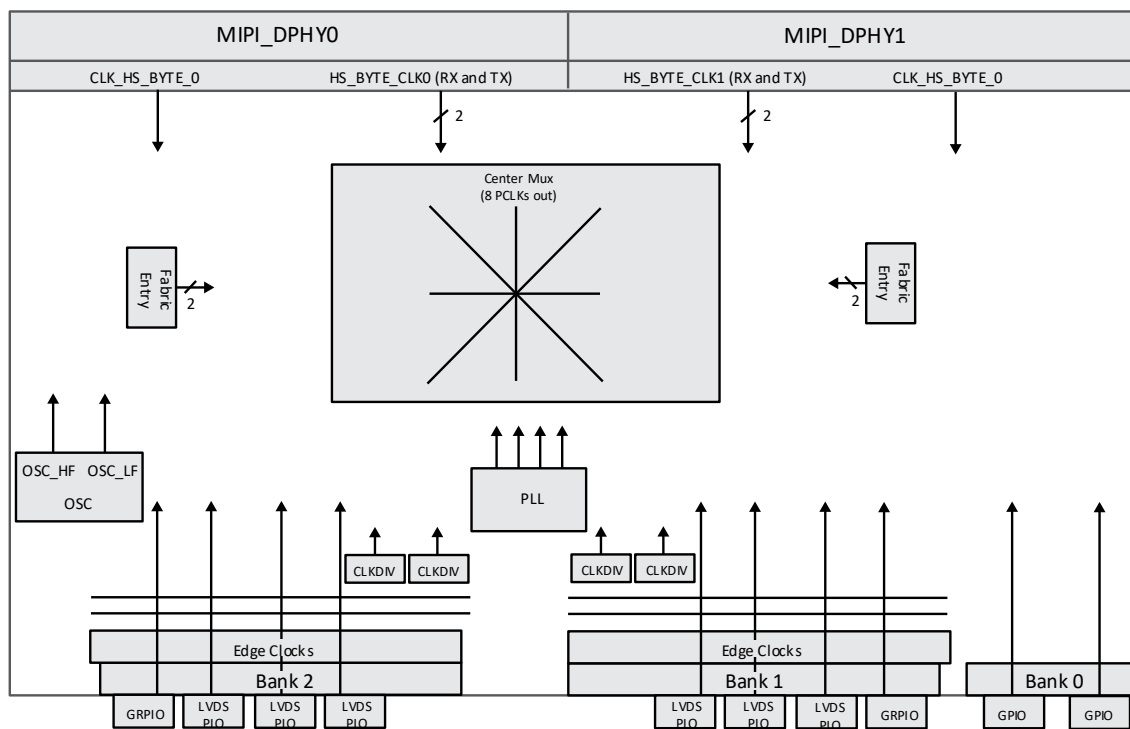


Figure 3.12. CrossLinkPlus Clocking Structure

3.5.3. Edge Clocks

The CrossLinkPlus device has Edge Clocks (ECLK) at the bottom two banks (Bank 1 and Bank 2) of the device ([Figure 3.12](#)). The CrossLinkPlus device has two edge clocks per Programmable I/O bank. These clocks, which have low injection time and skew, are used to clock I/O registers. Edge clock resources are designed for high speed I/O interfaces with high fan-out capability. The sources of edge clocks are:

- Dedicated Clock (PCLK) pins muxed with the DLLDEL output
- PLL outputs (CLKOP and CLKOS)
- Internal nodes

ECLK input MUX collects all clock sources as shown in [Figure 3.13](#) below. There are two ECLK Input MUXs, one on each bank. It drives the ECLK SYNC modules and the ECLK Clock Divider through a 2 to 1 MUX.

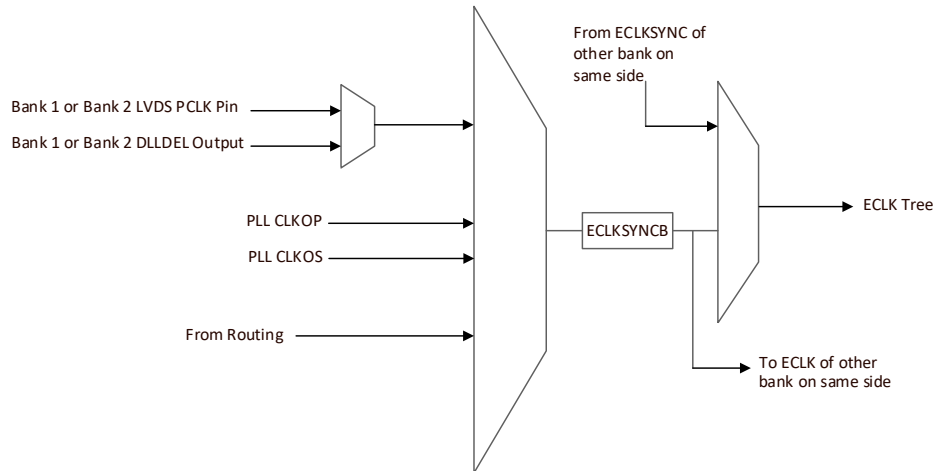


Figure 3.13. CrossLinkPlus Edge Clock Sources per Bank

3.5.4. Dynamic Clock Enables

Each PLL output has a user input signal to dynamically enable/disable its output to provide a glitch free clock. When the clock enable signal is set to logic 0, the corresponding output clock is held to logic 0. This allows you to save power by stopping the corresponding output clock when not in use.

3.5.5. Internal Oscillator (OSCI)

The OSCI element performs multiple functions on the CrossLinkPlus device. It is used for configuration and available during user mode. OSCI element has the following features in user mode:

- Always-on low frequency clock output (LFCLKOUT) with nominal frequency of 10 kHz
- High-frequency clock output (HFCLKOUT) with nominal frequency of 48 MHz that can be enabled or disabled using HFOUTEN input
- Programmable output dividers (HFCLKDIV) for 48 MHz, 24 MHz, 12 MHz, or 6 MHz HFCLKOUT output
- Both output clocks have a direct connection to primary clock routing

Figure 3.14, Table 3.6, and Table 3.7 show the OSCI definitions.



Figure 3.14. CrossLinkPlus OSCI Component Symbol

Table 3.6. OSCI Component Port Definition

Port Name	I/O	Description
HFOUTEN	I	High frequency clock output enable
HFCLKOUT	O	High frequency clock output
LFCLKOUT	O	Low Frequency clock output

Table 3.7. OSCI Component Attribute Definition

Defparam Name	Description	Value	Default
HFCLKDIV	Configure HF oscillator output divider	1, 2, 4, 8	1

3.6. Embedded Block RAM Overview

CrossLinkPlus devices contain sysMEM Embedded Block RAM (EBR). The EBR consists of a 9-kb RAM with memory core, dedicated input registers and output registers with separate clock and clock enable.

Support for different memory configurations:

- Single Port
- True Dual Port
- Pseudo Dual Port
- ROM
- FIFO (logic wrapper added automatically by design tools)

Flexible customization features:

- Initialization of RAM/ROM
- Memory cascading (handled automatically by design tools)
- Optional parity bit support
- Byte-enable
- Multiple block size options
- RAM modes support optional Write Through or Read-Before-Write modes

For details, refer to [CrossLinkPlus Memory Usage Guide \(FPGA-TN-02110\)](#).

Table 3.8. sysMEM Block Configurations

Memory Mode	Memory Size Configurations
Single Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18
True Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9
Pseudo Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18
ROM	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18

3.7. Power Management Unit

The embedded Power Management Unit (PMU) allows low-power Sleep State of the device. Figure 3.15 is the block diagram of the PMU IP.

When instantiated in the design, PMU is always on, and uses the low-speed clock from oscillator of the device to perform its operations.

The typical use case for the PMU is through a user implemented state machine that controls the sleep and wake up of the device. The state machine implemented in the FPGA fabric identifies when the device needs to go into sleep mode, issues the command through PMU FPGA fabric interface, assigns the parameters for sleep (time to wake up and so on) and issues Sleep command.

The device can be woken up externally using the PMU Wake-Up (USRWKUP) pin, or from the PMU Watch Dog Timer expiry or from I2C0 (address decoding detection or FIFO full in one of hardened I²C).

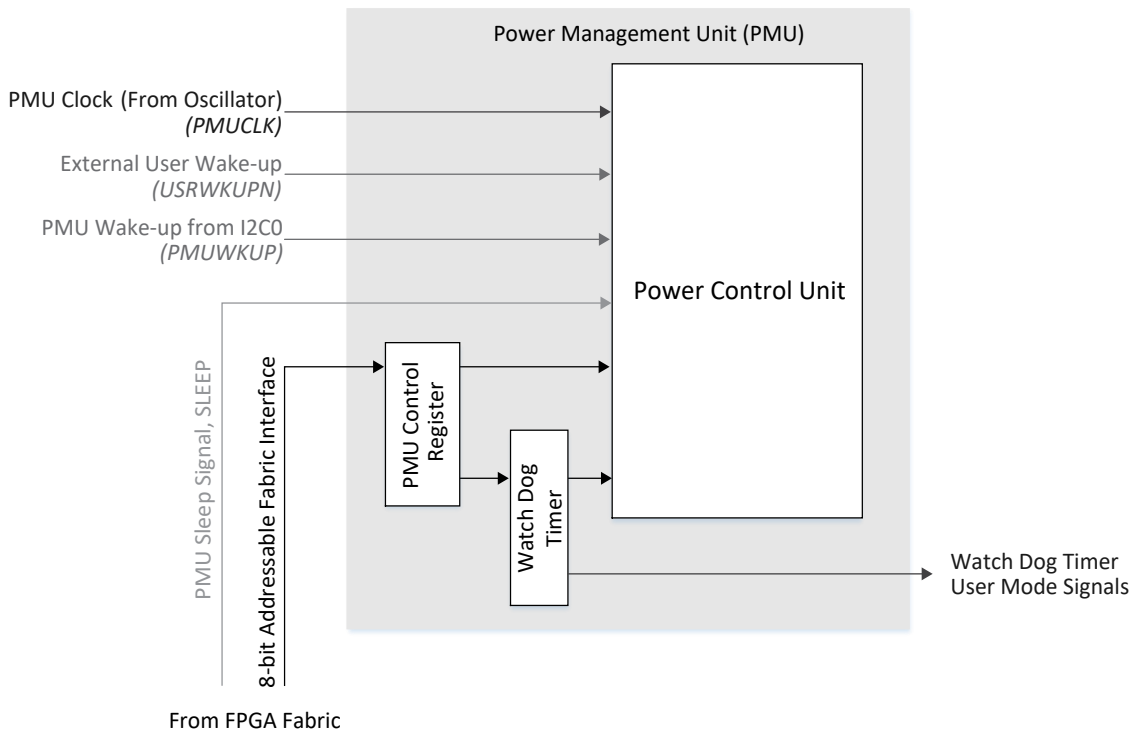


Figure 3.15. CrossLinkPlus MIPI D-PHY Block

3.7.1. PMU State Machine

PMU can place the device in two mutually exclusive states – Normal State and Sleep State. Figure 3.16 shows the PMU State Machine triggers for transition from one state to the other.

- **Normal State** – All elements of the device are active to the extent required by the design. In this state, the device is at fully active and performing as required by the application. Note that the power consumption of the device is the highest in this state.
- **Sleep State** – The device is power gated such that the device is not operational. The configuration of the device and the EBR contents are retained; thus, in Sleep mode, the device does not lose configuration SRAM and EBR contents. When it transitions to Normal state, device operates with these contents preserved.

The PMU is active along with the associated GPIOs. The power consumption of the device is lowest in this state. This helps reduce the overall power consumption for the device.

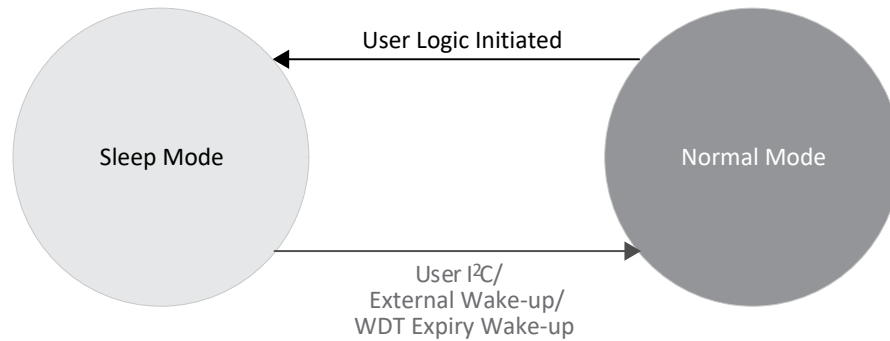


Figure 3.16. CrossLinkPlus PMU State Machine

For more details, refer to [Power Management and Calculation for CrossLinkPlus Devices \(FPGA-TN-02111\)](#).

3.8. User I²C IP

CrossLinkPlus devices have two I²C IP cores that can be configured either as an I²C master or as an I²C slave. The I2C0 core has pre-assigned pins, and supports PMU wakeup over I²C. The pins for the I2C1 interface are not pre-assigned – you can use any General Purpose I/O pins.

The I²C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Clock stretching
- Up to 1 MHz data transfer speed
- General call support
- Optionally delaying input or output data, or both
- Optional FIFO mode
- Transmit FIFO size is 10 bits x 16 bytes, receive FIFO size is 10 bits x 32 bytes

For further information on the User I²C, refer to [CrossLinkPlus Hardened IP Usage Guide \(FPGA-TN-02112\)](#).

3.9. Programming and Configuration

CrossLinkPlus is an SRAM-based programmable logic device that includes an internal Flash, as well as flexible SPI and I²C configuration modes. CrossLinkPlus provides four modes for loading the configuration data into the SRAM memory.

- **Self-Download Mode** – CrossLinkPlus retrieves bitstream from the internal Flash
- **Master SPI Mode** – CrossLinkPlus retrieves bitstream from an external SPI Flash
- **Slave SPI Mode** – System microprocessor writes bitstream to CrossLinkPlus through SPI port
- **Slave I²C Mode** – System microprocessor writes bitstream to CrossLinkPlus through I²C port

CrossLinkPlus provides a set of sysCONFIG I/O pins to program and configure the FPGA. The sysCONFIG pins are grouped together to create ports (I²C, SSPI, or MSPI) that are used to interact with the FPGA for programming, configuration, and access of resources inside the FPGA. The sysCONFIG pins in a configuration group, as shown in [Table 3.9](#), may be active and used for programming the FPGA. Or, they can be reconfigured to act as general purpose I/O.

Table 3.9. CrossLinkPlus sysCONFIG Pins

Pin Name	Associated sysCONFIG Port
CRESET_B	Self Download Mode/SSPI/MSPI/I ² C
CDONE	Self Download Mode/SSPI/MSPI/I ² C
SPI_SCK/MCK/SDA	SSPI/MSPI/I ² C
SPI_SS/CSN/SCL	SSPI/MSPI/I ² C
MOSI	SSPI/MSPI
MISO	SSPI/MSPI

As external power ramps up, a Power On Reset (POR) circuit inside the FPGA becomes active. When POR conditions are met, the POR circuit releases an internal reset strobe, allowing the device to begin its initialization process. After CrossLinkPlus drives CDONE low, CrossLinkPlus enters the memory initialization phase where it clears all of the SRAM memory inside the FPGA. CrossLinkPlus remains in initialization state until the CRESET_B pin is deasserted (HIGH) or after SSPI/I²C activation code is received.

- After CRESET_B goes from low to high, the Configuration Logic puts the device into master auto booting mode where it boots either from the internal Flash or an external SPI boot PROM.
- Holding the CRESET_B low postpones the master auto-booting event and allows the slave configuration ports (Slave SPI or Slave I²C) to detect a *Slave Active* condition where the SPI or I²C Master sends an Activation Key code to CrossLinkPlus. To prevent the device from entering Master Auto Boot Mode during power-up, CRESET_B must be asserted within 9.5 ms from V_{cc} min (Table 4.2). Once CRESET_B is asserted, the Activation Keys can be written to CrossLinkPlus at any time as long as CRESET_B is asserted.
- Sources should not drive output to CrossLinkPlus until configuration has been completed to ensure CrossLinkPlus is in a known state.

In addition to the flexible configuration modes, the CrossLinkPlus configuration engine supports the following special features:

- TransFR (Transparent Field Reconfiguration) allowing you to update logic in field without interrupting system operation by freezing I/O states during configuration
- Dual-Boot Support for primary and golden bitstreams provides automatic recovery from configuration failures. One image is in the internal Flash and second image is in the external Flash.
- Security and One-Time Programmable (OTP) modes protect bitstream integrity and prevent read back
- 64-bit unique TraceID per device

For more information, refer to [CrossLinkPlus Programming and Configuration Usage Guide \(FPGA-TN-02103\)](#).

4. DC and Switching Characteristics

4.1. Absolute Maximum Ratings

Table 4.1. Absolute Maximum Ratings^{1, 2, 3}

Symbol	Parameter	Min	Max	Unit
V _{CC}	Core Supply Voltage	-0.5	1.32	V
V _{CCGPLL}	PLL Supply Voltage	-0.5	1.32	V
V _{CCAUX}	Auxiliary Supply Voltage for Bank 1, Bank 2, and Flash	-0.5	3.63	V
V _{CCIO}	I/O Driver Supply Voltage for Banks 0, 1, 2	-0.5	3.63	V
—	Input or I/O Transient Voltage Applied	-0.5	3.63	V
V _{CCA_DPHYx} V _{CCPLL_DPHY} V _{CCMU_DPHY1}	MIPI D-PHY Supply Voltages	-0.5	1.32	V
—	Voltage Applied on MIPI D-PHY Pins	-0.5	1.32	V
T _A	Storage Temperature (Ambient)	-65	150	°C
T _J	Junction Temperature (TJ)	—	+125	°C

Notes:

1. Stress above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.

4.2. Recommended Operating Conditions

Table 4.2. Recommended Operating Conditions^{1, 2}

Symbol	Parameter	Min	Max	Unit
V _{CC}	Core Supply Voltage	1.14	1.26	V
V _{CCGPLL}	PLL Supply Voltage	1.14	1.26	V
V _{CCAUX}	Auxiliary Supply Voltage for Bank 1, Bank 2, and Flash – @ 2.5 V	2.375	2.625	V
	Auxiliary Supply Voltage for Bank 1, Bank 2, and Flash – @ 3.3 V	3.135	3.465	V
V _{CCIO0}	I/O Driver Supply Voltage for Bank 0	1.71	3.465	V
V _{CCIO1/2}	I/O Driver Supply Voltage for Bank 1, Bank 2	1.14	3.465	V
T _{JIND}	Junction Temperature, Industrial Operation	-40	100	°C
D-PHY External Power Supply				
V _{CCA_DPHYx}	Analog Supply Voltage for D-PHY	1.14	1.26	V
V _{CCPLL_DPHYx}	PLL Supply voltage for D-PHY	1.14	1.26	V

Notes:

1. For correct operation, all supplies must be held in their valid operation range.
2. Like power supplies, must be tied together if they are at the same supply voltage. Follow the noise filtering recommendations in [CrossLinkPlus Hardware Checklist \(FPGA-TN-02105\)](#).

4.3. Power Supply Ramp Rates

Over recommended operating conditions.

Table 4.3. Power Supply Ramp Rates

Symbol	Parameter	Min	Max	Unit
t_{RAMP}	Power supply ramp rates for all power supplies	0.6	10	V/ms

Note: Assume monotonic ramp rates.

4.4. Power-On-Reset Voltage Levels

Table 4.4. Power-On-Reset Voltage Levels^{1, 3, 4}

Symbol	Parameter	Min	Typ	Max	Unit	
V_{PORUP}	Power-On-Reset ramp up trip point (Monitoring V_{CC} , V_{CCIO0} , and V_{CCAUX})	V_{CC}	—	0.95	—	V
		V_{CCIO0} ²	0.87	—	1.50	V
		V_{CCAUX}	—	2.10	—	V
V_{PORDN}	Power-On-Reset ramp down trip point (Monitoring V_{CC} , V_{CCIO0} , and V_{CCAUX})	V_{CC}	—	0.825	—	V
		V_{CCIO0} ²	—	—	1.50	V
		V_{CCAUX}	—	1.90	—	V

Notes:

- These POR ramp up trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
- Only V_{CCIO0} (Config Bank) has a Power-On-Reset ramp up trip point. All other V_{CCIO} s do not have Power-On-Reset ramp up detection.
- V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.
- Configuration starts after V_{CC} , V_{CCIO0} , and V_{CCAUX} reach V_{PORUP} . For details, see $t_{CONFIGURATION}$ time in [Table 4.21](#).

4.5. Electro-Static Discharge (ESD) Performance

Refer to the [LIFMDF Product Family Qualification Summary](#) for complete qualification data, including the ESD performance.

4.6. DC Electrical Characteristics

Over recommended operating conditions.

Table 4.5. DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$I_{IL}, I_{IH}^{1,4,5}$	Input or I/O Leakage	$0 \leq V_{IN} \leq V_{CCIO}$	-10	—	+10	μA
I_{PU}^4	Internal Pull-Up Current	$V_{CCIO} = 1.8 V$ between $0 \leq V_{IN} \leq 0.65 * V_{CCIO}$	-3	—	-31	μA
		$V_{CCIO} = 2.5 V$ between $0 \leq V_{IN} \leq 0.65 * V_{CCIO}$	-8	—	-72	μA
		$V_{CCIO} = 3.3 V$ between $0 \leq V_{IN} \leq 0.65 * V_{CCIO}$	-11	—	-128	μA
C_1^2	I/O Capacitance ²	$V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.2 V,$ $V_{CC} = 1.2 V, V_{IO} = 0$ to $V_{IH} (MAX)$	—	6	—	pF
C_2^2	Dedicated Input Capacitance ²	$V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.2 V,$ $V_{CC} = 1.2 V, V_{IO} = 0$ to $V_{IH} (MAX)$	—	6	—	pF
C_3^2	MIPI D-PHY High Speed I/O Capacitance	$V_{CCIO} = 2.5V, V_{CC} = 1.2V, V_{CC*_{DPHY}} = 1.2V, V_{IO} = 0$ to $V_{IH} (MAX)$	—	5	—	pF
V_{HYST}^3	Hysteresis for Single-Ended Inputs	$V_{CCIO} = 3.3 V, 2.5 V, 1.8 V$ $V_{CC} = 1.2 V, V_{IO} = 0$ to $V_{IH} (MAX)$	—	200	—	mV

Notes:

- Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
- $T_A = 25^\circ C, f = 1.0$ MHz.
- Hysteresis is not available for $V_{CCIO} = 1.2$ V.
- Weak pull-up setting. Programmable pull-up resistors on Bank 0 sees higher current. Refer to [CrossLinkPlus sys/I/O Usage Guide \(FPGA-TN-02108\)](#) for details on programmable pull-up resistors.
- Input pins are clamped to V_{CCIO} and GND by a diode. When input is higher than V_{CCIO} , or lower than GND, the Input Leakage current is higher than the I_{IL} and I_{IH} .

4.7. CrossLinkPlus Supply Current

Over recommended operating conditions.

Table 4.6. CrossLinkPlus Supply Current

Symbol	Parameter	Typ	Unit
Normal Operation¹			
I_{CC}	V_{CC} Power Supply Current	7	mA
I_{CCPLL}	PLL Power Supply Current	50	μA
I_{CCAUX}	Auxiliary Power Supply Current for Bank 1, 2 and Flash Programming Supply Current	3	mA
I_{CCIOx}	Bank x Power Supply Current (per Bank)	60	μA
$I_{CCA_{DPHYx}}$	$V_{CCA_{DPHYx}}$ Power Supply Current	8.5	mA
$I_{CCPLL_{DPHYx}}$	$V_{CCPLL_{DPHYx}}$ Power Supply Current	1.5	mA
Standby Current²			
I_{CC_STDBY}	V_{CC} Power Supply Standby Current	4	mA
I_{CCPLL_STDBY}	PLL Power Supply Standby Current	10	μA
I_{CCAUX_STDBY}	Auxiliary Power Supply Current for Bank 1, 2 and Flash Programming Supply Standby Current	0.2	mA
I_{CCIOx_STDBY}	Bank Power Supply Standby Current (per Bank)	6	μA
$I_{CCA_{DPHYx_STDBY}}$	$V_{CCA_{DPHYx}}$ Power Supply Standby Current	6	μA
$I_{CCPLL_{DPHYx_STDBY}}$	$V_{CCPLL_{DPHYx}}$ Power Supply Standby Current	4	μA
Sleep/Power Down Mode Current³			
I_{CC_SLEEP}	V_{CC} Power Supply Sleep Current	0.2	mA
I_{CCPLL_SLEEP}	PLL Power Supply Current	10	μA
I_{CCAUX_SLEEP}	Auxiliary Power Supply Current for Bank 1, 2 and Flash Programming Supply Current	20	μA

Symbol	Parameter	Typ	Unit
I _{CCIOx_SLEEP}	Bank Power Supply Current (per Bank)	6	μA
I _{CCA_DPHY_SLEEP}	V _{CCA_DPHYx} Power Supply Sleep Current	6	μA
I _{CCPLL_DPHY_SLEEP}	V _{CCPLL_DPHYx} Power Supply Sleep Current	4	μA

Notes:

1. **Normal Operation**

2:1 MIPI CSI-2 Image Sensor Aggregator Bridge design under the following conditions:

- T_J = 25 °C, all power supplies at nominal voltages.
- Typical processed device in ucfBGA64 package.
- To determine power for all other applications and operating conditions, use Power Calculator in Lattice Diamond design software.

2. **Standby Operation**

A typically processed device in ucfBGA64 package with “blank” pattern programmed. A “blank” pattern configured the part to the following conditions:

- All outputs are tri-stated, all inputs are held at either V_{CCIO}, or GND.
- All clock inputs are at 0 MHz.
- T_J = 25 °C, all power supplies at nominal voltages.
- No pull-ups on I/O.

3. **Sleep/Power Down Mode**

2:1 MIPI CSI-2 Image Sensor Aggregator Bridge design under the following conditions:

- Design is put into Sleep/Power Down Mode with user logic powers down D-PHY, and enters into Sleep Mode in PMU.
- T_J = 25 °C, all power supplies at nominal voltages.
- Typical processed device in ucfBGA64 package.

4. **For ucfBGA64 package**

- V_{CCA_DPHY0} and V_{CCA_DPHY1} are tied together as V_{CCA_DPHYx}.
- V_{CCPLL_DPHY0} and V_{CCPLL_DPHY1} are tied together as V_{CCPLL_DPHYx}.

5. To determine the CrossLinkPlus start-up peak current, use the Power Calculator tool in the Lattice Diamond design software.

4.8. Power Management Unit (PMU) Timing

Over recommended operating conditions.

Table 4.7. PMU Timing

Symbol	Parameter	Device	Max	Unit
t _{PMUWAKE}	Time for PMU to wake from Sleep mode	All Devices	0.5	ms

Note: For details on PMU usage, refer to [Power Management and Calculation for CrossLinkPlus Devices \(FPGA-TN-02111\)](#).

4.9. sysI/O Recommended Operating Conditions

Over recommended operating conditions.

Table 4.8. sysI/O Recommended Operating Conditions¹

Standard	V _{CCIO}		
	Min	Typ	Max
LVC MOS33/LVTTL33	3.135	3.30	3.465
LVC MOS25	2.375	2.50	2.625
LVC MOS18	1.710	1.80	1.890
LVC MOS12 (Output only) ²	1.140	1.20	1.260
subLVDS (Input only)	1.710	1.80	1.890
	2.375	2.50	2.625
	3.135	3.30	3.465
SLVS200 (Input only) ³	1.140	1.20	1.260
	1.710	1.80	1.890
	2.375	2.50	2.625
	3.135	3.30	3.465
LVDS (Input only)	1.710	1.80	1.890
	2.375	2.50	2.625
	3.135	3.30	3.465
LVDS (Output only)	2.375	2.50	2.625
MIPI (Input only)	1.140	1.20	1.260

Notes:

1. For input voltage compatibility, refer to [CrossLinkPlus sysI/O Usage Guide \(FPGA-TN-02108\)](#).
2. For V_{CCIO1} and V_{CCIO2} only.
3. For SLVS200/MIPI interface I/O placement, see the [Programmable I/O Banks](#) section.

4.10. sysI/O Single-Ended DC Electrical Characteristics

Over recommended operating conditions.

Table 4.9. sysI/O Single-Ended DC Electrical Characteristics¹

Input/Output Standard	V _{IL}		V _{IH}		V _{OL} Max (V)	V _{OH} Min (V)	I _{OL} (mA)	I _{OH} (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVC MOS33/LVTTL33	-0.3	0.8	2.0	V _{CCIO} +0.2	0.40	V _{CCIO} - 0.4	8	-8
					0.20	V _{CCIO} - 0.2	0.1	-0.1
LVC MOS25	-0.3	0.7	1.7	V _{CCIO} +0.2	0.40	V _{CCIO} - 0.4	6	-6
					0.20	V _{CCIO} - 0.2	0.1	-0.1
LVC MOS18	-0.3	0.35 V _{CCIO}	0.67 V _{CCIO}	V _{CCIO} +0.2	0.40	V _{CCIO} - 0.4	4	-4
					0.20	V _{CCIO} - 0.2	0.1	-0.1
LVC MOS12 ⁽²⁾ (Output only)	—	—	—	—	0.40	V _{CCIO} - 0.4	2	-2
					0.20	V _{CCIO} - 0.2	0.1	-0.1

Notes:

1. V_{CCIO} in the table follows the V_{CCIO} power rail setting of the respective bank.
2. For V_{CCIO1} and V_{CCIO2} only.

4.11. sysI/O Differential Electrical Characteristics

4.11.1. LVDS/subLVDS/SLVS200

Over recommended operating conditions.

Table 4.10. LVDS/subLVDS1/SLVS200^{1, 2}

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{INP}, V_{INN}	Input Voltage	—	0.00	—	2.40	V
V_{CM}	Input Common Mode Voltage	Half the sum of the two inputs	0.05	—	2.35	V
$V_{THD(LVDS)}$	Differential Input Threshold	$ V_{INP} - V_{INN} $	100	—	—	mV
$V_{THD(subLVDS)}$	Differential Input Threshold	$ V_{INP} - V_{INN} $	90	—	—	mV
$V_{THD(SLVS200)}$	Differential Input Threshold	$ V_{INP} - V_{INN} $	70	—	—	mV
I_{IN}	Input Current	Normal Mode	-10	—	10	μ A
		Standby Mode	-10	—	10	μ A
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	$RT = 100 \Omega$	—	1.43	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	$RT = 100 \Omega$	0.90	1.08	—	V
V_{OD}	Output Voltage Differential	$ V_{OP} - V_{OM} , RT = 100 \Omega$	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between High and Low	—	—	—	50	mV
V_{OS}	Output Voltage Offset (Common Mode Voltage)	$(V_{OP} + V_{OM})/2, RT = 100 \Omega$	1.125	1.250	1.375	V
ΔV_{OS}	Change in V_{OS} between H and L	—	—	—	50	mV
I_{SAB}	Output Short Circuit Current	$V_{OD} = 0$ V driver outputs shorted to each other	—	—	12	mA

Notes:

- Inputs only for subLVDS and SLVS200.
- For SLVS200/MIPI interface I/O placement, see the [Programmable I/O Banks](#) section.

4.11.2. Hardened MIPI D-PHY I/O

Over recommended operating conditions.

Table 4.11. MIPI D-PHY

Symbol	Description	Min	Typ	Max	Unit
Receiver					
High Speed					
V _{CMRX}	Common-Mode Voltage HS Receive Mode	70	—	330	mV
V _{IDTH}	Differential Input High Threshold	—	—	70	mV
V _{IDTL}	Differential Input Low Threshold	-70	—	—	mV
V _{IHHS}	Single-ended input High Voltage	—	—	460	mV
V _{ILHS}	Single-ended Input Low Voltage	-40	—	—	mV
V _{TERM-EN}	Single-ended Threshold for HS Termination Enable	—	—	450	mV
Z _{ID}	Differential Input Impedance	80	100	125	Ω
Low Power					
V _{IH}	Logic 1 Input Voltage	880	—	—	mV
V _{IL}	Logic 0 Input Voltage, not in ULP State	—	—	550	mV
V _{IL-ULPS}	Logic 0 Input Voltage, in ULP State	—	—	300	mV
V _{HYST}	Input Hysteresis	25	—	—	mV
Transmitter					
High Speed					
V _{CMTX}	HS Transmit Static Common Mode Voltage	150	200	250	mV
V _{OD}	HS Transmit Differential Voltage	140	200	270	mV
V _{OHHS}	HS Single-ended Output High Voltage	—	—	360	mV
Z _{OS}	Single-ended Output Impedance	40	50	62.5	Ω
ΔZ _{OS}	Single-ended Output Impedance Mismatch	—	—	10	%
Low Power					
V _{OH}	Output High Voltage	1.1	1.2	1.3	V
V _{OL}	Output Low Voltage	-50	—	50	mV
Z _{OLP}	Output Impedance in LP Mode	110	—	—	Ω

4.12. CrossLinkPlus Maximum General Purpose I/O Buffer Speed

Over recommended operating conditions.

Table 4.12. CrossLinkPlus Maximum I/O Buffer Speed

Buffer	Description	Max	Unit
Maximum Input Frequency			
LVDS25	LVDS, $V_{CCIO} = 2.5\text{ V}$	600	MHz
subLVDS	subLVDS, $V_{CCIO} = 2.5\text{ V}$	600	MHz
MIPI D-PHY (HS) ^{6,7}	MIPI D-PHY	600	MHz
MIPI D-PHY (LP) ⁷	MIPI D-PHY	5	MHz
SLVS200 ⁷	SLVS200, $V_{CCIO} = 2.5\text{ V}$	600	MHz
LVC MOS33/LVTTL33	LVC MOS/LVTTL, $V_{CCIO} = 3.3\text{ V}$	300	MHz
LVC MOS25D	Differential LVC MOS, $V_{CCIO} = 2.5\text{ V}$	300	MHz
LVC MOS25	LVC MOS, $V_{CCIO} = 2.5\text{ V}$	300	MHz
LVC MOS18	LVC MOS, $V_{CCIO} = 1.8\text{ V}$	155	MHz
Maximum Output Frequency			
LVDS25	LVDS, $V_{CCIO} = 2.5\text{ V}$	600	MHz
LVC MOS33/LVTTL33	LVC MOS/LVTTL, $V_{CCIO} = 3.3\text{ V}$	300	MHz
LVTTL33D	Differential LVTTL, $V_{CCIO} = 3.3\text{ V}$	300	MHz
LVC MOS33D	Differential LVC MOS, 3.3 V	300	MHz
LVC MOS25	LVC MOS, 2.5 V	300	MHz
LVC MOS25D	Differential LVC MOS, 2.5 V	300	MHz
LVC MOS18	LVC MOS, 1.8 V	155	MHz
LVC MOS12	LVC MOS, $V_{CCIO1/2} = 1.2\text{ V}$	70	MHz

Notes:

- These maximum speeds are characterized but not tested on every device.
- Maximum I/O speed for differential output standards emulated with resistors depends on the layout.
- LVC MOS timing is measured with the load specified in [Table 4.23](#).
- Actual system operation may vary depending on user logic implementation.
- Maximum data rate equals two times the clock rate when utilizing DDR.
- This is the maximum MIPI D-PHY input rate on the programmable I/O Bank 1 and Bank 2. The hardened MIPI D-PHY input and output rates are described in [Hardened MIPI D-PHY Performance](#) section. For SLVS200/MIPI interface I/O placement, see the [Programmable I/O Banks](#) section.
- Implement the following guideline for I/O placement when MIPI Rx inputs are present on the programmable I/O banks to ensure optimal performance:

	Bank 1	Bank 2
SLVS200/MIPI Rx on Bank 1	No LVC MOS Outputs	No LVC MOS Outputs
SLVS200/MIPI Rx on Bank 2	No LVC MOS Outputs	No LVC MOS Outputs
SLVS200/MIPI Rx on Bank 1 and Bank 2	No LVC MOS Outputs	No LVC MOS Outputs

- The Diamond Software PAR Design Strategy setting of LVC MOS12_18_ONLY (default) allows outputs as long as they are LVC MOS12 or LVC MOS18.
- The Diamond Software PAR Design Strategy setting of LVMOS_NOT_PERMITTED causes an error in PAR regarding I/O placement if there are any outputs in Bank 1 or Bank 2 when an SLVS/MIPI Receiver interface is present.

4.13. CrossLinkPlus External Switching Characteristics

Over recommended operating conditions.

Table 4.13. CrossLinkPlus External Switching Characteristics^{3,4}

Parameter	Description	Conditions	-6		Unit
			Min	Max	
Clocks					
Primary Clock					
f _{MAX_PRI}	Frequency for Primary Clock Tree	—	—	150	MHz
t _{W_PRI}	Clock Pulse Width for Primary Clock	—	0.8	—	ns
t _{SKEW_PRI}	Primary Clock Skew Within a Clock	—	—	450	ps
Edge Clock					
f _{MAX_EDGE}	Frequency for Edge Clock Tree	—	—	600	MHz
t _{W_EDGE}	Clock Pulse Width for Edge Clock	—	0.783	—	ns
t _{SKEW_EDGE}	Edge Clock Skew Within a Bank	—	—	120	ps
Generic DDR Interfaces¹					
Generic DDRX8 or DDRX4 or DDRX2 I/O with Clock and Data Centered at General Purpose Pins (GDDR_X_RX/TX.ECLK.Centered or GDDR_X_RX/TX.ECLK.Centered or GDDR_X_RX/TX.ECLK.Centered)					
t _{SU_GDDR_X_4_8_CENTERED}	Input Data Set-Up Before CLK Rising and Falling edges	—	0.167	—	ns
t _{HD_GDDR_X_4_8_CENTERED}	Input Data Hold After CLK Rising and Falling edges	—	0.167	—	ns
t _{DVB_GDDR_X_4_8_CENTERED}	Output Data Valid Before CLK Output Rising and Falling edges	Data Rate = 1.2 Gb/s	0.297	—	ns
		Other Data Rates	-0.120	—	ns+1/2UI
t _{DVA_GDDR_X_4_8_CENTERED}	Output Data Valid After CLK Output Rising and Falling edges	Data Rate = 1.2 Gb/s	0.297	—	ns
		Other Data Rates	-0.120	—	ns+1/2 UI
f _{MAX_GDDR_X_4_8_CENTERED}	Frequency for ECLK ²	GDDR _X 2	—	300	MHz
		GDDR _X 4 and GDDR _X 8	—	600	MHz

Parameter	Description	Conditions	-6		Unit
			Min	Max	
Generic DDR Interfaces ¹					
Generic DDRX8 or DDRX4 or DDRX2 I/O with Clock and Data Centered at General Purpose Pins (GDDR_X8_RX/TX.ECLK.Centered or GDDR_X4_RX/TX.ECLK.Centered or GDDR_X2_RX/TX.ECLK.Centered)					
Generic DDRX1 I/O with Clock and Data Centered at General Purpose Pins (GDDR_X1_RX/TX.SCLK.Centered)					
t _{SU_GDDR_X1_CENTERED}	Input Data Set-Up Before CLK Rising and Falling edges	—	0.917	—	ns
t _{HD_GDDR_X1_CENTERED}	Input Data Hold After CLK Rising and Falling edges	—	0.917	—	ns
t _{DVB_GDDR_X1_CENTERED}	Output Data Valid Before CLK Output Rising and Falling edges	Data Rate = 300 Mb/s	1.217	—	ns
		Other Data Rates	-0.450	—	ns+1/2 UI
t _{DVA_GDDR_X1_CENTERED}	Output Data Valid After CLK Output Rising and Falling edges	Data Rate = 300 Mb/s	1.217	—	ns
		Other Data Rates	-0.450	—	ns+1/2 UI
f _{MAX_GDDR_X1_CENTERED}	Frequency for PCLK ²	—	—	150	MHz
Generic DDRX8 or DDRX4 or DDRX2 I/O with Clock and Data Aligned at General Purpose Pins (GDDR_X8_RX/TX.ECLK.Aligned or GDDR_X4_RX/TX.ECLK.Aligned or GDDR_X2_RX/TX.ECLK.Aligned)					
t _{SU_GDDR_X2_4_8_ALIGNED}	Input Data Valid After CLK Rising and Falling edges	Data Rate = 1.2 Gb/s	—	0.188	ns
		Other Data Rates	—	-0.229	ns+1/2 UI
t _{HD_GDDR_X2_4_8_ALIGNED}	Input Data Hold After CLK Rising and Falling edges	Data Rate = 1.2 Gb/s	0.646	—	ns
		Other Data Rates	0.229	—	ns+1/2 UI
t _{DIA_GDDR_X2_4_8_ALIGNED}	Output Data Invalid After CLK Rising and Falling edges Output	—	—	0.120	ns
t _{DIB_GDDR_X2_4_8_ALIGNED}	Output Data Invalid Before CLK Output Rising and Falling edges	—	—	0.120	ns
f _{MAX_GDDR_X2_4_8_ALIGNED}	Frequency for ECLK ²	GDDR _X 2	—	300	MHz
		GDDR _X 4 and GDDR _X 8	—	600	MHz

Parameter	Description	Conditions	-6		Unit
			Min	Max	
Generic DDR Interfaces ¹					
Generic DDRX1 I/O with Clock and Data Aligned at General Purpose Pins (GDDRX1_RX/TX.SCLK.Aligned)					
t _{SU_GDDR1_ALIGNED}	Input Data Valid After CLK Rising and Falling edges	Data Rate = 300 Mb/s	—	0.750	ns
		Other Data Rates	—	-0.917	ns+1/2UI
t _{HD_GDDR1_ALIGNED}	Input Data Hold After CLK Rising and Falling edges	Data Rate = 300 Mb/s	2.583	—	ns
		Other Data Rates	0.916	—	ns+1/2UI
t _{DIA_GDDR1_ALIGNED}	Output Data Invalid After CLK Rising and Falling edges Output	—	—	0.450	ns
t _{DIB_GDDR1_ALIGNED}	Output Data Invalid Before CLK Output Rising and Falling edges	—	—	0.450	ns
f _{MAX_GDDR1_ALIGNED}	Frequency for ECLK ²	—	—	150	MHz
General Purpose I/O MIPI D-PHY Rx with 1:8 or 1:16 Gearing					
t _{SU_GDDR1_MP}	Input Data Set-Up Before CLK	842 Mb/s < Data Rate ≤ 1.2 Gb/s and V _{IDTH} = 140 mV V _{IDTL} = -140 mV	0.200	—	UI
		473 Mb/s < Data Rate ≤ 842 Mb/s and V _{IDTH} = 140 mV V _{IDTL} = -140 mV	0.150	—	UI
		Data Rate ≤ 473 Mb/s and V _{IDTH} = 70 mV V _{IDTL} = -70 mV	0.150	—	UI
t _{HD_GDDR1_MP}	Input Data Hold After CLK	842 Mb/s < Data Rate ≤ 1.2 Gb/s and V _{IDTH} = 140 mV V _{IDTL} = -140 mV	0.200	—	UI
		473 Mb/s < Data Rate ≤ 842 Mb/s and V _{IDTH} = 140 mV V _{IDTL} = -140 mV	0.150	—	UI
		Data Rate ≤ 473 Mb/s and V _{IDTH} = 70 mV V _{IDTL} = -70 mV	0.150	—	UI
f _{MAX_GDDR1_MP}	Frequency for ECLK ²	—	—	600	MHz

Parameter	Description	Conditions	-6		Unit
			Min	Max	
Generic DDRX71 or DDRX141 Inputs (GDDR71_RX.ECLK or GDDR141_RX.ECLK)					
t _{RPBi_DVA}	Input Valid Bit "i" switching from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	—	—	0.3	UI
		—	—	-0.222	ns+ (i+ 1/2)*UI
t _{RPBi_DVE}	Input Hold Bit "i" switching from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	—	0.7	—	UI
		—	0.222	—	ns+ (i+ 1/2)*UI
f _{MAX_RX71_141}	DDR71/DDR141 ECLK Frequency ²	—	—	450	MHz
Generic DDR Interfaces ¹					
Generic DDRX141 Outputs with Clock and Data Aligned at Pin (GDDR141_TX.ECLK)					
t _{TPBi_DOV}	Data Output Valid Bit "i" switching from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	—	—	0.143	ns+i*UI
t _{TPBi_DOI}	Data Output Invalid Bit "i" switching from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	—	-0.143	—	ns+i*UI
t _{TPBi_skew_UI}	Tx skew in UI	—	—	0.15	UI
f _{MAX_TX71}	DDR71 ECLK Frequency ²	—	—	525	MHz
Generic DDRX141 Outputs with Clock and Data Aligned at Pin (GDDR141_TX.ECLK)					
t _{TPBi_DOV}	Data Output Valid Bit "i" switching from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	—	—	0.125	ns+i*UI
t _{TPBi_DOI}	Data Output Invalid Bit "i" switching from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	—	-0.125	—	ns+i*UI
t _{TPBi_skew_UI}	TX skew in UI	—	—	0.15	UI
f _{MAX_TX141}	DDR141 ECLK Frequency ²	—	—	600	MHz

Notes:

1. Generic DDRX8, DDRX71 and DDRX141 timing numbers based on LVDS I/O.
2. Maximum clock frequencies are tested under best case conditions. System performance may vary upon the user environment.
3. These numbers are generated using best case PLL location.
4. All numbers are generated with the Lattice Diamond design software.

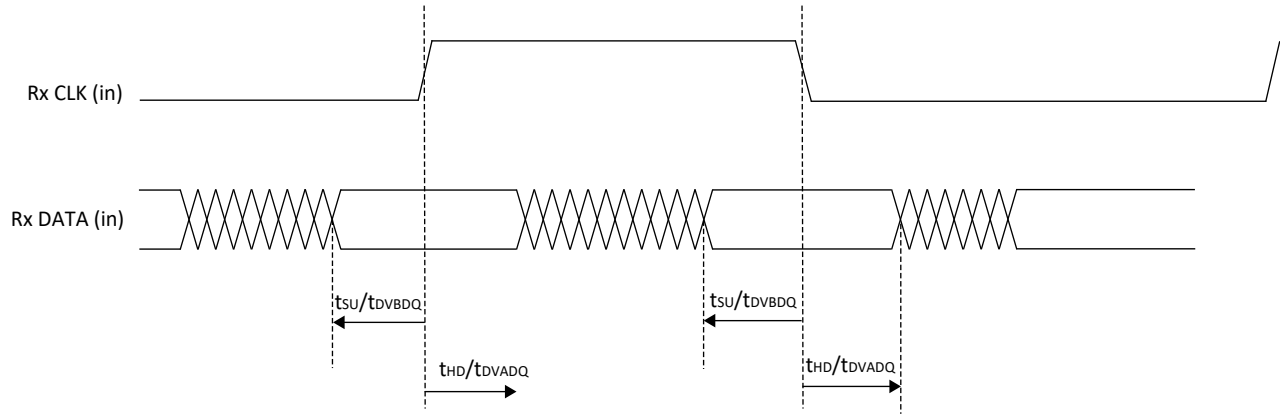


Figure 4.1. Receiver RX.CLK.Centered Waveforms

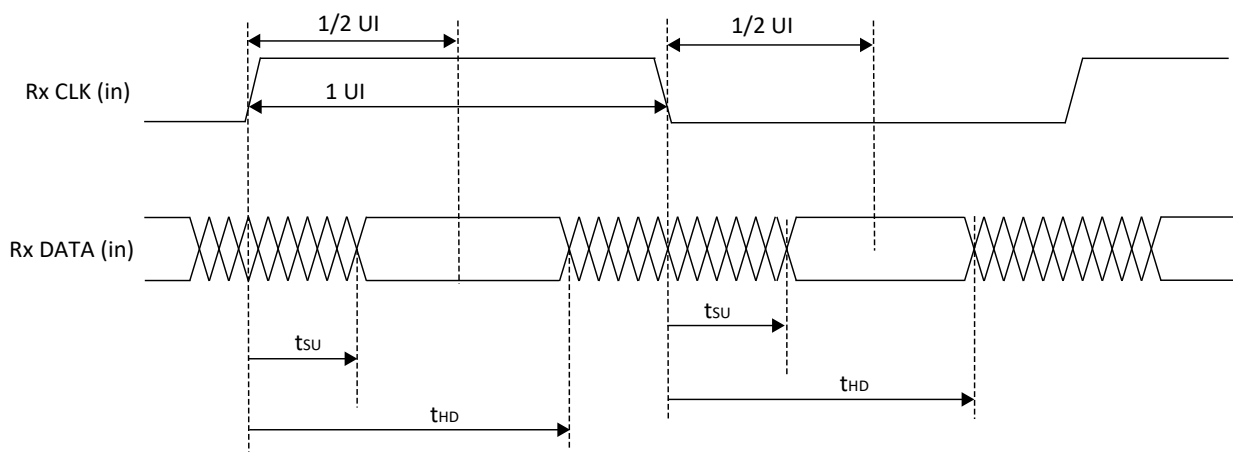


Figure 4.2. Receiver RX.CLK.Aligned Input Waveforms

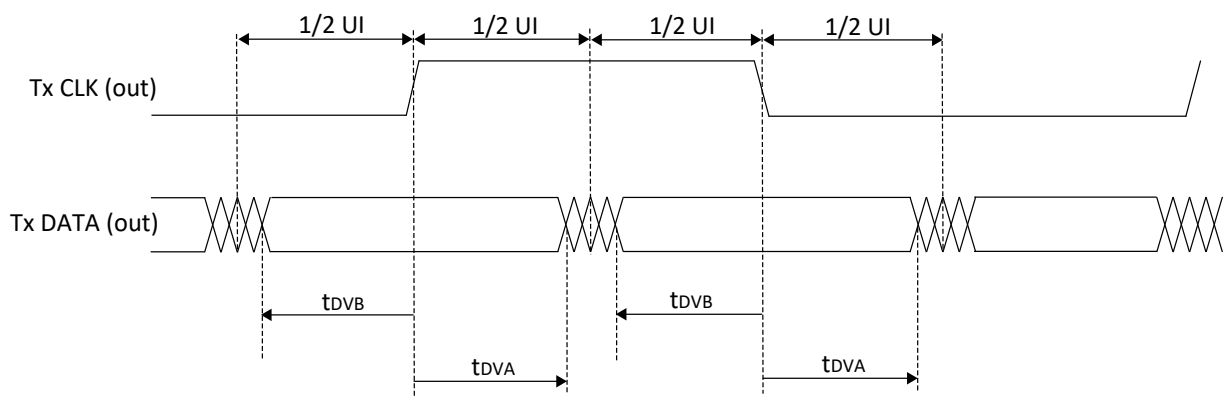


Figure 4.3. Transmit TX.CLK.Centered Output Waveforms

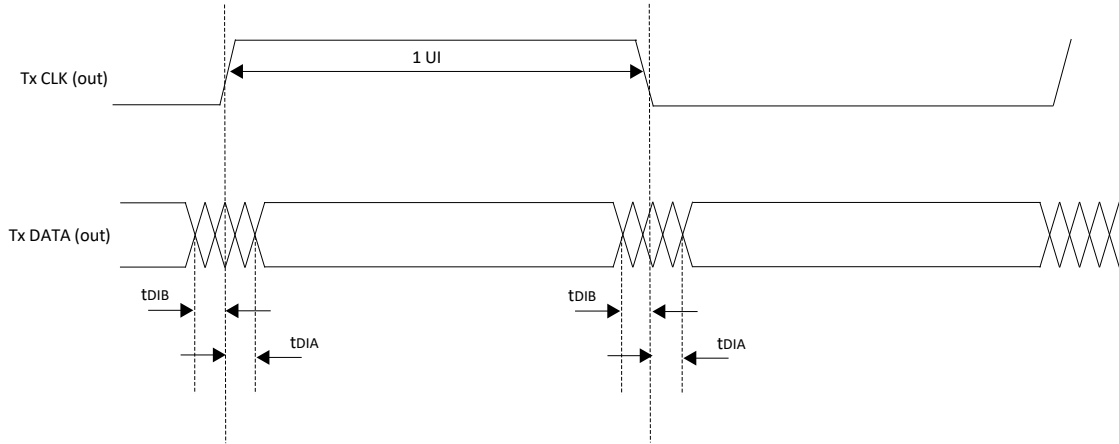


Figure 4.4. Transmit TX.CLK.Aligned Waveforms

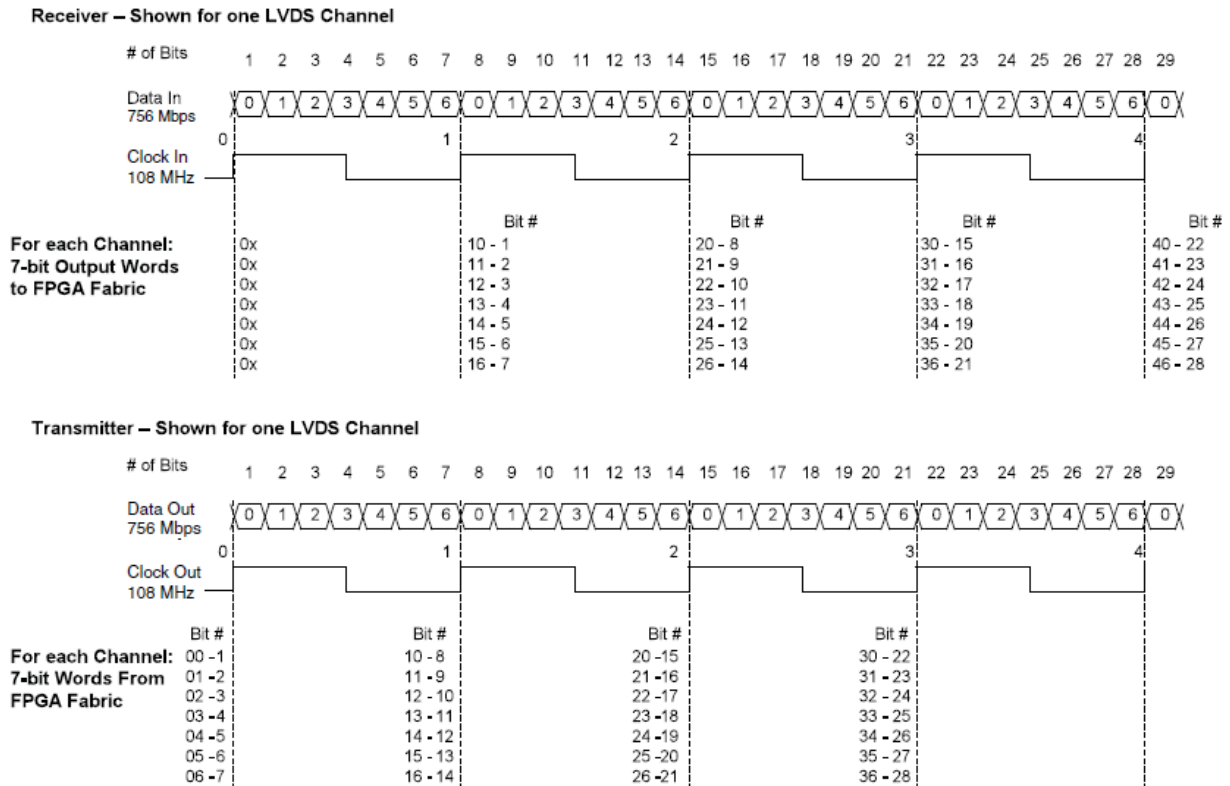


Figure 4.5. DDRX71, DDRX141 Video Timing Waveforms

4.14. sysCLOCK PLL Timing

Over recommended operating conditions.

Table 4.14. sysCLOCK PLL Timing

Parameter	Descriptions	Conditions	Min	Max	Unit
f_{IN}	Input Clock Frequency (CLKI, CLKFB)	—	10	400	MHz
f_{PD}	Phase Detector Input Clock Frequency	—	10	400	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)	—	4.6875	600	MHz
f_{VCO}	PLL VCO Frequency	—	600	1200	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	—	45	55	%
t_{PH}	Output Phase Accuracy	—	-5	5	%
t_{OPJIT}^1	Output Clock Period Jitter ³	$f_{OUT} \geq 100$ MHz	—	100	ps p-p
		$f_{OUT} < 100$ MHz	—	0.025	UIPP
	Output Clock Cycle-to-Cycle Jitter ³	$f_{OUT} \geq 100$ MHz	—	200	ps p-p
		$f_{OUT} < 100$ MHz	—	0.05	UIPP
	Output Clock Phase Jitter	$f_{PD} > 100$ MHz	—	200	ps p-p
		$f_{PD} < 100$ MHz	—	0.05	UIPP
t_{SPO}	Static Phase Offset	Divider ratio = integer	—	400	ps p-p
t_{LOCK}^2	PLL Lock-in Time	—	—	15	ms
t_{UNLOCK}	PLL Unlock Time	—	—	50	ns
t_{IPJIT}	Input Clock Period Jitter	$f_{PD} \geq 20$ MHz	—	500	ps p-p
		$f_{PD} < 20$ MHz	—	0.02	UIPP
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	ns

Notes:

- Jitter sample is taken over 10,000 samples for Periodic jitter, and 2,000 samples for Cycle-to-Cycle jitter of the primary PLL output with clean reference clock with no additional I/O toggling.
- Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
- Period jitter and cycle-to-cycle jitter numbers are guaranteed for $f_{PD} \geq 10$ MHz. For $f_{PD} < 10$ MHz, the jitter numbers may not be met in certain conditions.

4.15. Hardened MIPI D-PHY Performance

Over recommended operating conditions.

Table 4.15. 1500 Mb/s MIPI_DPHY_X8_RX/TX Timing Table (1500 Mb/s > MIPI D-PHY Data Rate > 1200 Mb/s)

Parameter	Description	Min	Max	Unit
t _{SU_MIPIX8}	Input Data Setup before CLK	0.227	—	UI
t _{HD_MIPIX8}	Input Data Hold after CLK	0.305	—	UI
t _{DVB_MIPIX8}	Output Data Valid before CLK Output	0.200	—	UI
t _{DVA_MIPIX8}	Output Data Valid after CLK Output	0.200	—	UI

Table 4.16. 1200 Mb/s MIPI_DPHY_X4_RX/TX Timing Table (1200 Mb/s > MIPI D-PHY Data Rate > 1000 Mb/s)

Parameter	Description	Min	Max	Unit
t _{SU_MIPIX4}	Input Data Setup before CLK	0.200	—	UI
t _{HD_MIPIX4}	Input Data Hold after CLK	0.200	—	UI
t _{DVB_MIPIX4}	Output Data Valid before CLK Output	0.200	—	UI
t _{DVA_MIPIX4}	Output Data Valid after CLK Output	0.200	—	UI

Table 4.17. 1000 Mb/s MIPI_DPHY_X4_RX/TX Timing Table (1000 Mb/s > MIPI D-PHY Data Rate > 10 Mb/s)

Parameter	Description	Min	Max	Unit
t _{SU_MIPIX4}	Input Data Setup before CLK	0.150	—	UI
t _{HD_MIPIX4}	Input Data Hold after CLK	0.150	—	UI
t _{DVB_MIPIX4}	Output Data Valid before CLK Output	0.150	—	UI
t _{DVA_MIPIX4}	Output Data Valid after CLK Output	0.150	—	UI

4.16. Internal Oscillators (HFOSC, LFOSC)

Over recommended operating conditions.

Table 4.18. Internal Oscillators

Parameter	Parameter Description	Min	Typ	Max	Unit
f _{CLKHF}	HFOSC CLKK Clock Frequency	43.2	48	52.8	MHz
f _{CLKLF}	LFOSC CLKK Clock Frequency	9	10	11	kHz
DCH _{CLKHF}	HFOSC Duty Cycle (Clock High Period)	45	50	55	%
DCH _{CLKLF}	LFOSC Duty Cycle (Clock High Period)	45	50	55	%

4.17. User I²C

Over recommended operating conditions.

Table 4.19. User I²C¹

Symbol	Parameter	STD Mode			FAST Mode			FAST Mode Plus ²			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{SCL}	SCL Clock Frequency	—	—	100	—	—	400	—	—	1000 ²	kHz
T _{DELAY}	Optional delay through delay block	—	62	—	—	62	—	—	62	—	ns

Notes:

1. Refer to the I²C Specification for timing requirements.
2. Fast Mode Plus maximum speed may be achieved by using external pull up resistor on I²C bus. Internal pull up may not be sufficient to support the maximum speed.

4.18. CrossLinkPlus sysCONFIG Port Timing Specifications

Over recommended operating conditions.

Table 4.20. sysCONFIG Port Timing Specifications

Symbol	Parameter	Min	Max	Unit
All Configuration Mode				
t _{PRGM} ³	Minimum CRESET_B LOW pulse width required to restart configuration (from falling edge to rising edge)	290	—	ns
Slave SPI¹				
f _{CCLK}	SPI_SCK Input Clock Frequency	—	110	MHz
t _{STSU}	MOSI Setup Time	0.5	—	ns
t _{STH}	MOSI Hold Time	2.0	—	ns
t _{STCO}	SPI_SCK Falling Edge to Valid MISO Output	—	13.3	ns
t _{SCS}	Chip Select HIGH Time	25	—	ns
t _{SCSS}	Chip Select Setup Time	0.5	—	ns
t _{SCSH}	Chip Select Hold Time	0.5	—	ns
Master SPI				
f _{CCLK}	MCK Output Clock Frequency	—	26.4	MHz
I²C²				
f _{MAX}	Maximum SCL Clock Frequency (Fast-Mode Plus)	—	1	MHz

Notes:

1. Refer to [CrossLinkPlus Programming and Configuration Usage Guide \(FPGA-TN-02103\)](#), for timing requirements to enable CrossLinkPlus SSPI Mode.
2. Refer to the I²C specification for timing requirements when configuring with I²C port.
3. t_{PRGM} minimum time does not apply when SLAVE_SPI_PORT, MASTER_SPI_PORT and I²C_PORT are disabled through Diamond Software. Contact your Lattice Sales Representatives for details.

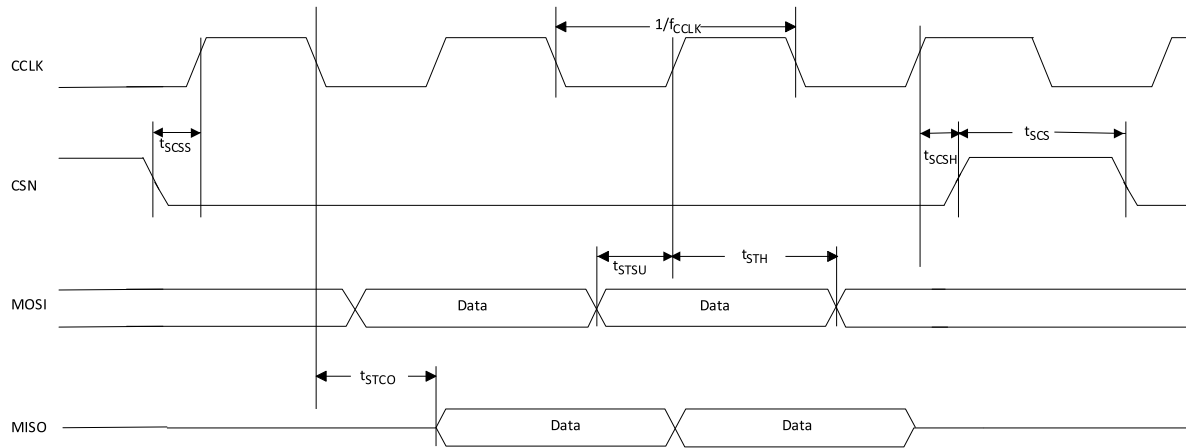


Figure 4.6. SPI Timing Waveforms

4.19. SRAM Configuration Time from internal Flash

Over recommended operating conditions.

Table 4.21. SRAM Configuration Time from internal Flash

Symbol	Parameter	Typ	Unit
T _{CONFIGURATION}	POR/CRESET_B to Device I/O Active ¹	5	ms

Note:

1. Before and during configuration, the I/O are held in tristate with weak internal pull-ups enabled. I/O are released to user functionality when the device has finished configuration.

4.20. Flash Programming/Erase Specifications

Over recommended operating conditions.

Table 4.22. Flash Programming/Erase Specifications

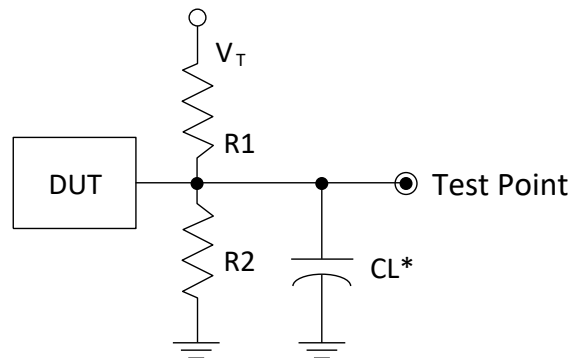
Symbol	Parameter	Min	Max ¹	Unit
N _{PROGCYC}	Flash programming cycles per T _{RETENTION}	—	250	Cycles
	Flash Write/Erase cycles ²	—	250	
T _{RETENTION}	Data retention at 100 °C junction temperature	10	—	Years
	Data retention at 85 °C junction temperature	20	—	

Notes:

1. Maximum Flash memory reads are limited to 3.15e11 cycles over the lifetime of the product.
3. A Write/Erase cycle is defined as any number of writes over time followed by any erase cycle.

4.21. Switching Test Conditions

Figure 4.7 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are listed in Table 4.23.



*CL Includes Test Fixture and Probe Capacitance

Figure 4.7. Output Test Load, LVTTTL and LVCMOS Standards

Table 4.23. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R ₁	R ₂	C _L	Timing Ref.	V _T
LVTTTL and other LVCMOS settings (L ≥ H, H ≥ L)	∞	∞	0 pF	LVC MOS 3.3 = 1.5 V	—
				LVC MOS 2.5 = V _{CCIO} /2	—
				LVC MOS 1.8 = V _{CCIO} /2	—
				LVC MOS 1.2 = V _{CCIO} /2	—
LVC MOS 2.5 I/O (Z ≥ H)	∞	1 MΩ	0 pF	V _{CCIO} /2	—
LVC MOS 2.5 I/O (Z ≥ L)	1 MΩ	∞	0 pF	V _{CCIO} /2	V _{CCIO}
LVC MOS 2.5 I/O (H ≥ Z)	∞	100	0 pF	V _{OH} - 0.10	—
LVC MOS 2.5 I/O (L ≥ Z)	100	∞	0 pF	V _{OL} + 0.10	V _{CCIO}

Note: Output test conditions for all other interfaces are determined by the respective standards.

5. Signal Descriptions

5.1. Dual Function Pin Descriptions

The following table describes the dual functions available to certain pins on the CrossLinkPlus device. These pins may alternatively be used as general purpose I/O when the described dual function is not enabled.

Table 5.1. Dual Function Pin Descriptions

Signal Name	I/O	Description
General Purpose		
USER_SCL	I/O	User Slave I ² CO clock input and Master I ² CO clock output. Enables PMU wake-up via I ² CO.
USER_SDA	I/O	User Slave I ² CO data input and Master I ² CO data output. Enables PMU wakeup via I ² CO.
PMU_WKUPN	—	This pin wakes the PMU from sleep mode when toggled low.
Clock Functions		
GPLL2_0[T, C]_IN	I	General Purpose PLL (GPLL) input pads: T = true and C = complement. These pins can be used to input a reference clock directly to the General Purpose PLL. These pins do not provide direct access to the primary clock network.
GR_PCLK[Bank]0	I	These pins provide a short General Routing path to the primary clock network, but should only be used when the design has used up all the PCLK pins. These pins should only be used for low speed clocks that are not sensitive to skew. Refer to CrossLinkPlus sysCLOCK PLL/DLL Design and Usage Guide (FPGA-TN-02109) for details.
PCLK[T/C][Bank]_[num]	I/O	General Purpose Primary CLK pads: [T/C] = True/Complement, [Bank] = (0, 1 and 2). These pins provide direct access to the primary and edge clock networks.
MIPI_CLK[T/C][Bank]_0	I/O	MIPI D-PHY Reference CLK pads: [T/C] = True/Complement, [Bank] = (0, 1 and 2). These pins can be used to input a reference clock directly to the D-PHY PLLs. These pins do not provide direct access to the primary clock network.
Configuration		
CDONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. Holding CDONE delays configuration.
SPI_SCK	I	Input Configuration Clock for configuring CrossLinkPlus in Slave SPI mode (SSPI).
MCK	O	Output Configuration Clock for configuring CrossLinkPlus in Master SPI mode (MSPI).
SPI_SS	I	Input Chip Select for configuring CrossLinkPlus in Slave SPI mode (SSPI).
CSN	O	Output Chip Select for configuring CrossLinkPlus in Master SPI mode (MSPI).
MOSI	I/O	Data Output when configuring CrossLinkPlus in Master SPI mode (MSPI), data input when configuring CrossLinkPlus in Slave SPI mode (SSPI).
MISO	I/O	Data Input when configuring CrossLinkPlus in Master SPI mode (MSPI), data output when configuring CrossLinkPlus in Slave SPI mode (SSPI).
SCL	I/O	Slave I ² C clock I/O when configuring CrossLinkPlus in I ² C mode.
SDA	I/O	Slave I ² C data I/O when configuring CrossLinkPlus in I ² C mode.

5.2. Dedicated Function Pin Descriptions

Table 5.2. Dedicated Function Pin Descriptions

Signal Name	I/O	Description
Configuration		
CRESET_B	I	Configuration Reset, active LOW.
MIPI D-PHY		
DPHY[num]_CK[P/N]	I/O	MIPI D-PHY Clock [num] = D-PHY 0 or 1, P = Positive, N = Negative.
DPHY[num]_D[P/N][lane]	I/O	MIPI D-PHY Data [num] = D-PHY 0 or 1, P = Positive, N = Negative, Lane = data lane in the D-PHY block 0, 1, 2 or 3.

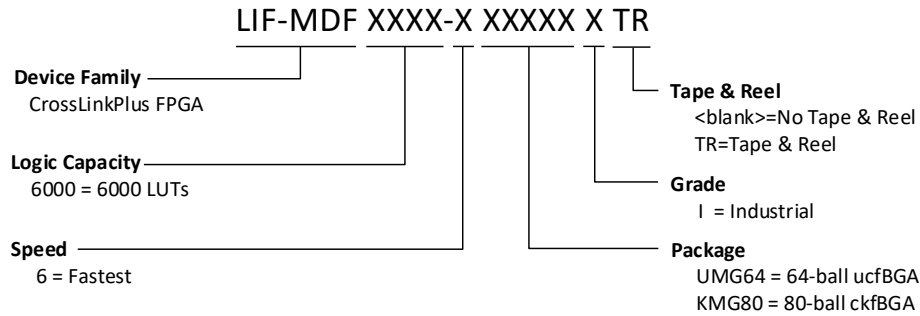
5.3. Pin Information Summary

Table 5.3. Pin Information Summary

Pin Type	CrossLinkPlus	
	ucfBGA64	ckfBGA80
Total General Purpose I/O	29	37
VCC/VCCIOx/VCCAUX/VCCGPLL	8	9
GND	3	6
D-PHY Clock/Data	20	20
D-PHY VCC	2	4
D-PHY GND	1	3
CRESET_B	1	1
Total Balls	64	80
Bank 0	7	7
Bank 1	10	14
Bank 2	12	16
Total General Purpose Single Ended I/O	29	37
Bank 0	0	0
Bank 1	5	7
Bank 2	6	8
Total General Purpose Differential I/O Pairs	11	15

6. Ordering Information

6.1. CrossLinkPlus Part Number Description



6.2. Ordering Part Numbers

Industrial

Part Number	Grade	Package	Pins	Temp.	LUTs (K)
LIF-MDF6000-6UMG64I	-6	Lead free ucfBGA	64	Industrial	5.9
LIF-MDF6000-6KMG80I	-6	Lead free ckfBGA	80	Industrial	5.9

References

For more information, refer to the following technical notes:

- [CrossLinkPlus High-Speed I/O Interface \(FPGA-TN-02102\)](#)
- [CrossLinkPlus Hardware Checklist \(FPGA-TN-02105\)](#)
- [CrossLinkPlus Programming and Configuration Usage Guide \(FPGA-TN-02103\)](#)
- [CrossLinkPlus sysCLOCK PLL/DLL Design and Usage Guide \(FPGA-TN-02109\)](#)
- [CrossLinkPlus sysI/O Usage Guide \(FPGA-TN-02108\)](#)
- [CrossLinkPlus Memory Usage Guide \(FPGA-TN-02110\)](#)
- [Power Management and Calculation for CrossLinkPlus Devices \(FPGA-TN-02111\)](#)
- [CrossLinkPlus I2C Hardened IP Usage Guide \(FPGA-TN-02112\)](#)
- [Advanced CrossLinkPlus I²C Hardened IP Reference Guide \(FPGA-TN-02135\)](#)

For package information, refer to the following technical notes:

- [PCB Layout Recommendations for BGA Packages \(FPGA-TN-02024\)](#)
- [Solder Reflow Guide for Surface Mount Devices \(FPGA-TN-02041\)](#)
- [Wafer-Level Chip-Scale Package Guide \(TN1242\)](#)
- [Thermal Management \(FPGA-TN-02044\)](#)
- [Package Diagrams \(FPGA-DS-02053\)](#)

For further information, refer to the following websites:

- JEDEC Standards (LVTTL, LVCMOS): www.jedec.org
- MIPI Standards (D-PHY): www.mipi.org
- [Lattice Insights](#) for Lattice Semiconductor training courses and learning plans

Technical Support

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.2, October 2023

Section	Change Summary
Disclaimers	Updated with the latest disclaimers.
References	Added link to the Lattice Insights webpage.
Technical Support	Added link to the Lattice Answer Database webpage.

Revision 1.1, February 2022

Section	Change Summary
DC and Switching Characteristics	Added Figure 4.6. SPI Timing Waveforms.

Revision 1.0, August 2021

Section	Change Summary
All	Production release.
DC and Switching Characteristics	<ul style="list-style-type: none"> Updated the CrossLinkPlus Maximum General Purpose I/O Buffer Speed section. Added information regarding the Diamond Software PAR Design Strategy settings. Updated note in Table 4.22. Flash Programming/Erase Specifications. <ul style="list-style-type: none"> Indicated the NPROGCYC maximum values. Indicated the maximum Flash memory read cycle limit in footnote.
Ordering Information	Placed CrossLinkPlus Part Number Description and Ordering Part Numbers under this heading.
—	Minor formatting changes.

Revision 0.92, March 2021

Section	Change Summary
General Description	<ul style="list-style-type: none"> Added 80-ball ckfBGA (49 mm²) under <i>Ultra small footprint packages</i> in the Features section. Added 80-ball ckfBGA in Table 2.1. CrossLinkPlus Feature Summary.
Signal Descriptions	Added 80-ball ckfBGA in Table 5.3. Pin Information Summary.
CrossLinkPlus Part Number Description	Added LIF-MDF6000-6KMG80I in Ordering Part Numbers.

Revision 0.91, January 2020

Section	Change Summary
Acronyms in This Document	Added/revised acronyms and descriptions.
Architecture Overview	<ul style="list-style-type: none"> In the section introduction, mentioned internal Flash as key system resource. In the Programming and Configuration sub-section, updated information on CRESET_B pin and Dual Boot Support.
DC and Switching Characteristics	<ul style="list-style-type: none"> Updated V_{CCAUX} information in and removed footnote from Table 4.1. Absolute Maximum Ratings. Removed footnote from Table 4.2. Recommended Operating Conditions. Updated values in Table 4.4. Power-On-Reset Voltage Levels. Updated footnote 7 in Table 4.12. CrossLinkPlus Maximum I/O Buffer Speed.
—	Minor formatting and editorial changes.

Revision 0.90, September 2019

Section	Change Summary
All	Preliminary release.



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