



# SP690T/S/R, SP802T/S/R, SP804T/S/R, and SP805T/S/R

## 3.0V/3.3V Low Power Microprocessor Supervisory with Battery Switch-Over

- **RESET** and **RESET** Outputs
- Reset asserted down to  $V_{CC} = 1V$
- Reset Time Delay - 200ms
- Watchdog Timer - 1.6 sec timeout
- **40 $\mu$ A Maximum  $V_{CC}$  Supply Current**
- **1 $\mu$ A Maximum Battery Supply Current**
- **Power Switching**
  - 50mA Output in  $V_{CC}$  Mode (1.5 $\Omega$ )**
  - 10mA Output in Battery Mode (15 $\Omega$ )**
- Battery Can Exceed  $V_{CC}$  in Normal Operation
- Precision Voltage Monitor for Power-Fail or Low-Battery Warning
- Available in 8 pin SO and DIP packages
- Pin Compatible Upgrades to  
MAX690T/S/R, MAX802T/S/R,  
MAX804T/S/R, MAX805T/S/R



### DESCRIPTION

The **SP690T/S/R**, **SP802T/S/R**, **SP804T/S/R** and **SP805T/S/R** devices are a family of microprocessor ( $\mu$ P) supervisory circuits that integrate a myriad of components involved in discrete solutions to monitor power-supply and battery-control functions in  $\mu$ P and digital systems. The series will significantly improve system reliability and operational efficiency when compared to discrete solutions. The features of the **SP690T/S/R**, **SP802T/S/R**, **SP804T/S/R** and **SP805T/S/R** devices include a watchdog timer, a  $\mu$ P reset and backup-battery switchover, and power-failure warning; a complete  $\mu$ P monitoring and watchdog solution. The series is ideal for 3.0V or 3.3V applications in portable electronics, computers, controllers, and intelligent instruments and is a solid match for designs where it is critical to monitor the power supply to the  $\mu$ P and it's related digital components. Refer to **Sipex's SP690A/692A/802L/802M/805L/805M** series for similar devices designed for +5V systems.

Part Number	RESET Active	RESET Threshold	RESET Accuracy	PFI Accuracy	Watchdog Input	Backup-Battery Switch
SP690T/805T	LOW/HIGH	3.075V	$\pm 75mV$	$\pm 4\%$	YES	YES
SP802T/804T	LOW/HIGH	3.075V	$\pm 60mV$	$\pm 2\%$	YES	YES
SP690S/805S	LOW/HIGH	2.925V	$\pm 75mV$	$\pm 4\%$	YES	YES
SP802S/804S	LOW/HIGH	2.925V	$\pm 60mV$	$\pm 2\%$	YES	YES
SP690R/805R	LOW/HIGH	2.625V	$\pm 75mV$	$\pm 4\%$	YES	YES
SP802R/804R	LOW/HIGH	2.625V	$\pm 60mV$	$\pm 2\%$	YES	YES

## ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

$V_{CC}$ .....-0.3V to 6.0V  
 $V_{BATT}$ .....-0.3V to 6.0V  
 All Other Inputs (NOTE 1).....-0.3V to the higher of  $V_{CC}$  or  $V_{BATT}$

Continuous Input Current:

$V_{CC}$ .....100mA  
 $V_{BATT}$ .....20mA  
 GND.....20mA  
 WDI, PFI.....20mA

Continuous Output Current:

RESET, RESET, PFO.....20mA  
 $V_{OUT}$ .....100mA

Power Dissipation per Package:

8pin NSOIC (derate 6.14mW/°C above +70°C).....500mW  
 8pin PDIP (derate 11.8mW/°C above +70°C).....1,000mW  
 Storage Temperature.....-65°C to +160°C

Lead Temperature(soldering,10sec).....+300°C

ESD Rating.....4KV Human Body Model



### CAUTION:

ESD (ElectroStatic Discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Personnel should be properly grounded prior to handling this device. The protective foam should be discharged to the destination socket before devices are removed.

## SPECIFICATIONS

$V_{CC}$  = 3.17V to 5.50V for the SP690T/SP80\_T,  $V_{CC}$  = 3.02V to 5.50V for the SP690S/SP80\_S,  $V_{CC}$  = 2.72V to 5.50V for the SP690R/SP80\_R,  $V_{BATT}$  = 3.60V, and  $T_A$  =  $T_{MIN}$  to  $T_{MAX}$  unless otherwise noted. Typical values taken at  $T_{AMB}$  = +25°C

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Operating Voltage Range, $V_{CC}$ or $V_{BATTERY}$ , NOTE 1	1.0		5.5	Volts	
$V_{CC}$ Supply Current, $I_{SUPPLY}$		25	40	$\mu$ A	excluding $I_{OUT}$
$V_{CC}$ Supply Current in Battery Backup Mode		20	40	$\mu$ A	$V_{CC}=2.0V, V_{BATTERY}=2.3V$ , excluding $I_{OUT}$
$V_{BATTERY}$ Supply Current in Any Mode, NOTE 2		0.4	1	$\mu$ A	excluding $I_{OUT}$
$V_{BATTERY}$ Leakage Current, NOTE 3		0.001	0.5	$\mu$ A	
$V_{BATTERY}$ Leakage Current, NOTE 4	-0.1		0.02	$\mu$ A	$3.3V > V_{CC} > V_{BATTERY} + 0.2V$
Output Voltage, $V_{OUT}$	$V_{CC} - 0.03$ $V_{CC} - 0.3$ $V_{CC} - 0.0015$	$V_{CC} - 0.0075$ $V_{CC} - 0.075$ $V_{CC} - 0.0003$		V	$I = 5mA$ $I_{OUT} = 50mA$ $I_{OUT} = 250\mu A, V_{CC} > 2.5V$
$V_{OUT}$ in Battery-Backup Mode	$V_{BATTERY} - 0.02$	$V_{BATTERY} - 0.0045$ $V_{BATTERY} - 0.018$ $V_{BATTERY} - 0.15$		V	$I_{OUT} = 250\mu A, V_{BATTERY} = 2.3V$ $I_{OUT} = 1mA, V_{BATTERY} = 2.3V$ $I_{OUT} = 10mA, V_{BATTERY} = 3.3V$
Battery Switch Threshold, $V_{CC}$ falling	0.065 2.30	0.025 2.40	2.50	V	$V_{BATTERY} - V_{CC}, V_{SW} > V_{CC} > 1.75V$ , NOTE 5 $V_{BATTERY} > V_{CC}$ , NOTE 6
Battery Switch Threshold, $V_{CC}$ rising, NOTE 7				V	Values are identical to the Reset Threshold values at $V_{CC}$ rising

## SPECIFICATIONS (continued)

$V_{CC} = 3.17V$  to  $5.50V$  for the SP690T/SP80\_T,  $V_{CC} = 3.02V$  to  $5.50V$  for the SP690S/SP80\_S,  $V_{CC} = 2.72V$  to  $5.50V$  for the SP690R/SP80\_R,  $V_{BATT} = 3.60V$ , and  $T_A = T_{MIN}$  to  $T_{MAX}$  unless otherwise noted. Typical values taken at  $T_{AMB} = +25^{\circ}C$ .

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS	
Reset Threshold, $V_{RST}$ NOTE 8	3.00	3.075	3.15	V	SP690T/805T, $V_{CC}$ falling	
	3.00	3.085	3.17		SP690T/805T, $V_{CC}$ rising	
	2.85	2.925	3.00		SP690S/805S, $V_{CC}$ falling	
	2.85	2.935	3.02		SP690S/805S, $V_{CC}$ rising	
	2.55	2.625	2.70		SP690R/805R, $V_{CC}$ falling	
	2.55	2.635	2.72		SP690R/805R, $V_{CC}$ rising	
		3.00	3.075	3.12	V	SP802T/804T, $V_{CC}$ falling
		3.00	3.085	3.14		SP802T/804T, $V_{CC}$ rising
		2.88	2.925	3.00		SP802S/804S, $V_{CC}$ falling
		2.88	2.935	3.02		SP802S/804S, $V_{CC}$ rising
		2.59	2.625	2.70		SP802R/804R, $V_{CC}$ falling
		2.59	2.635	2.72		SP802R/804R, $V_{CC}$ rising
Reset Timeout Period, $t_{WP}$	140	200	280	ms		
$\overline{RESET}$ , $\overline{PFO}$ Output Voltage, $V_{OH}$	$V_{CC} - 0.3$	$V_{CC} - 0.15$		V	$I_{SOURCE} = 30\mu A$	
$\overline{RESET}$ , $\overline{PFO}$ Output Voltage, $V_{OL}$		0.06	0.30	V	$I_{SINK} = 1.2mA$ , SP690_/802_ where $V_{CC} = V_{RST}$ minimum	
$\overline{RESET}$ , $\overline{PFO}$ Output Voltage, $V_{OL}$		0.13	0.30	V	$V_{BATTERY} = 0V$ , $V_{CC} = 1.0V$ , $I_{SINK} = 40\mu A$	
RESET Output Voltage, $V_{OL}$		0.06	0.30	V	$I_{SINK} = 1.2mA$ , SP804_/805_ where $V_{CC} = V_{RST}$ maximum	
RESET Output Leakage Current, NOTE 11	-1		-1	$\mu A$	$V_{BATTERY} = 0V$ , $V_{CC} = V_{RST}$ minimum, $V_{RESET} = 0V$ or $V_{CC}$	
Output Short to GND Current, $I_{OS}$ , PFO and RESET		180	500	$\mu A$	$V_{CC} = 3.3V$ , $V_{OH} = 0V$	
Watchdog Timeout, $t_{WD}$	1.12	1.60	2.24	s	$V_{CC} < 3.6V$	
WDI Pulse Width	1			$\mu s$		
WDI Input Threshold $V_{IH}$ $V_{IL}$			$0.7 \times V_{CC}$	V	$0.3 \times V_{CC}$	
WDI Input Current	-1	0.01	1	$\mu A$	$0V < V_{CC} < 5.5V$	
PFI Input Threshold	1.200 1.225	1.25 1.25	1.300 1.275	V	SP690_/805_, $V_{CC} \leq 3.6V$ , $V_{PFI}$ falling SP802_/804_, $V_{CC} \leq 3.6V$ , $V_{PFI}$ falling	
PFI Input Current	-25	0.01	25	nA		
PFI Hysteresis, $V_{PFH}$		10	20	mV	PFI rising, $V_{CC} \leq 3.6V$	

## SPECIFICATIONS (continued)

$V_{CC} = 3.17V$  to  $5.50V$  for the SP690T/SP80\_T,  $V_{CC} = 3.02V$  to  $5.50V$  for the SP690S/SP80\_S,  $V_{CC} = 2.72V$  to  $5.50V$  for the SP690R/SP80\_R,  $V_{BATT} = 3.60V$ , and  $T_A = T_{MIN}$  to  $T_{MAX}$  unless otherwise noted. Typical values taken at  $T_{AMB} = +25^{\circ}C$ .

**NOTE 1:** The following are tested at  $V_{BATT} = 3.6V$  and  $V_{CC} = 5.5V$ :  $V_{CC}$  supply current, watchdog functionality, logic input leakage, PFI functionality, and the  $\overline{RESET}$  and RESET states. The state of  $\overline{RESET}$  or RESET and PFO is tested at  $V_{CC} = V_{CC}(\min)$ .

**NOTE 2:** Tested  $V_{BATT} = 3.6V$ ,  $V_{CC} = 3.5V$  and  $0V$ .

**NOTE 3:** Leakage current into the battery is tested under the following worst-case conditions:  $V_{CC} = 5.5V$ ,  $V_{BATT} = 1.8V$  and at  $V_{CC} = 1.5V$ ,  $V_{BATT} = 1.0V$ .

**NOTE 4:** "-" equals the battery-charging current, "+" equals the battery-discharging current.

**NOTE 5:** When  $V_{SW} > V_{CC} > V_{BATT}$ ,  $V_{OUT}$  remains connected to  $V_{CC}$  until  $V_{CC}$  drops below  $V_{BATT}$ . The  $V_{CC}$ -to- $V_{BATT}$  comparator has a small 25mV typical hysteresis to prevent oscillation.

**NOTE 6:** When  $V_{BATT} > V_{CC} > V_{SW}$ ,  $V_{OUT}$  remains connected to  $V_{CC}$  until  $V_{CC}$  drops below the battery switch threshold,  $V_{SW}$ .

**NOTE 7:**  $V_{OUT}$  switches from  $V_{BATT}$  to  $V_{CC}$  when  $V_{CC}$  rises above the reset threshold, independent of  $V_{BATT}$ . Switchover back to  $V_{CC}$  occurs at the exact voltage that causes  $\overline{RESET}$  to go HIGH (on the SP804\_ and SP805\_ RESET goes LOW). Switchover occurs 200ms prior to reset.

**NOTE 8:** The reset threshold tolerance is wider for  $V_{CC}$  rising than for  $V_{CC}$  falling to accommodate the 10mV typical hysteresis, which prevents internal oscillation.

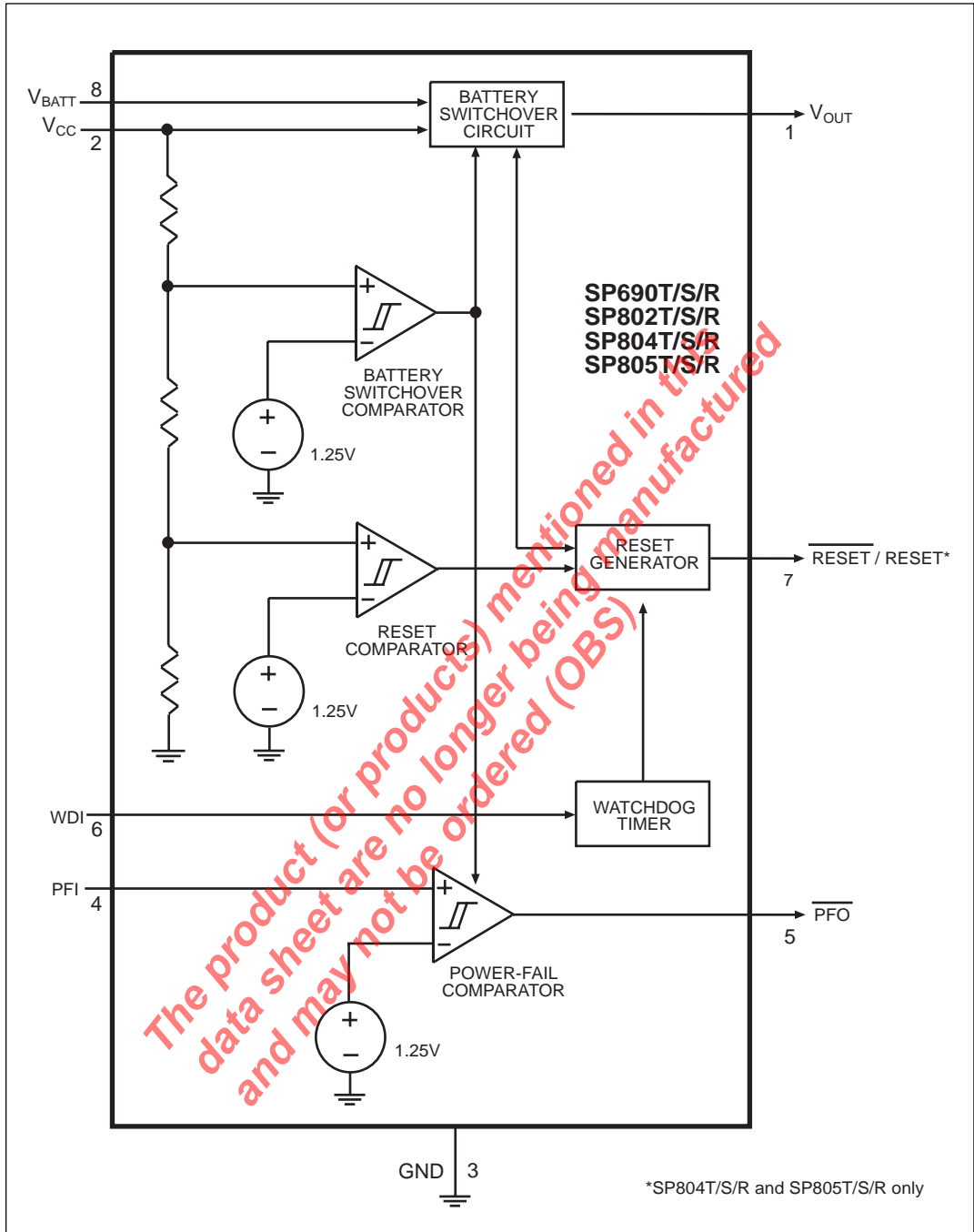
**NOTE 9:** SP690\_ and SP802\_ devices only.

**NOTE 10:** SP804\_ and SP805\_ devices only.

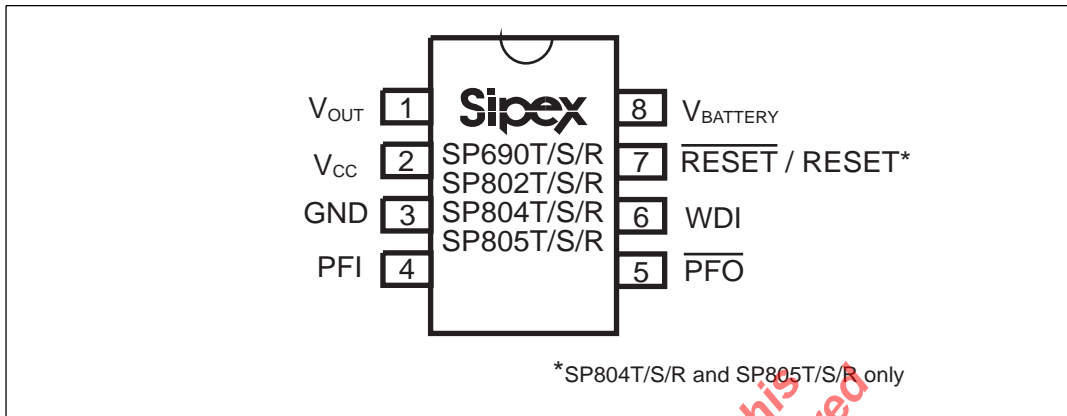
**NOTE 11:** The leakage current into or out of the RESET pin is tested with RESET asserted (RESET output high impedance).

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

# INTERNAL BLOCK DIAGRAM



## PINOUT



## PIN ASSIGNMENTS

Pin 1 —  $V_{OUT}$  — Output Supply Voltage for CMOS RAM. When  $V_{CC}$  is above the reset threshold,  $V_{OUT}$  connects to  $V_{CC}$  through a P-channel MOSFET switch. When  $V_{CC}$  falls below the  $V_{SW}$  and  $V_{BATTERY}$ ,  $V_{BATTERY}$  connects to  $V_{OUT}$ . Connect to  $V_{CC}$  if no battery is used.

Pin 2 —  $V_{CC}$  — +5V Supply Input

Pin 3 — GND — Ground reference for all signals

Pin 4 — PFI — Power-Fail Comparator Input. When PFI is less than 1.25V or when  $V_{CC}$  falls below the  $V_{SW}$ , PFO goes LOW, otherwise PFO remains HIGH. Connect to GND if unused.

Pin 5 —  $\overline{PFO}$  — Power-Fail Comparator Output. Leave open if unused.

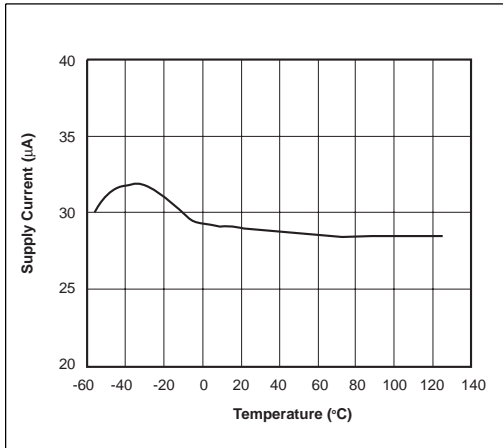
Pin 6 — WDI — Watchdog Input. If WDI remains HIGH or LOW for 1.6 seconds, the internal watchdog timer triggers a reset. The internal watchdog timer clears when reset is asserted or WDI sees a rising or falling edge. **The watchdog function cannot be disabled.**

Pin 7 for **SP690 /802\_ only** — Active-LOW Reset Output. — Whenever RESET is triggered by a watchdog timeout, it goes LOW for 200ms. It stays LOW whenever  $V_{CC}$  is below the reset threshold and remains LOW for 200ms after  $V_{CC}$  rises above the reset threshold or when the watchdog triggers a reset.

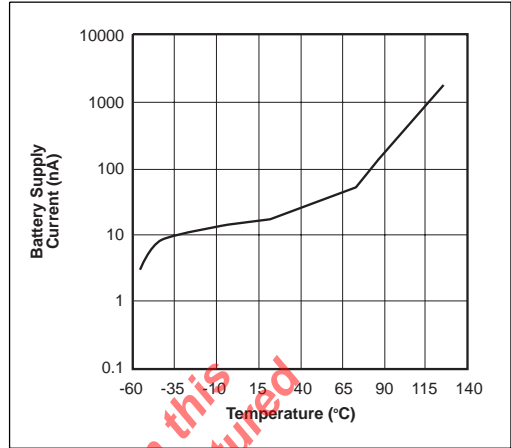
Pin 7 for **SP804 /805\_ only** — Active-HIGH Open-Drain Reset Output. — The inverse operation of RESET.

Pin 8 —  $V_{BATTERY}$  — Backup-Battery Input. When  $V_{CC}$  falls below  $V_{SW}$  and  $V_{BATTERY}$ ,  $V_{OUT}$  switches from  $V_{CC}$  to  $V_{BATTERY}$ . When  $V_{CC}$  rises above the reset threshold,  $V_{OUT}$  reconnects to  $V_{CC}$ .  $V_{BATTERY}$  may exceed  $V_{CC}$ . Connect to  $V_{CC}$  if no battery is used.

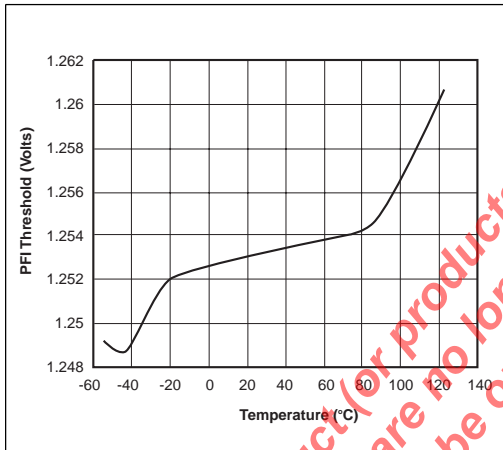
**TYPICAL CHARACTERISTICS ( $T_{AMB} = 25^{\circ}\text{C}$ , unless otherwise noted)**



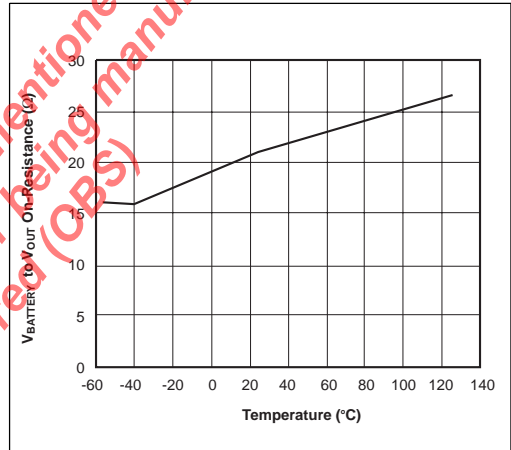
**Figure 1.  $V_{CC}$  Supply Current vs. Temperature (Normal Mode)**



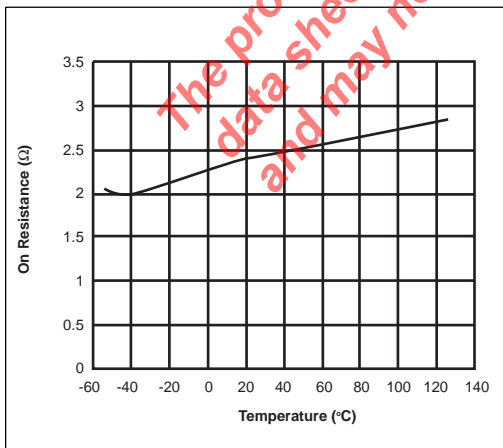
**Figure 2. Battery Supply Current vs. Temperature**



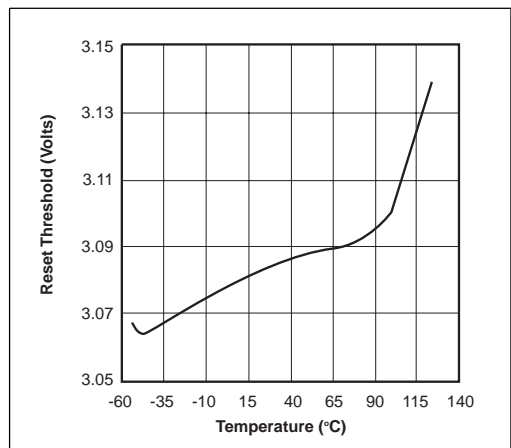
**Figure 3. PFI Threshold vs. Temperature**



**Figure 4.  $V_{BATTERY}$  to  $V_{OUT}$  ON-Resistance vs. Temperature**



**Figure 5.  $V_{CC}$  to  $V_{OUT}$  On-Resistance vs. Temperature**



**Figure 6. Reset Threshold vs. Temperature**

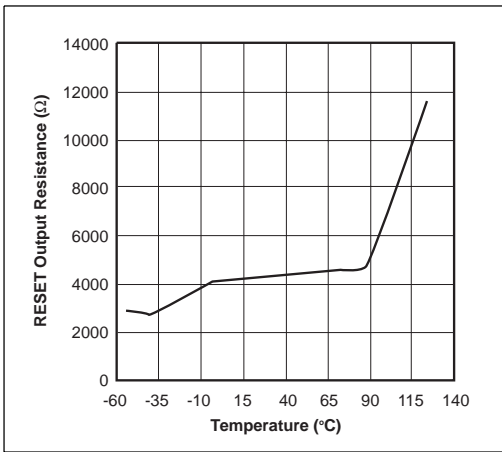


Figure 7. Reset Output Resistance vs. Temperature

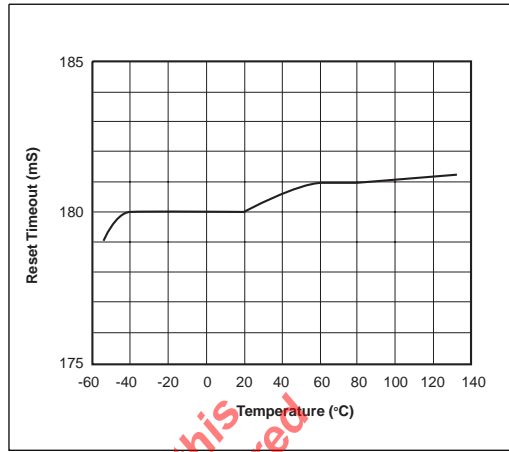


Figure 8. Reset Timeout vs. Temperature

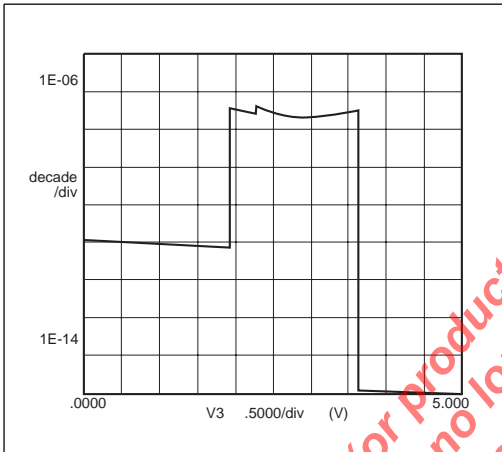


Figure 9. Battery Current vs.  $V_{CC}$  Voltage

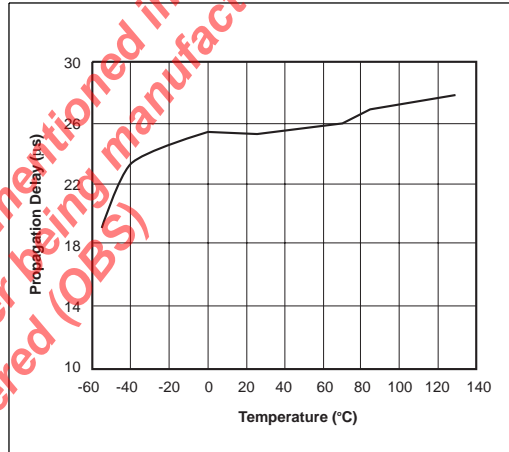


Figure 10. Reset-Comparator Propagation Delay vs. Temperature

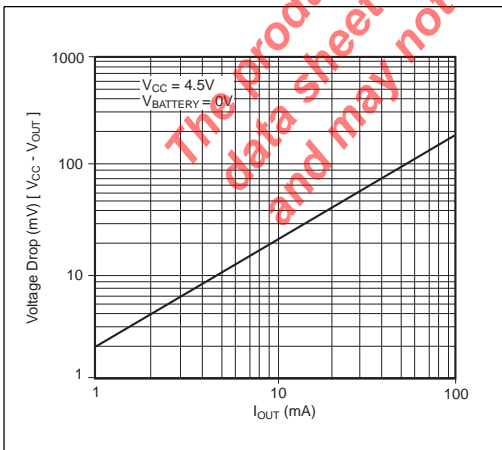


Figure 11.  $V_{CC}$  to  $V_{OUT}$  Vs. Output Current

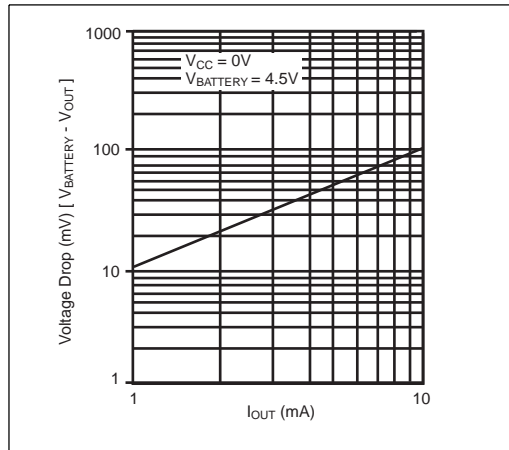


Figure 12.  $V_{BATTERY}$  to  $V_{OUT}$  Vs. Output Current



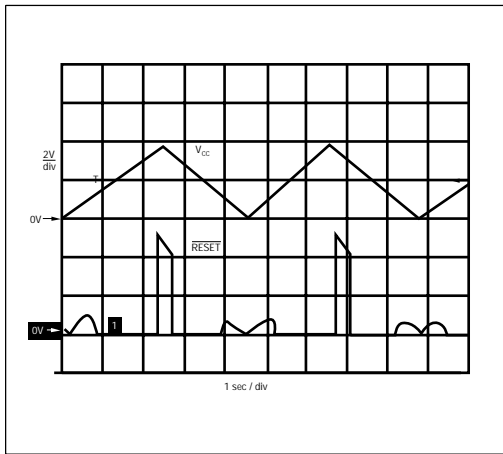


Figure 13A. SP690A  $\overline{\text{RESET}}$  Output Voltage vs. Supply Voltage

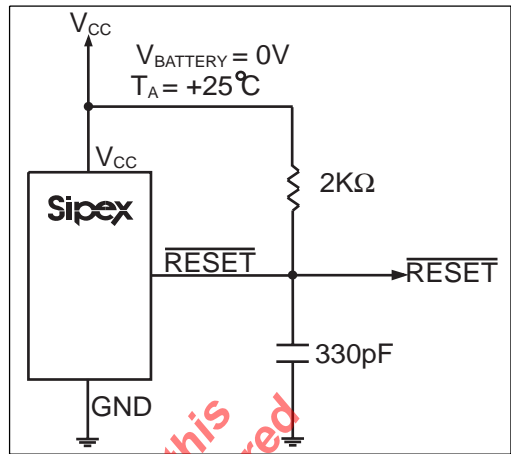


Figure 13B. Circuit for the SP690A/802L  $\overline{\text{RESET}}$  Output Voltage vs. Supply Voltage

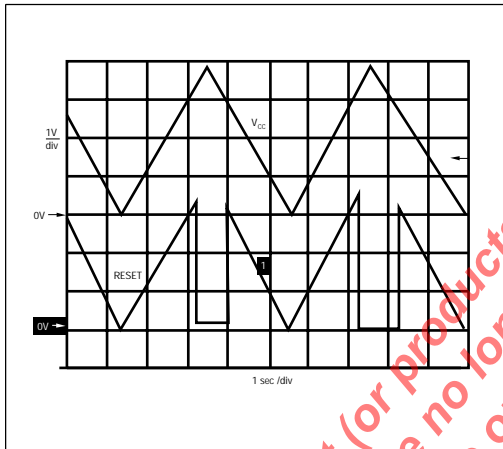


Figure 14A. SP805L  $\overline{\text{RESET}}$  Output Voltage vs. Supply Voltage

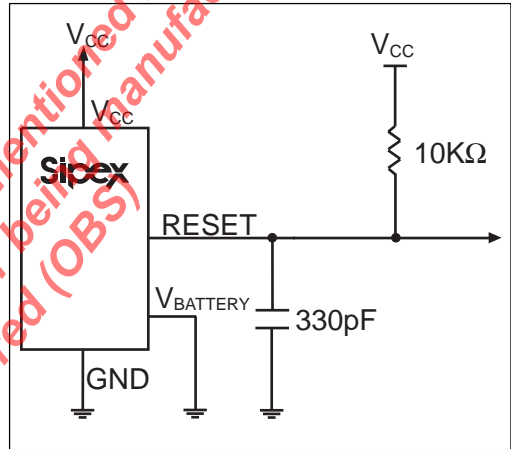


Figure 14B. Circuit for the SP805  $\overline{\text{RESET}}$  Output Voltage vs. Supply Voltage

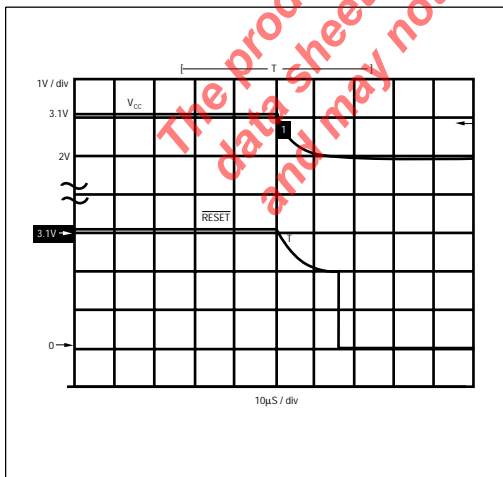


Figure 15A. SP690A  $\overline{\text{RESET}}$  Response Time

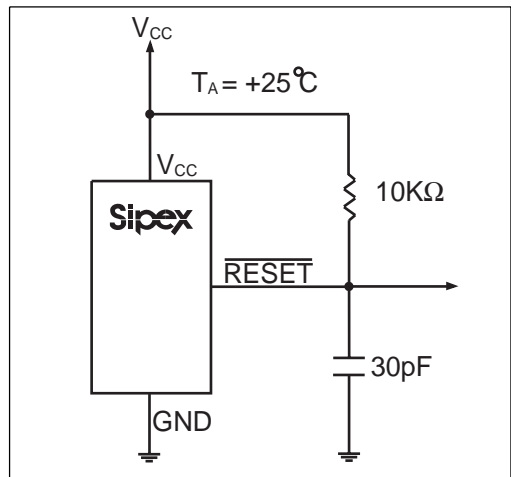


Figure 15B. Circuit for the SP690A/802L  $\overline{\text{RESET}}$  Response Time

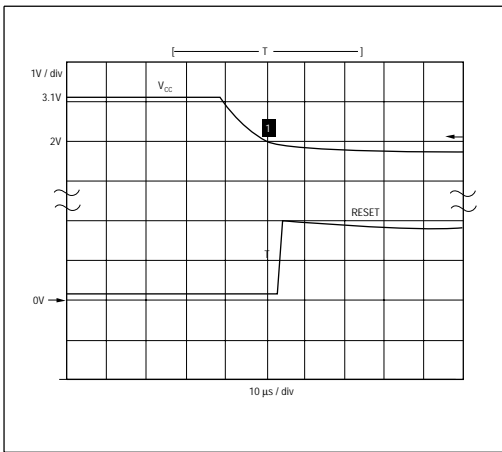


Figure 16A. SP805L RESET Response Time

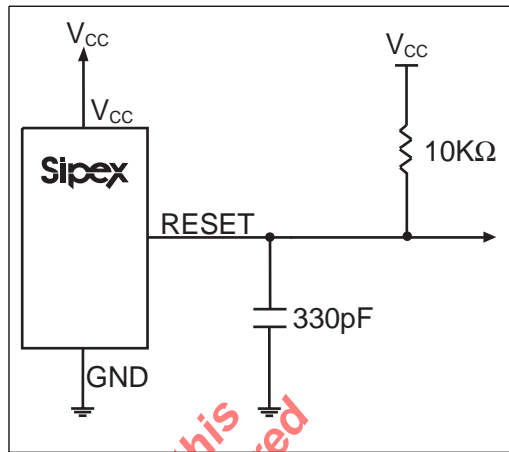


Figure 16B. Circuit for the SP805L RESET Response Time

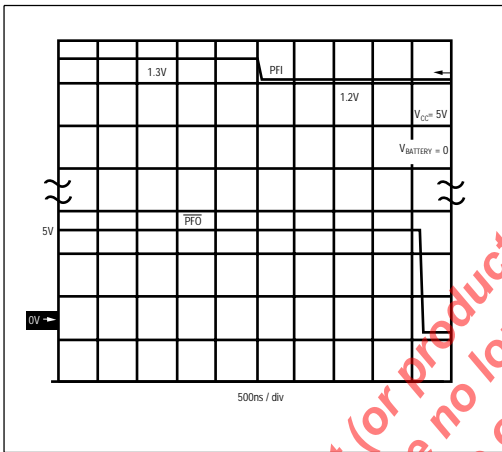


Figure 17A. Power-Fail Comparator Response Time (fall)

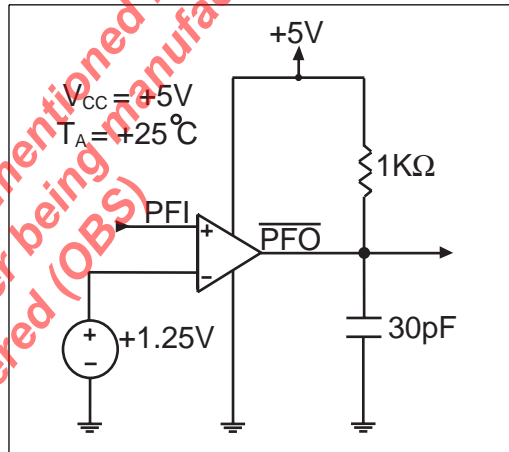


Figure 17B. Circuit for the Power-Fail Comparator Response Time (fall)

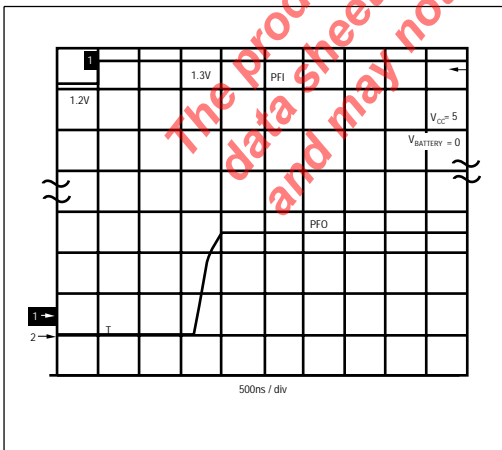


Figure 18A. Power-Fail Comparator Response Time (rise)

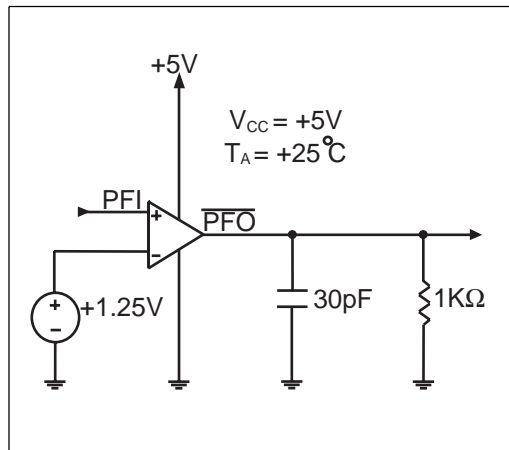


Figure 18B. Circuit for the Power-Fail Comparator Response Time (rise)

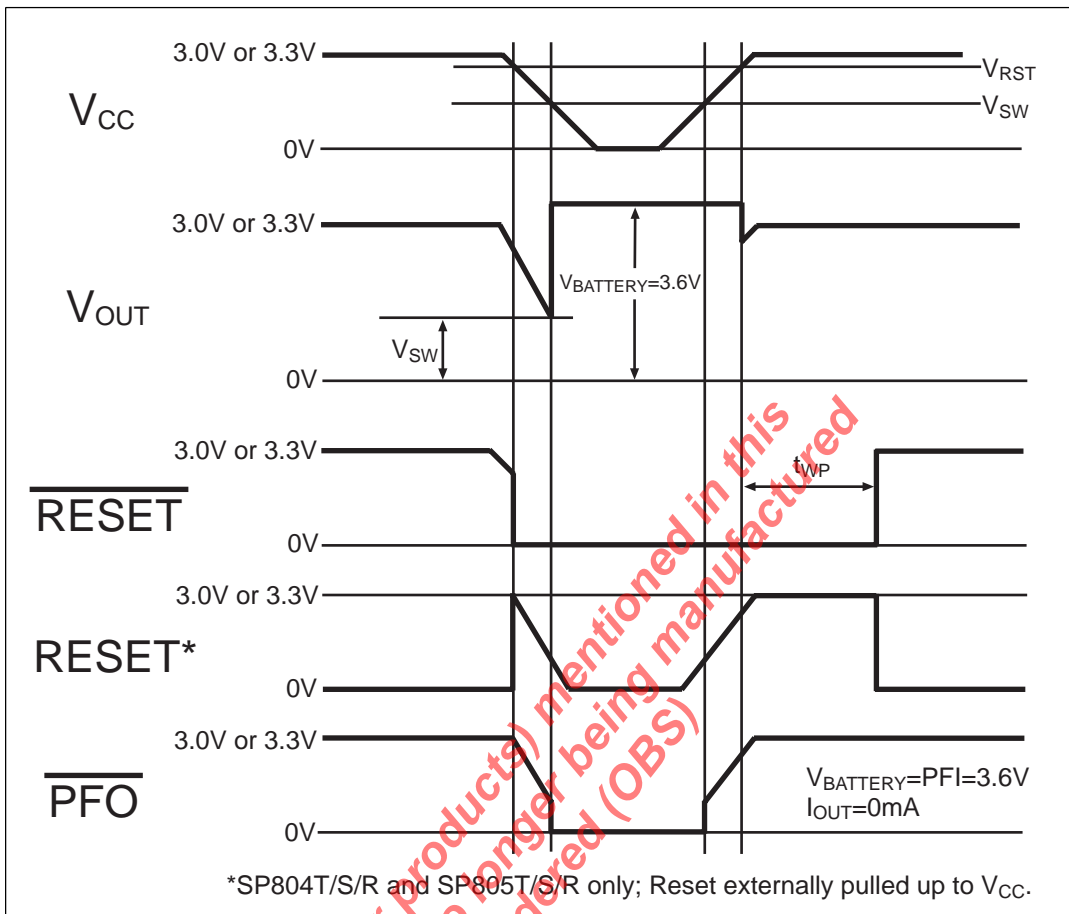


Figure 19. Timing Diagram

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

## FEATURES

The **SP690T/S/R**, **SP802T/S/R**, **SP804T/S/R** and **SP805T/S/R** devices provide four key functions:

1. A battery backup switch for CMOS RAM, CMOS microprocessors, or other logic.
2. A reset output during power-up, power-down and brownout conditions.
3. A reset pulse if the optional watchdog timer has not been toggled within a specified time.
4. A 1.25V threshold detector for power-fail warning, low battery detection, or to monitor a power supply other than 3.3V or 3.0V.

The **SP690T/S/R**, **SP802T/S/R**, **SP804T/S/R** and **SP805T/S/R** devices differ in their reset-voltage threshold levels and are ideally suited for applications in automotive systems, intelligent instruments, and battery-powered computers and controllers. The series is a solid match for designs where it is critical to monitor the power supply to the  $\mu\text{P}$  and it's related digital components.

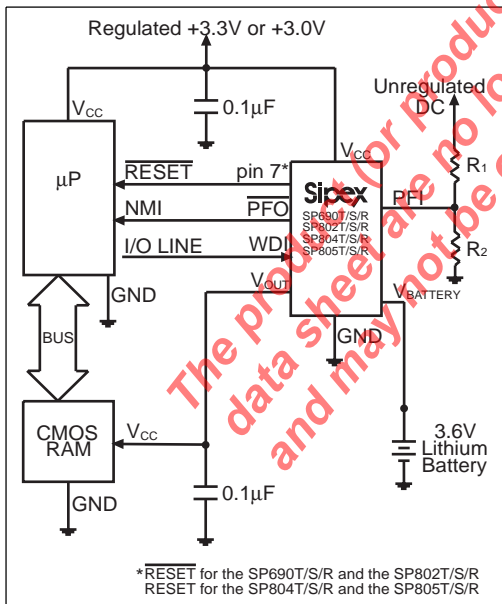


Figure 20. Typical Operating Circuit

## THEORY OF OPERATION

The **SP690T/S/R**, **SP802T/S/R**, **SP804T/S/R** and **SP805T/S/R** devices are microprocessor ( $\mu\text{P}$ ) supervisory circuits that monitor the power supplied to digital circuits such as microprocessors, microcontrollers, or memory. The series is an ideal solution for portable, battery-powered equipment that requires power supply monitoring. Implementing this series will reduce the number of components and overall complexity. The watchdog functions of this product family will continuously oversee the operational status of a system.

These  $\mu\text{P}$  supervisory circuits are not short-circuit protected. Shorting  $V_{\text{OUT}}$  to ground - excluding power-up transients such as charging a decoupling capacitor - may potentially damage these devices. Decouple both  $V_{\text{CC}}$  and  $V_{\text{BATTERY}}$  pins to ground by placing  $0.1\mu\text{F}$  capacitors as close to the device as possible. The operational features and benefits of the **SP690T/S/R**, **SP802T/S/R**, **SP804T/S/R** and **SP805T/S/R** devices are described in more detail below.

### Reset Output

The microprocessor's ( $\mu\text{P}$ 's) reset input starts the  $\mu\text{P}$  in a known state. When the  $\mu\text{P}$  is in an unknown state, it should be held in reset. The **SP690T/S/R**, **SP802T/S/R**, **SP804T/S/R** and **SP805T/S/R** devices assert reset during power-up and prevent code execution errors during power-down or brownout conditions.

$\overline{\text{RESET}}$  is guaranteed to be a logic LOW for  $0\text{V} < V_{\text{CC}} < V_{\text{RST}}$ , provided that  $V_{\text{BATTERY}}$  is greater than 1V. Without a backup battery,  $\overline{\text{RESET}}$  is guaranteed valid for  $V_{\text{CC}} > 1\text{V}$ . Once  $V_{\text{CC}}$  exceeds the reset threshold, an internal timer keeps  $\overline{\text{RESET}}$  low for the reset timeout period. After this period,  $\overline{\text{RESET}}$  goes HIGH, as seen in Figure 19.

If a brownout condition occurs and  $V_{\text{CC}}$  dips below the reset threshold,  $\overline{\text{RESET}}$  goes LOW. Each time  $\overline{\text{RESET}}$  is triggered, it stays low for the reset timeout period. Any time  $V_{\text{CC}}$  goes below the reset threshold, the internal timer restarts.

The watchdog timer can also initiate a reset. Refer to the **Watchdog Input** section.

The **SP804T/S/R** and **SP805T/S/R** active-HIGH RESET output is open drain and the inverse of the **SP690T/S/R** and **SP802T/S/R** RESET outputs.

$\overline{\text{RESET}}$  is also triggered by a watchdog timeout. If WDI remains either high or low for a period that exceeds the watchdog timeout period (1.6 sec),  $\overline{\text{RESET}}$  pulses low for 200mS. As long as  $\overline{\text{RESET}}$  is asserted, the watchdog timer remains cleared. When  $\overline{\text{RESET}}$  comes high, the watchdog resumes timing and must be serviced within 1.6sec. If WDI is tied high or low, a RESET pulse is triggered every 1.8sec ( $t_{\text{WD}}$  plus  $t_{\text{RS}}$ ).

### Reset Threshold

The **SP690T** and **SP805T** devices are designed for 3.3V systems with a  $\pm 5\%$  power-supply tolerance and a 10% system tolerance. Except for watchdog faults, reset will not assert as long as the power supply remains above 3.15V (3.3V - 5%). Reset is guaranteed to assert before the power supply falls below 3.0V.

The **SP690S** and **SP805S** devices are designed for 3.3V  $\pm 10\%$  power supplies. Except for watchdog faults, they are guaranteed not to assert reset as long as the supply remains above 3.0V (3.3V - 10%). Reset is guaranteed to assert before the power supply fails below 2.85V ( $V_{\text{CC}}$  - 14%).

The **SP690R** and **SP805R** devices are optimized for monitoring 3.0V  $\pm 10\%$  power supplies. Reset will not occur until  $V_{\text{CC}}$  falls below 2.7V (3.0V - 10%), but is guaranteed to occur before the supply falls below 2.55V (3.0V - 15%).

The **SP802T/S/R** and **SP804T/S/R** devices are respectively similar to the **SP690T/S/R** and **SP805T/S/R** devices with tightened reset and power-fail threshold tolerances.

### Watchdog Input

The watchdog circuit monitors the  $\mu\text{P}$ 's activity. If the  $\mu\text{P}$  does not toggle the watchdog input (WDI) within 1.6sec, a reset pulse is triggered. The internal 1.6sec timer is cleared by either a reset pulse or by a transition (LOW-to-HIGH or HIGH-to-LOW) at WDI. If WDI is tied HIGH or LOW, a  $\overline{\text{RESET}}$  pulse is triggered every 1.8sec ( $t_{\text{WD}}$  plus  $t_{\text{RS}}$ ).

As long as reset is asserted, the timer remains cleared and does not count. As soon as reset is de-asserted, the timer starts counting. Unlike the 5V **SP690A** series, the watchdog function **cannot** be disabled.

### Power-Fail Comparator

The power-fail comparator can be used as an under-voltage detector to signal the failing of a power supply (it is completely separate from the rest of the circuitry and does not need to be dedicated to this function). The PFI input is compared to an internal 1.25V. If PFI is less than  $V_{\text{PFT}}$ , PFO goes low.

The power-fail comparator turns off and  $\overline{\text{PFO}}$  goes LOW when  $V_{\text{CC}}$  falls below  $V_{\text{SW}}$  on power-down. The power-fail comparator turns on as  $V_{\text{CC}}$  crosses  $V_{\text{SW}}$  on power-up. If the comparator is not used, connect PFI to ground and leave PFO unconnected.

### Backup-Battery Switchover

In the event of a brownout or power failure, it may be necessary to preserve the contents of RAM. With a backup battery installed at  $V_{\text{BATTERY}}$ , the devices automatically switch RAM to backup power when  $V_{\text{CC}}$  fails.

This family of  $\mu\text{P}$  supervisors (designed for 3.3V and 3V systems) doesn't always connect  $V_{\text{BATTERY}}$  to  $V_{\text{OUT}}$  when  $V_{\text{BATTERY}}$  is greater than  $V_{\text{CC}}$ .  $V_{\text{BATTERY}}$  connects to  $V_{\text{OUT}}$  (through a 15 $\Omega$  switch) when  $V_{\text{CC}}$  is below  $V_{\text{SW}}$  and  $V_{\text{BATTERY}}$  is greater than  $V_{\text{CC}}$ .

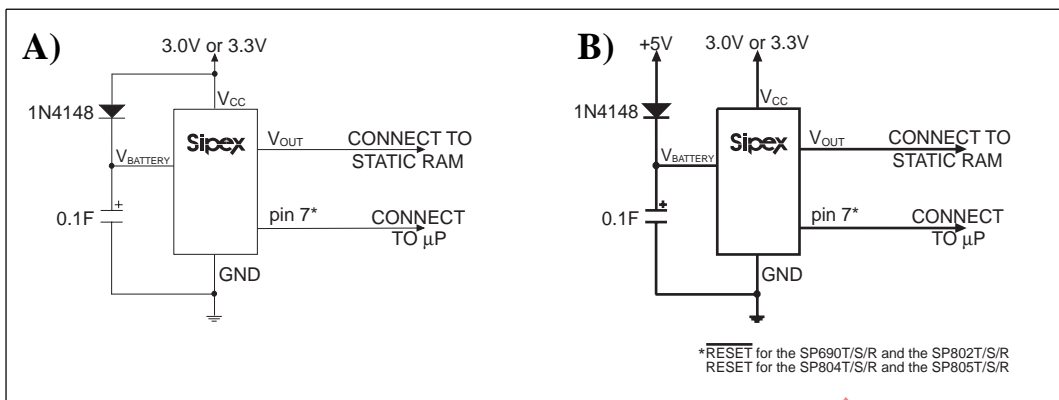


Figure 21. Using a High Capacity Capacitor as a Backup Power Source

Switchover at  $V_{SW}$  (2.40V) ensures that battery-backup mode is entered before  $V_{OUT}$  gets too close to the 2.0V minimum required to reliably retain data in CMOS RAM. Switchover at higher  $V_{CC}$  voltages would decrease backup-battery life. When  $V_{CC}$  recovers, switchover is deferred until  $V_{CC}$  rises above the reset threshold,  $V_{RST}$ , to ensure a stable supply.  $V_{OUT}$  is connected to  $V_{CC}$  through a 1.5Ω PMOS power switch.

### Using a High Capacity Capacitor as a Backup Power Source

Figure 21 shows two ways to use a High Value Capacitor as a backup power source. The High Value Capacitor may be connected through a diode to the 3V input as in Figure 21A or, if a 5V supply is also available, the High Value Capacitor may be charged up to the 5V supply as in Figure 21B allowing a longer backup period. Since  $V_{BATTERY}$  can exceed  $V_{CC}$  while  $V_{CC}$  is above the reset threshold, there are no special precautions when using these  $\mu P$  supervisors with a High Value Capacitor.

### Operation Without a Backup Power Source

These  $\mu P$  supervisors were designed for battery-backed applications. If a backup power source is not used, connect both  $V_{BATTERY}$  and  $V_{OUT}$  to  $V_{CC}$ . Since there is no need to switch over to any backup power source,  $V_{OUT}$  does not need to be switched. A direct connection to  $V_{CC}$  eliminates any voltage drops across the switch which may push  $V_{OUT}$  below  $V_{CC}$ .

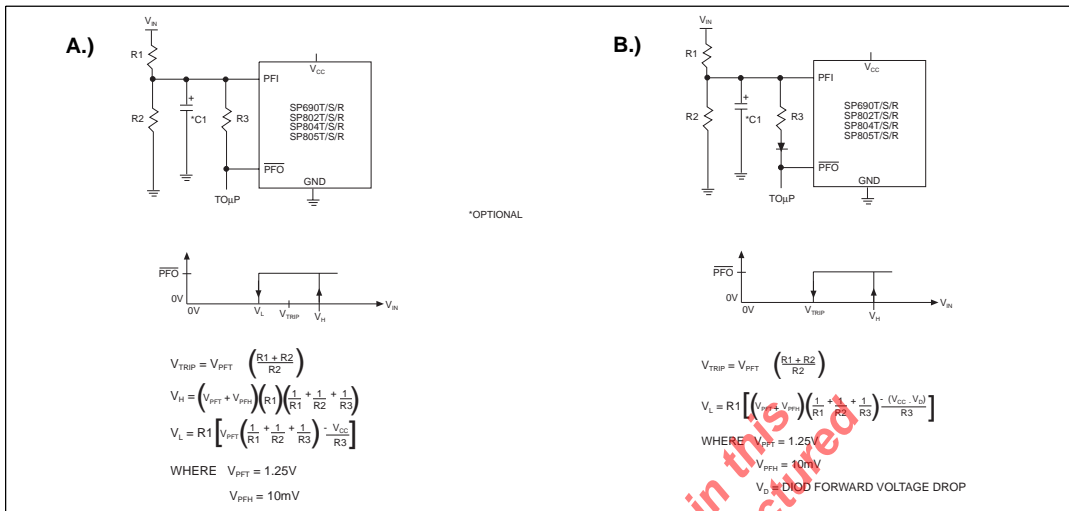
### Replacing the Backup Battery

If  $V_{BATTERY}$  is decoupled with a 0.1 $\mu F$  capacitor to ground, the backup battery can be removed while  $V_{CC}$  remains valid without danger of triggering RESET/RESET. As long as  $V_{CC}$  stays above  $V_{SW}$ , battery-backup mode cannot be entered.

### Adding Hysteresis to the Power-Fail Comparator

The power-fail comparator has a typical input hysteresis of 10mV. This is sufficient for most applications where a power-supply line is being monitored through an external voltage divider (refer to the Monitoring an Additional Power Supply section).

If additional noise margin is desired, connect a resistor between PFO and PFI as shown in Figure 22A. Select the ratio of R1 and R2 such that PFI sees 1.25V when  $V_{IN}$  falls to its trip point ( $V_{TRIP}$ ). R3 adds the hysteresis and will typically be more than 10 times the value of R1 or R2. The hysteresis window extends both above ( $V_H$ ) and below ( $V_L$ ) the original trip point ( $V_{TRIP}$ ).

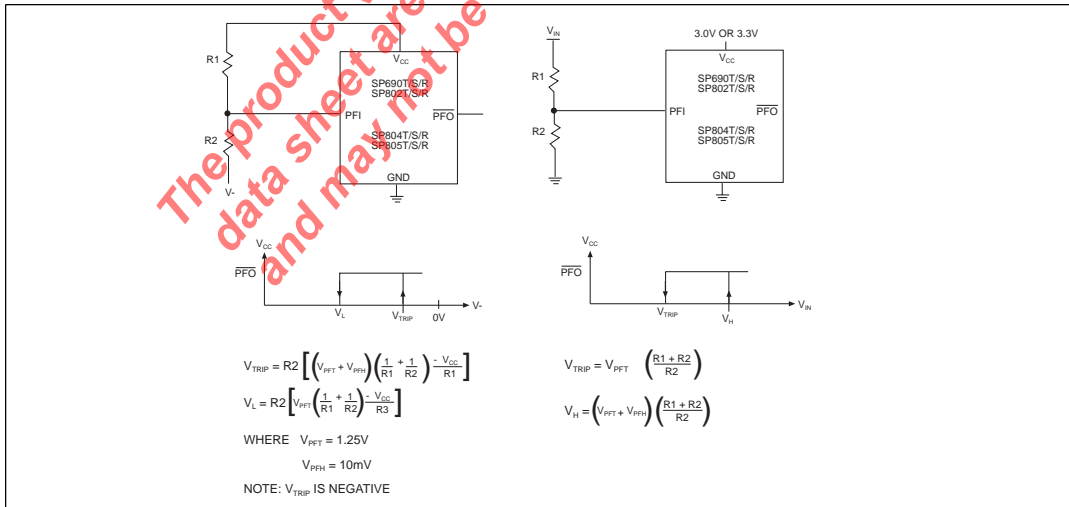


**Figure 22A. Adding Additional Hysteresis to the Power-Fail Comparator.**

**Figure 22B. Shifting the Additional Hysteresis above  $V_{PFT}$**

Connecting an ordinary signal diode in series with R3, as in **Figure 22B**, causes the lower trip point ( $V_L$ ) to coincide with the trip point without hysteresis ( $V_{TRIP}$ ), so the entire hysteresis window occurs above  $V_{TRIP}$ . This method provides additional noise margin without compromising the accuracy of the power-fail threshold when the monitored voltage is falling. It is useful for accurately detecting when a voltage falls past a threshold.

The current through R1 and R2 should be at least 1µA to ensure that the 25nA (max over extended temperature range) PFI input current does not shift the trip point. R3 should be larger than 10kΩ so it does not load down the PFO pin. Capacitor C1 adds additional noise rejection.



**Figure 23. Using the Power-Fail Comparator to Monitor an Additional Power Supply**

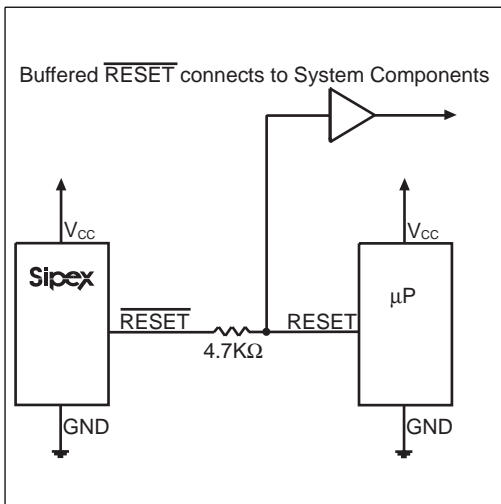


Figure 24. Interfacing to Microprocessors with Bidirectional  $\overline{\text{RESET}}$  I/O

### Monitoring an Additional Power Supply

These  $\mu\text{P}$  supervisors can monitor either positive or negative supplies using a resistor voltage divider to PFI.  $\overline{\text{PFO}}$  can be used to generate an interrupt to the  $\mu\text{P}$ , as seen in *Figure 23*.

### Interfacing to $\mu\text{Ps}$ with Bidirectional Reset Pins

Any  $\mu\text{Ps}$  with bidirectional reset pins, such as the Motorola 68HC11 series, can interface with the  $\overline{\text{SP690}}$  and the  $\overline{\text{SP802}}$   $\overline{\text{RESET}}$  outputs. For example, if the  $\overline{\text{RESET}}$  output is driven HIGH and the  $\mu\text{P}$  wants to pull it LOW, indeterminate logic levels may result. To correct this, connect a 4.7k $\Omega$  resistor between the  $\overline{\text{RESET}}$  output and the  $\mu\text{P}$  reset I/O, as in *Figure 24*. Buffer the  $\overline{\text{RESET}}$  output to other system components.

### Negative-Going $V_{\text{CC}}$ Transients

While issuing resets to the  $\mu\text{P}$  during power-up, power-down, and brownout conditions, these supervisors are relatively immune to short-duration negative-going  $V_{\text{CC}}$  transients (glitches). It is usually undesirable to reset the  $\mu\text{P}$  when  $V_{\text{CC}}$  experiences only small glitches.

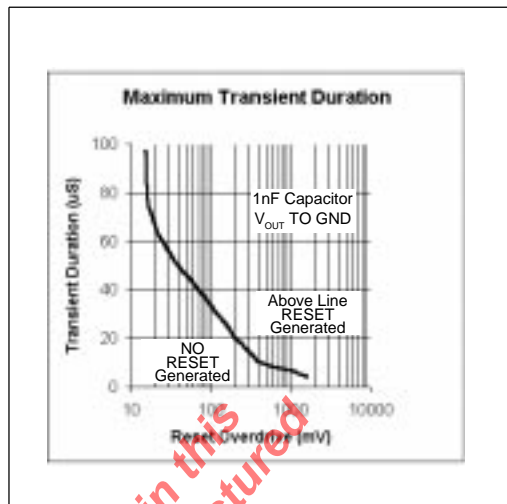
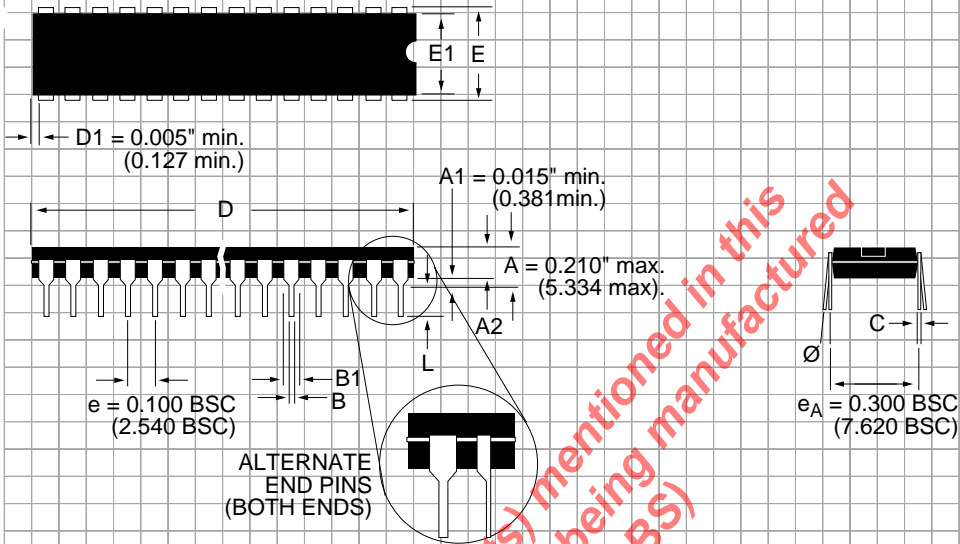


Figure 25. Maximum Transient Duration without Causing a Reset Pulse vs. Reset Comparator Overdrive

*Figure 25* shows maximum transient duration vs. reset-comparator overdrive, for which reset pulses are not generated. The data was generated using negative-going  $V_{\text{CC}}$  pulses, starting at 3.3V and ending below the reset threshold by the magnitude indicated (reset comparator overdrive). The graph shows the maximum pulse width a negative-going  $V_{\text{CC}}$  transient may typically have without causing a reset pulse to be issued. As the amplitude of the transient increases (i.e. goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a  $V_{\text{CC}}$  transient that goes 100mV below the reset threshold and lasts for 40 $\mu\text{s}$  or less will not cause a reset pulse to be issued. A 100nF bypass capacitor mounted close to the  $V_{\text{CC}}$  pin provides additional transient immunity.

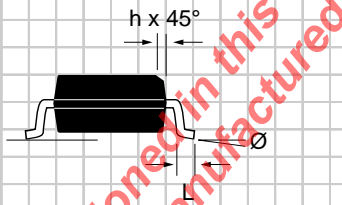
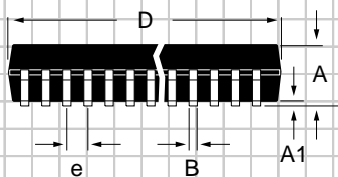
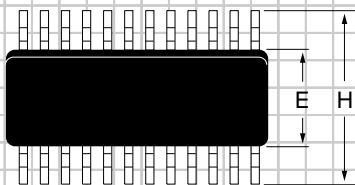


# PACKAGE: PLASTIC DUAL-IN-LINE (NARROW)



DIMENSIONS (Inches) Minimum/Maximum (mm)	8-PIN	14-PIN	16-PIN	18-PIN	20-PIN	22-PIN
A2	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)
B	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)
B1	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)
C	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)
D	0.355/0.400 (9.017/10.160)	0.735/0.775 (18.669/19.685)	0.780/0.800 (19.812/20.320)	0.880/0.920 (22.352/23.368)	0.980/1.060 (24.892/26.924)	1.145/1.155 (29.083/29.337)
E	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)
E1	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)
L	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)
Ø	0°/15° (0°/15°)	0°/15° (0°/15°)	0°/15° (0°/15°)	0°/15° (0°/15°)	0°/15° (0°/15°)	0°/15° (0°/15°)

**PACKAGE: PLASTIC  
SMALL OUTLINE (SOIC)  
(NARROW)**



DIMENSIONS (Inches) Minimum/Maximum (mm)	8-PIN	14-PIN	16-PIN
A	0.053/0.069 (1.346/1.748)	0.053/0.069 (1.346/1.748)	0.053/0.069 (1.346/1.748)
A1	0.004/0.010 (0.102/0.249)	0.004/0.010 (0.102/0.249)	0.004/0.010 (0.102/0.249)
B	0.014/0.019 (0.35/0.49)	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)
D	0.189/0.197 (4.80/5.00)	0.337/0.344 (8.552/8.748)	0.386/0.394 (9.802/10.000)
E	0.150/0.157 (3.802/3.988)	0.150/0.157 (3.802/3.988)	0.150/0.157 (3.802/3.988)
e	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)
H	0.228/0.244 (5.801/6.198)	0.228/0.244 (5.801/6.198)	0.228/0.244 (5.801/6.198)
h	0.010/0.020 (0.254/0.498)	0.010/0.020 (0.254/0.498)	0.010/0.020 (0.254/0.498)
L	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)
Ø	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)

The product (or product) mentioned in this data sheet are not being manufactured (B.S.)

## ORDERING INFORMATION

Model	Temperature Range	Package Types
SP690TCN.....	0°C to +70°C.....	8-Pin NSOIC
SP690TCP.....	0°C to +70°C.....	8-Pin PDIP
SP690TEN.....	-40°C to +85°C.....	8-Pin NSOIC
SP690TEP.....	-40°C to +85°C.....	8-Pin PDIP
SP690SCN.....	0°C to +70°C.....	8-Pin NSOIC
SP690SCP.....	0°C to +70°C.....	8-Pin PDIP
SP690SEN.....	-40°C to +85°C.....	8-Pin NSOIC
SP690SEP.....	-40°C to +85°C.....	8-Pin PDIP
SP690RCN.....	0°C to +70°C.....	8-Pin NSOIC
SP690RCP.....	0°C to +70°C.....	8-Pin PDIP
SP690REN.....	-40°C to +85°C.....	8-Pin NSOIC
SP690REP.....	-40°C to +85°C.....	8-Pin PDIP
SP802TCN.....	0°C to +70°C.....	8-Pin NSOIC
SP802TCP.....	0°C to +70°C.....	8-Pin PDIP
SP802TEN.....	-40°C to +85°C.....	8-Pin NSOIC
SP802TEP.....	-40°C to +85°C.....	8-Pin PDIP
SP802SCN.....	0°C to +70°C.....	8-Pin NSOIC
SP802SCP.....	0°C to +70°C.....	8-Pin PDIP
SP802SEN.....	-40°C to +85°C.....	8-Pin NSOIC
SP802SEP.....	-40°C to +85°C.....	8-Pin PDIP
SP802RCN.....	0°C to 0°C.....	8-Pin NSOIC
SP802RCP.....	0°C to +70°C.....	8-Pin PDIP
SP802REN.....	-40°C to +85°C.....	8-Pin NSOIC
SP802REP.....	-40°C to +85°C.....	8-Pin PDIP
SP804TCN.....	0°C to +70°C.....	8-Pin NSOIC
SP804TCP.....	0°C to +70°C.....	8-Pin PDIP
SP804TEN.....	-40°C to +85°C.....	8-Pin NSOIC
SP804TEP.....	-40°C to +85°C.....	8-Pin PDIP
SP804SCN.....	0°C to +70°C.....	8-Pin NSOIC
SP804SCP.....	0°C to +70°C.....	8-Pin PDIP
SP804SEN.....	-40°C to +85°C.....	8-Pin NSOIC
SP804SEP.....	-40°C to +85°C.....	8-Pin PDIP
SP804RCN.....	0°C to +70°C.....	8-Pin NSOIC
SP804RCP.....	0°C to +70°C.....	8-Pin PDIP
SP804REN.....	-40°C to +85°C.....	8-Pin NSOIC
SP804REP.....	-40°C to +85°C.....	8-Pin PDIP
SP805TCN.....	0°C to +70°C.....	8-Pin NSOIC
SP805TCP.....	0°C to +70°C.....	8-Pin PDIP
SP805TEN.....	-40°C to +8C.....	8-Pin NSOIC
SP805TEP.....	-40°C to +85°C.....	8-Pin PDIP
SP805SCN.....	0°C to +70°C.....	8-Pin NSOIC
SP805SCP.....	0°C to +70°C.....	8-Pin PDIP
SP805SEN.....	-40°C to +85°C.....	8-Pin NSOIC
SP805SEP.....	-40°C to +85°C.....	8-Pin PDIP
SP805RCN.....	0°C to +70°C.....	8-Pin NSOIC
SP805RCP.....	0°C to +70°C.....	8-Pin PDIP
SP805REN.....	-40°C to +85°C.....	8-Pin NSOIC
SP805REP.....	-40°C to +85°C.....	8-Pin PDIP

The product (or products) mentioned in this data sheet are no longer being manufactured (OBS)

Please consult the factory for pricing and availability on a Tape-On-Reel option.



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