

## Features

- Gate drive supply range from 6 V to 20 V
- CMOS Schmitt-triggered inputs
- 3.3V and 5V logic compatible
- Two independent gate drivers
- Matched propagation delay for both channels
- Outputs in phase with inputs
- Leadfree, RoHS compliant

## Typical Applications

- General Purpose Dual Low Side Driver
- DC-DC converters

## Product Summary

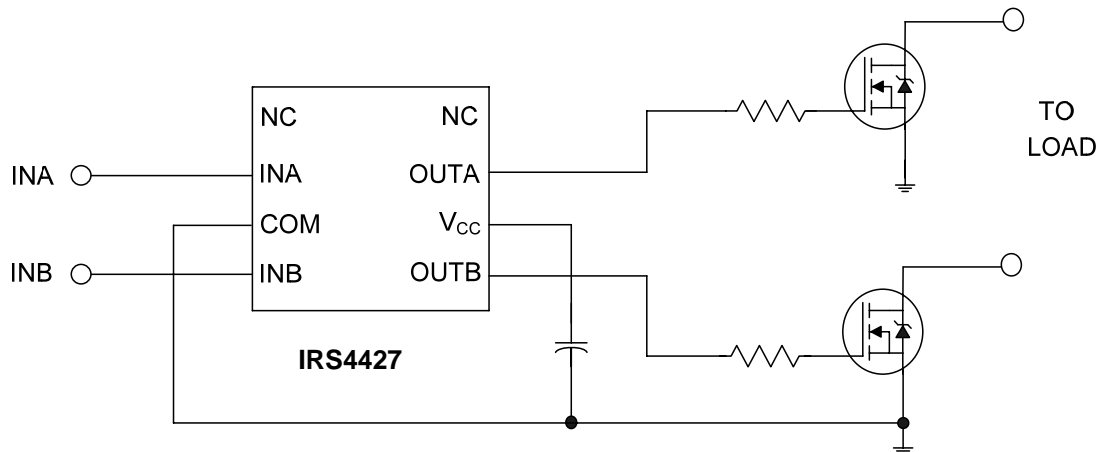
Topology	General Driver
$V_{OUT}$	6V - 20V
$I_{o+}$ & $I_{o-}$ (typical)	2.3A & 3.3A
$t_{on}$ & $t_{off}$ (typical)	50ns & 50ns

## Package Type



PDIP 8

## Typical Connection Diagram



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and Design Tips for proper circuit board layout.

<b>Table of Contents</b>	<b>Page</b>
Typical connection diagram	1
Description	3
Qualification Information	4
Absolute Maximum Ratings	5
Recommended Operating Conditions	5
Static Electrical Characteristics	6
Dynamic Electrical Characteristics	6
Functional Block Diagram	7
Input/Output Pin Equivalent Circuit Diagram	8
Lead Definitions	9
Lead Assignments	9
Application Information and Additional Details	10
Package Details	12
Part Marking Information	13
Ordering Information	14

**Description**

The IRS4427 is a low voltage, high speed power MOSFET and IGBT driver. Proprietary latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays between two channels are matched.

**Qualification Information<sup>†</sup>**

<b>Qualification Level</b>		Industrial <sup>††</sup>
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.
<b>Moisture Sensitivity Level</b>		Not Applicable (non surface mount package style)
<b>ESD</b>	Machine Model	Class B (per JEDEC standard JESD22-A115)
	Human Body Model	Class 3A (per EIA/JEDEC standard EIA/JESD22-A114)
<b>IC Latch-Up Test</b>		Class I, Level A (per JESD78)
<b>RoHS Compliant</b>		Yes

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

**Absolute Maximum Ratings**

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min	Max	Units
V <sub>CC</sub>	Fixed supply voltage	-0.3	20	V
V <sub>O</sub>	Output voltage	-0.3	V <sub>CC</sub> + 0.3	
V <sub>IN</sub>	Logic input voltage	-0.3	V <sub>CC</sub> + 0.3	
P <sub>D</sub>	Package power dissipation @ TA ≤ 25°C	—	1	W
R <sub>thJA</sub>	Thermal resistance, junction to ambient	—	125	°C/W
T <sub>J</sub>	Junction temperature	—	150	°C
T <sub>S</sub>	Storage temperature	-55	150	
T <sub>L</sub>	Lead temperature (soldering, 10 seconds)	—	300	

**Recommended Operating Conditions**

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. The offset rating is tested with supply of V<sub>CC</sub> = 15V.

Symbol	Definition	Min	Max	Units
V <sub>CC</sub>	Fixed supply voltage	6	20	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	
V <sub>IN</sub>	Logic input voltage	0	V <sub>CC</sub>	
T <sub>A</sub>	Ambient temperature	-40	125	°C

**Static Electrical Characteristics**

$V_{CC} = 15V$ ,  $T_A = 25^\circ C$  unless otherwise specified. The  $V_{IN}$  and  $I_{IN}$  parameters are referenced to COM and are applicable to input leads: INA and INB. The  $V_O$  and  $I_O$  parameters are referenced to COM and are applicable to the output leads: OUTA and OUTB.

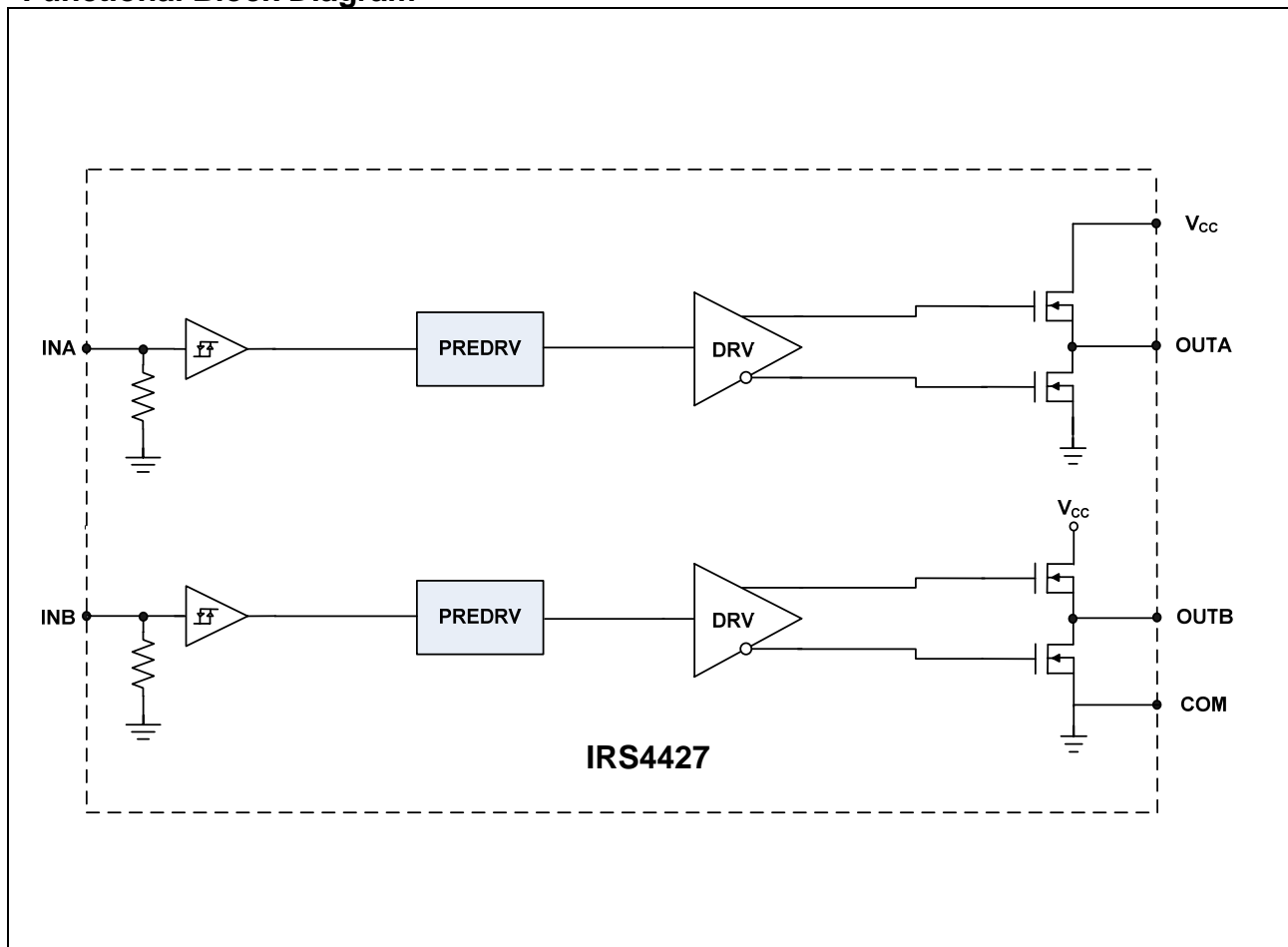
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
$V_{IH}$	Logic "1" input voltage	2.5	—	—	V	
$V_{IL}$	Logic "0" input voltage	—	—	0.8		
$V_{OH}$	High level output voltage, $V_{BIAS} - V_O$	—	—	1.4	V	$I_O = 0\text{ mA}$
$V_{OL}$	Low level output voltage, $V_O$	—	—	0.15		$I_O = 20\text{ mA}$
$I_{IN+}$	Logic "1" input bias current	—	5	15	$\mu A$	$V_{IN} = 5V$
$I_{IN-}$	Logic "0" input bias current	-30	-10	—		$V_{IN} = 0V$
$I_{QCC}$	Quiescent $V_{CC}$ supply current	—	100	200		$V_{IN} = 0V$ or $5V$
$I_{O+}$	Output high short circuit pulsed current	—	2.3	—	A	$V_O = 0V$ , $V_{IN} = 5V$
$I_{O-}$	Output low short circuit pulsed current	—	3.3	—		$V_O = 15V$ , $V_{IN} = COM$

**Dynamic Electrical Characteristics**

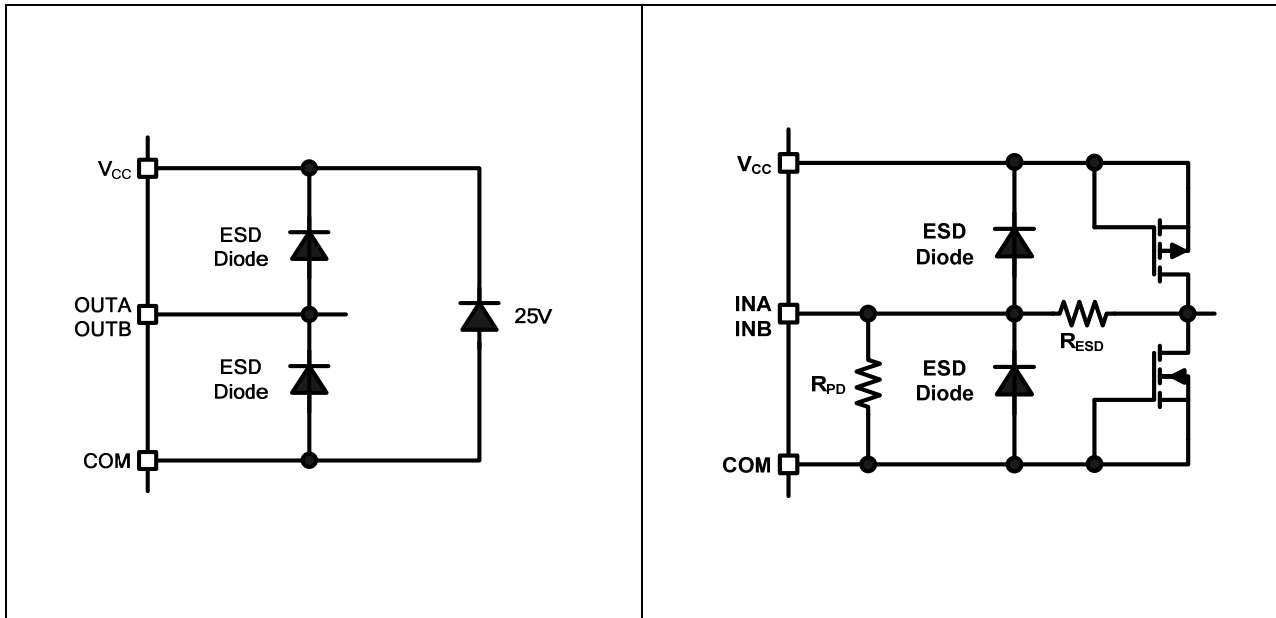
$V_{CC} = 15V$ ,  $T_A = 25^\circ C$ , and  $C_L = 1000pF$  unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
$t_{on}$	Turn-on propagation delay	—	50	95	ns	Figure 2
$t_{off}$	Turn-off propagation delay	—	50	95		
$t_r$	Turn-on rise time	—	25	55		
$t_f$	Turn-off fall time	—	25	55		

**Functional Block Diagram**



**Input/Output Pin Equivalent Circuit Diagrams**

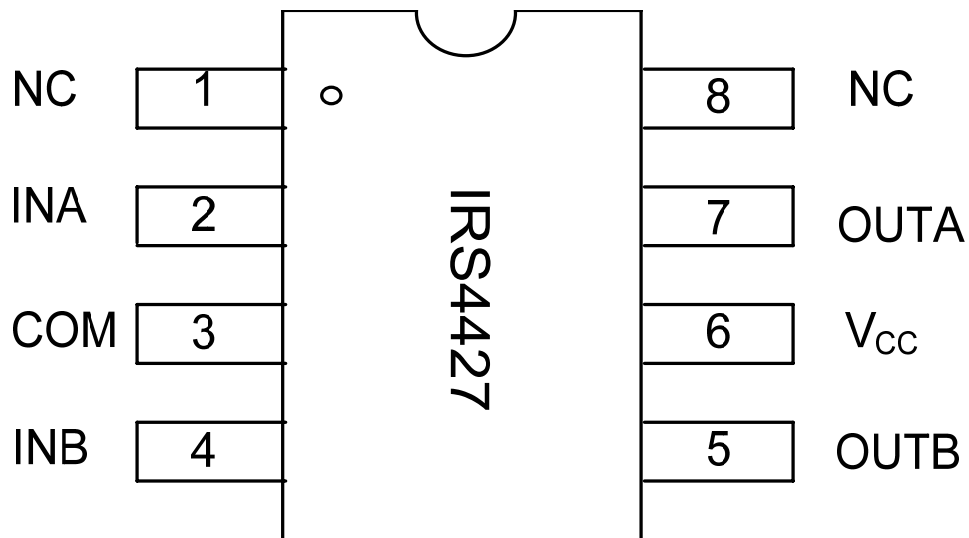




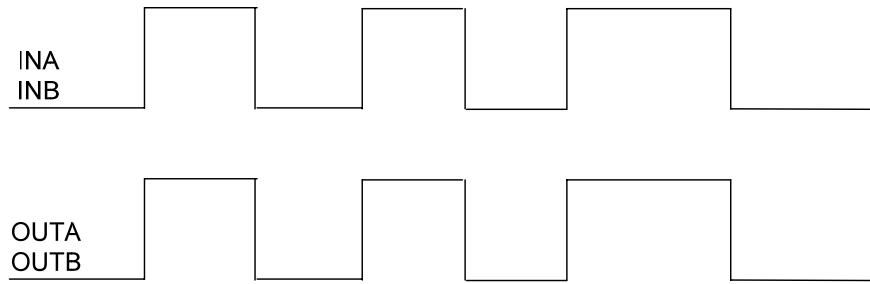
**Lead Definitions**

PIN	Symbol	Description
1	NC	No connection
2	INA	Logic input for gate driver output (OUTA), in phase
3	COM	Ground
4	INB	Logic input for gate driver output (OUTB), in phase
5	OUTB	Gate drive output B
6	V <sub>CC</sub>	Supply voltage
7	OUTA	Gate drive output A
8	NC	No connection

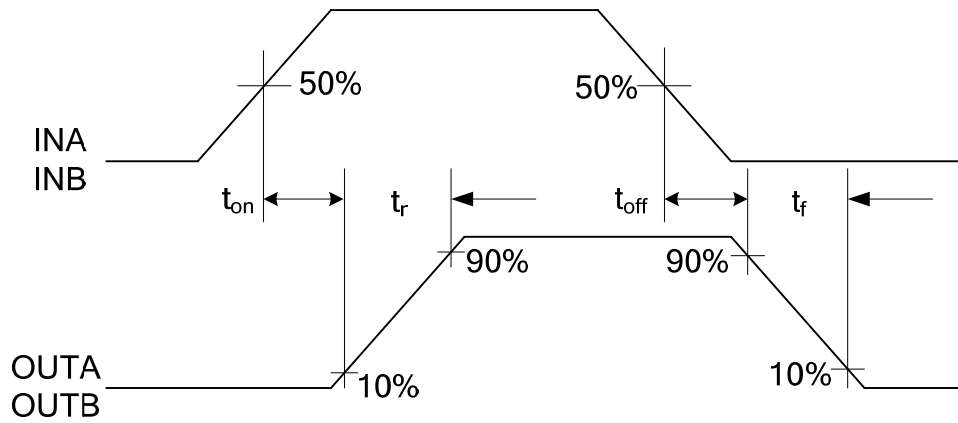
**Lead Assignments**



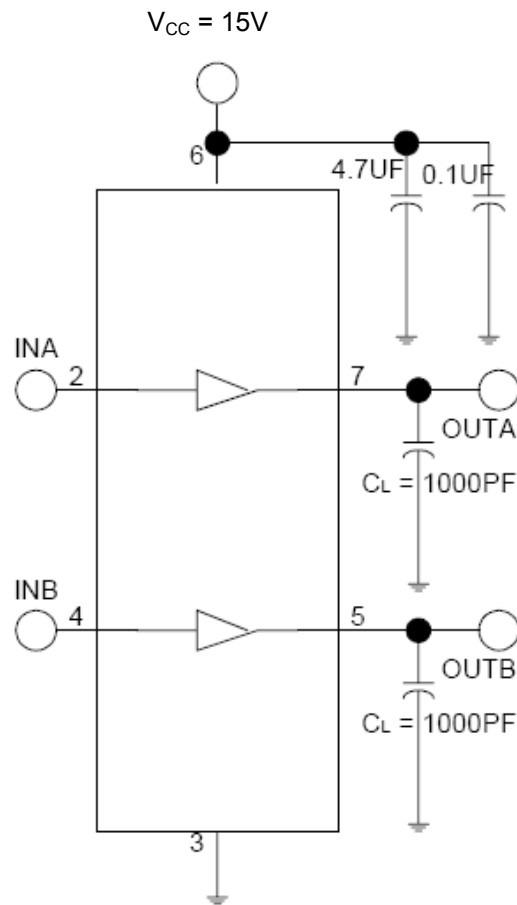
**Application Information and Additional Details**



**Figure 1: Input/output Timing Diagram**

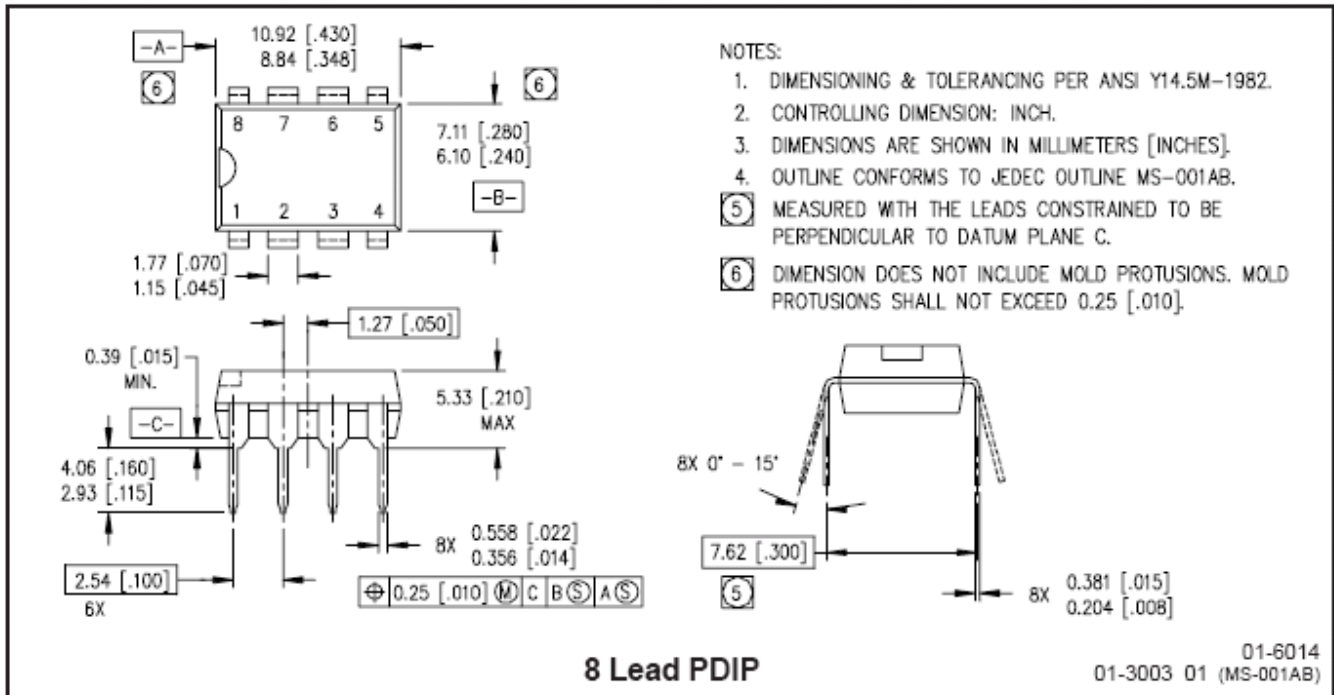


**Figure 2: Switching Time Waveform Definitions**



**Figure 3: Switching Time Test Circuit**

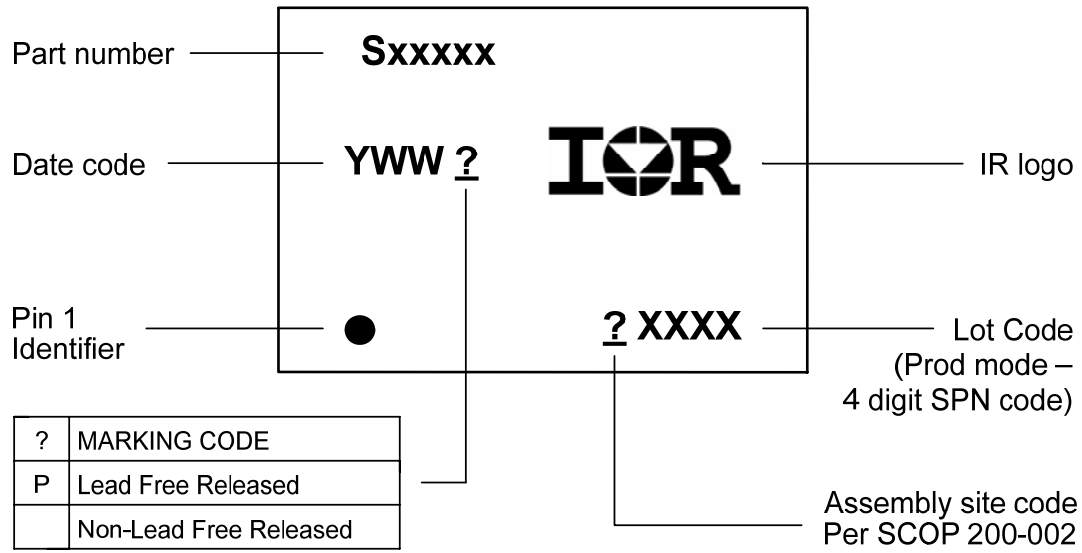
**Package Details, PDIP8**



**NOTES:**

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.
- ⑤ MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
- ⑥ DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

**Part Marking Information**



**Ordering Information**

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IRS4427	PDIP 8	Tube/Bulk	50	IRS4427PBF

The information provided in this document is believed to be accurate and reliable. However, International Rectifier assumes no responsibility for the consequences of the use of this information. International Rectifier assumes no responsibility for any infringement of patents or of other rights of third parties which may result from the use of this information. No license is granted by implication or otherwise under any patent or patent rights of International Rectifier. The specifications mentioned in this document are subject to change without notice. This document supersedes and replaces all information previously supplied.

For technical support, please contact IR's Technical Assistance Center  
<http://www.irf.com/technical-info/>

**WORLD HEADQUARTERS:**  
 233 Kansas St., El Segundo, California 90245  
 Tel: (310) 252-7105