

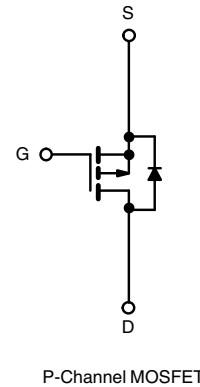
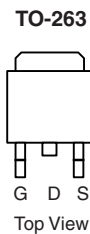
## IRF9610STRLPBF-VB Datasheet

### P-Channel 200V (D-S)MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	-200	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = -10$ V	0.50
$Q_g$ max. (nC)	44	
$Q_{gs}$ (nC)	7.1	
$Q_{gd}$ (nC)	27	
Configuration	Single	

#### FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- P-channel
- Fast switching
- Ease of paralleling
- Simple drive requirements

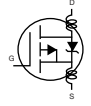



ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)					
PARAMETER	SYMBOL		LIMIT	UNIT	
Drain-Source Voltage	$V_{DS}$		-200	V	
Gate-Source Voltage	$V_{GS}$		$\pm 20$	V	
Continuous Drain Current	$V_{GS}$ at -10 V	$T_C = 25\text{ }^\circ\text{C}$	-11	A	
		$T_C = 100\text{ }^\circ\text{C}$	-6.8		
Pulsed Drain Current <sup>a</sup>	$I_{DM}$		-44		
Linear Derating Factor			1.0	W/ $^\circ\text{C}$	
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$		700	mJ	
Repetitive Avalanche Current <sup>a</sup>	$I_{AR}$		-11	A	
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$		13	mJ	
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$		$P_D$	125	W
Peak Diode Recovery dV/dt <sup>c</sup>	$dV/dt$		-5.0	V/ns	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$		-55 to +150	$^\circ\text{C}$	
Soldering Recommendations (Peak temperature) <sup>d</sup>	for 10 s		300		
Mounting Torque	6-32 or M3 screw		10	lbf · in	
			1.1	N · m	

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = -50$  V, starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 8.7$  mH,  $R_g = 25\text{ }^\circ\Omega$ ,  $I_{AS} = -11$  A (see fig. 12).
- $I_{SD} \leq -11$  A,  $dI/dt \leq 150$  A/ $\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 1.6 mm from case.

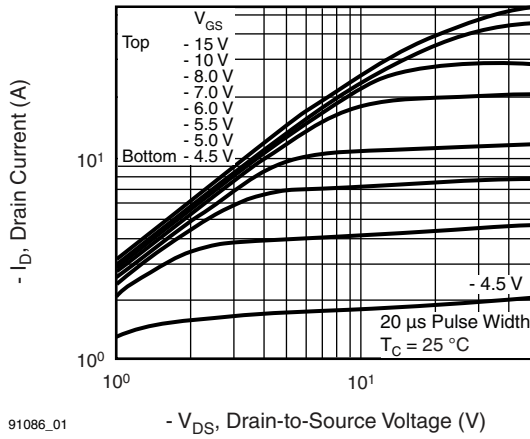
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.50	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	1.0	

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$		-200	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = -1\text{ mA}$		-	-0.2	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$		-2.0	-	-4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -200\text{ V}, V_{GS} = 0\text{ V}$		-	-	-100	$\mu\text{A}$
		$V_{DS} = -160\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	-500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}$	$I_D = -6.6\text{ A}^b$	-	0.50	-	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = -50\text{ V}, I_D = -6.6\text{ A}^b$		4.1	-	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = -25\text{ V}, f = 1.0\text{ MHz}$ , see fig. 5		-	1200	-	pF
Output Capacitance	$C_{oss}$			-	370	-	
Reverse Transfer Capacitance	$C_{rss}$			-	81	-	
Total Gate Charge	$Q_g$	$V_{GS} = -10\text{ V}$	$I_D = -11\text{ A}, V_{DS} = -160\text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	44	nC
Gate-Source Charge	$Q_{gs}$			-	-	7.1	
Gate-Drain Charge	$Q_{gd}$			-	-	27	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -100\text{ V}, I_D = -11\text{ A}$ $R_g = 9.1\text{ }\Omega, R_D = 8.6\text{ }\Omega$ , see fig. 10 <sup>b</sup>		-	14	-	ns
Rise Time	$t_r$			-	43	-	
Turn-Off Delay Time	$t_{d(off)}$			-	39	-	
Fall Time	$t_f$			-	38	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal Source Inductance	$L_S$			-	7.5	-	
Gate Input Resistance	$R_g$	$f = 1\text{ MHz}$ , open drain		0.3	-	1.7	$\Omega$
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p-n junction diode 		-	-	-11	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	-44	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = -11\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	-5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = -11\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$		-	250	300	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	2.9	3.6	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

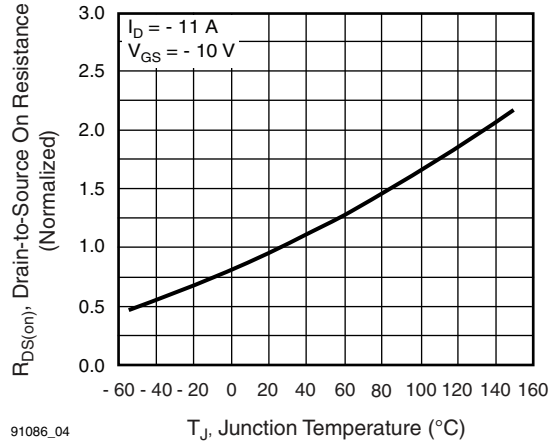
**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

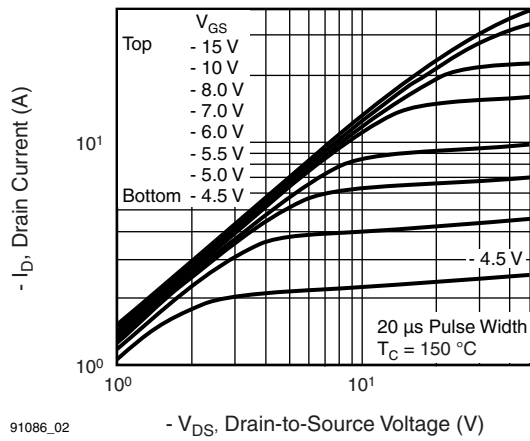
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



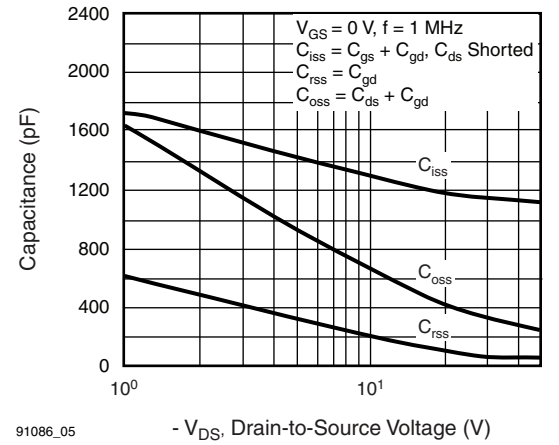
**Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ °C}$**



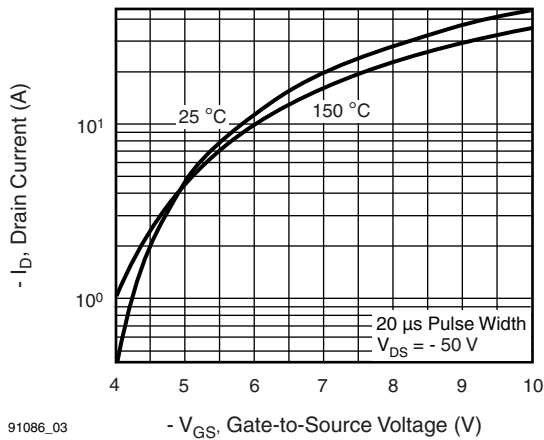
**Fig. 4 - Normalized On-Resistance vs. Temperature**



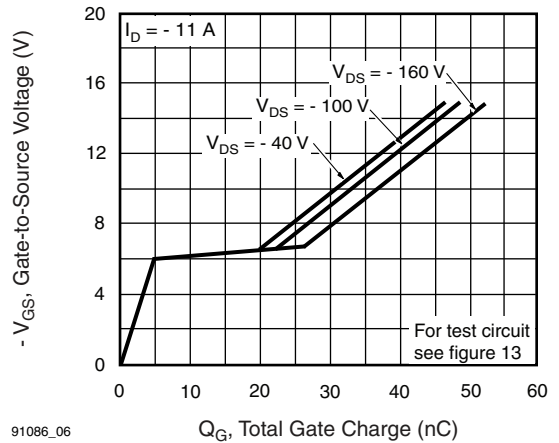
**Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ °C}$**



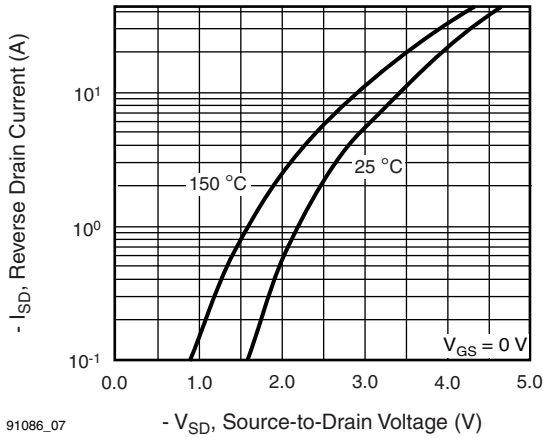
**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



**Fig. 3 - Typical Transfer Characteristics**

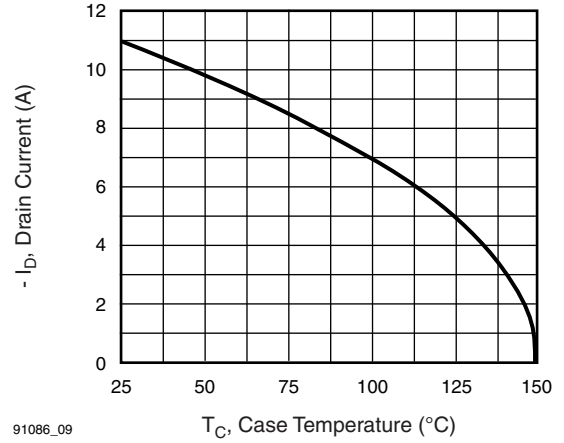


**Fig. 6 - Typical Gate Charge vs. Drain-to-Source Voltage**



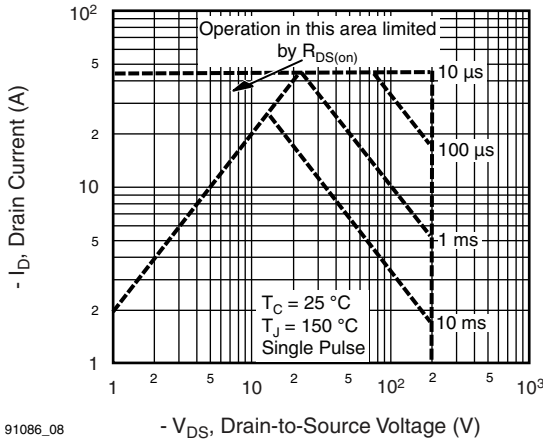
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Fig. 7 - Typical Source-Drain Diode Forward Voltage



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Fig. 9 - Maximum Drain Current vs. Case Temperature



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Fig. 8 - Maximum Safe Operating Area

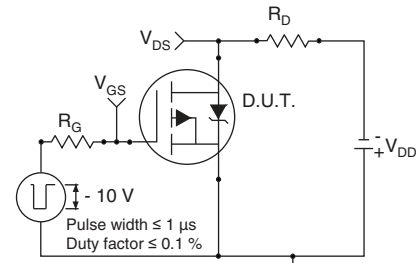


Fig. 10a - Switching Time Test Circuit

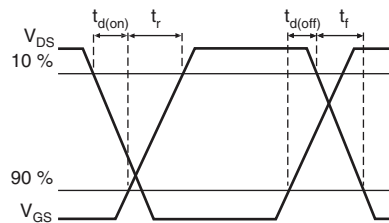
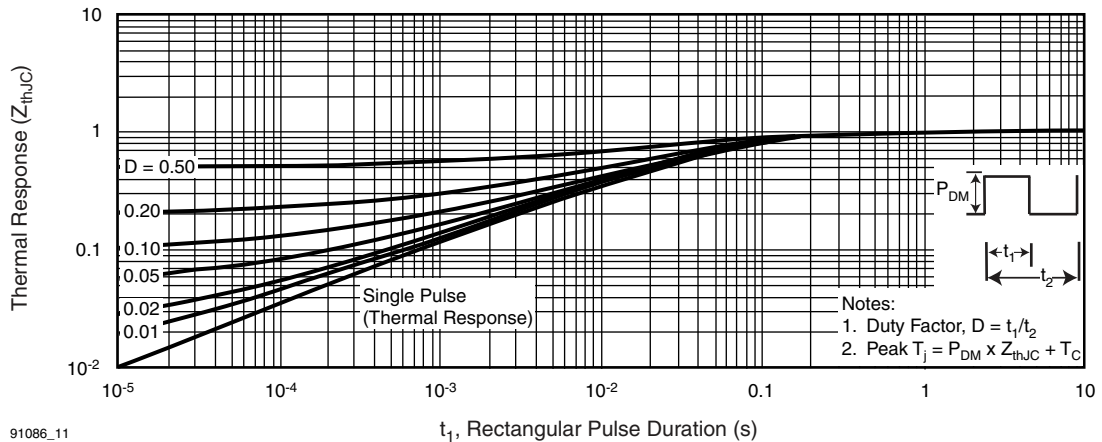


Fig. 10b - Switching Time Waveforms



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Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

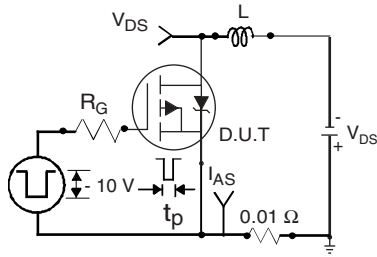


Fig. 12a - Unclamped Inductive Test Circuit

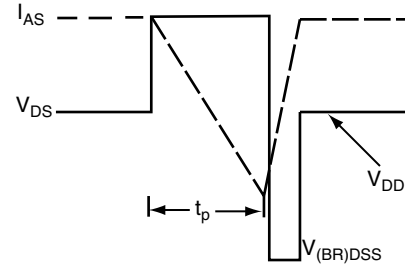


Fig. 12b - Unclamped Inductive Waveforms

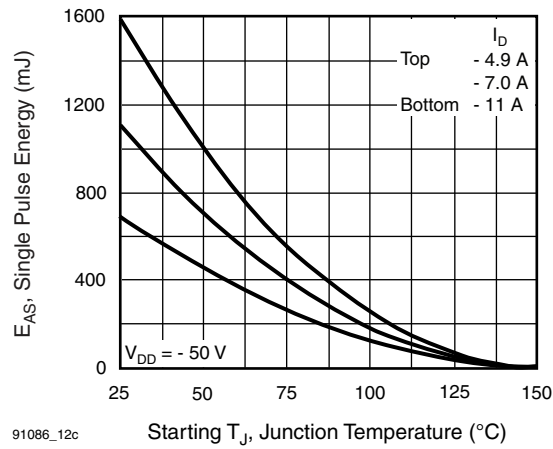


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

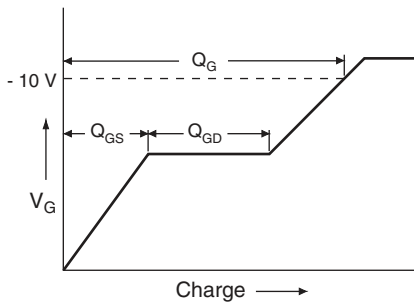


Fig. 13a - Basic Gate Charge Waveform

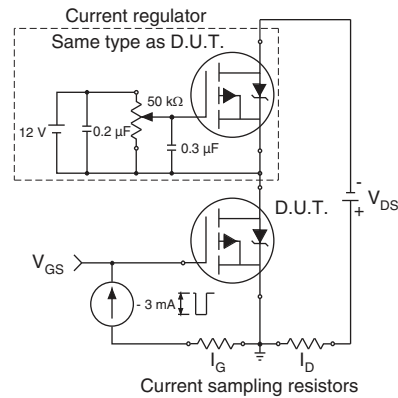
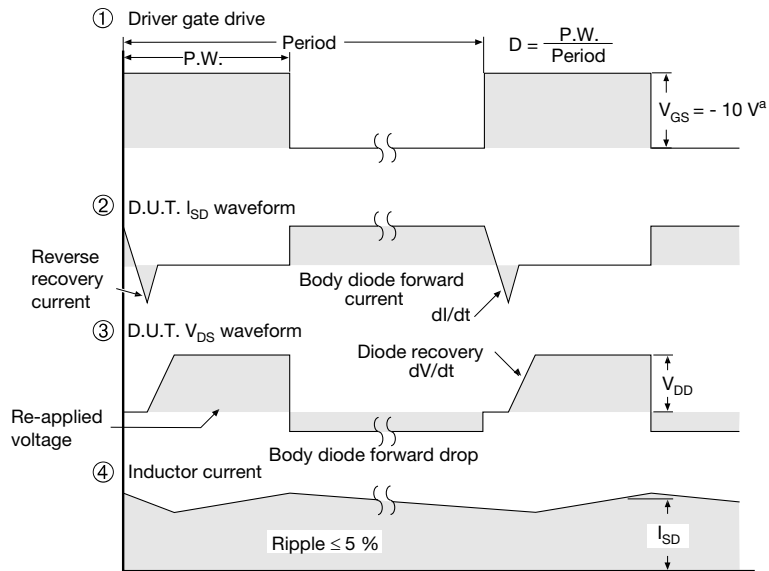
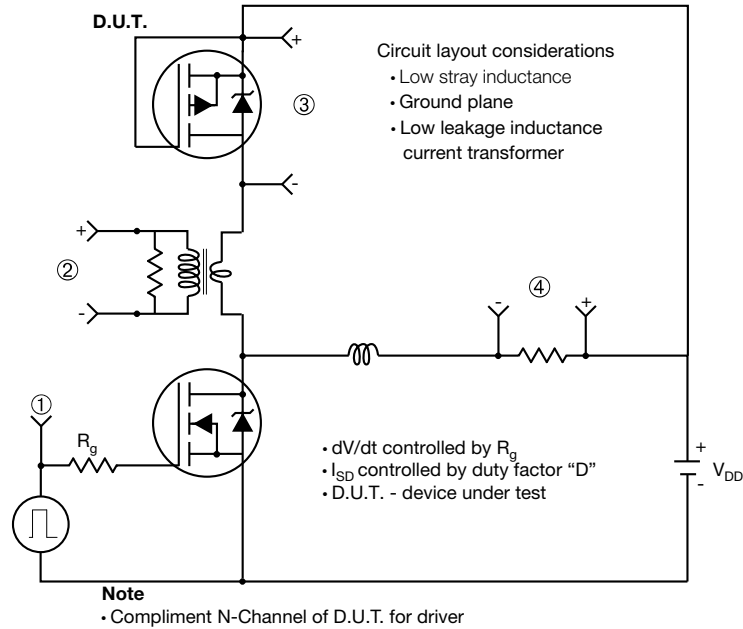


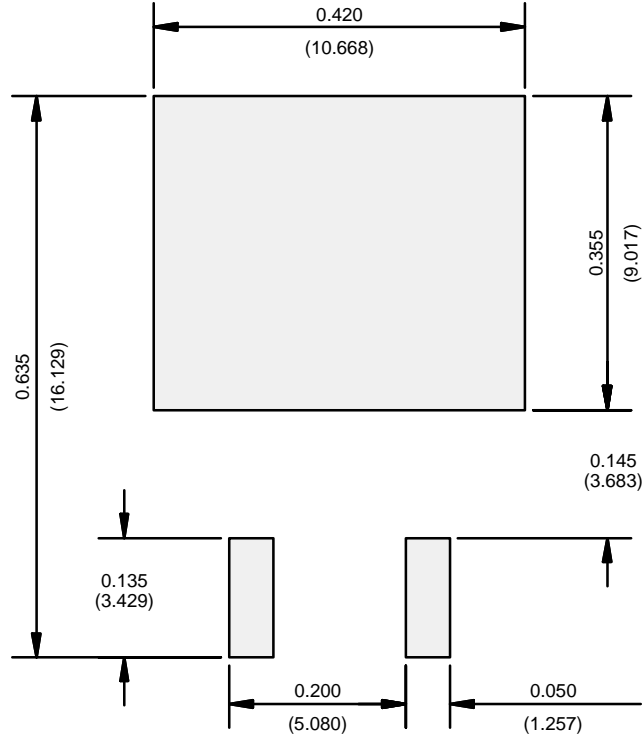
Fig. 13b - Gate Charge Test Circuit

**Peak Diode Recovery dV/dt Test Circuit**



**Fig. 14 - For P-Channel**

**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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