MC14024B

7-Stage Ripple Counter

The MC14024B is a 7−stage ripple counter with short propagation delays and high maximum clock rates. The Reset input has standard noise immunity, however the Clock input has increased noise immunity due to Hysteresis. The output of each counter stage is buffered.

- Diode Protection on All Inputs
- Output Transitions Occur on the Falling Edge of the Clock Pulse
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range
- Pin−for−Pin Replacement for CD4024B

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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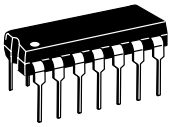
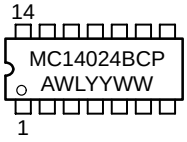
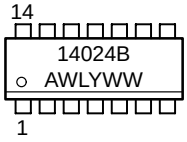
MARKING DIAGRAMS

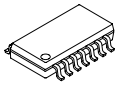


PDIP−14
P SUFFIX
CASE 646

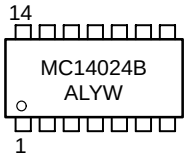


SOIC−14
D SUFFIX
CASE 751A





SOEIAJ−14
F SUFFIX
CASE 965



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

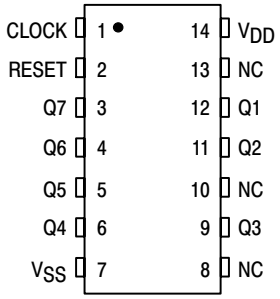
Device	Package	Shipping
MC14024BCP	PDIP−14	2000/Box
MC14024BD	SOIC−14	2750/Box
MC14024BDR2	SOIC−14	2500/Tape & Reel
MC14024BF	SOEIAJ−14	See Note 1.
MC14024BFEL	SOEIAJ−14	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

TRUTH TABLE

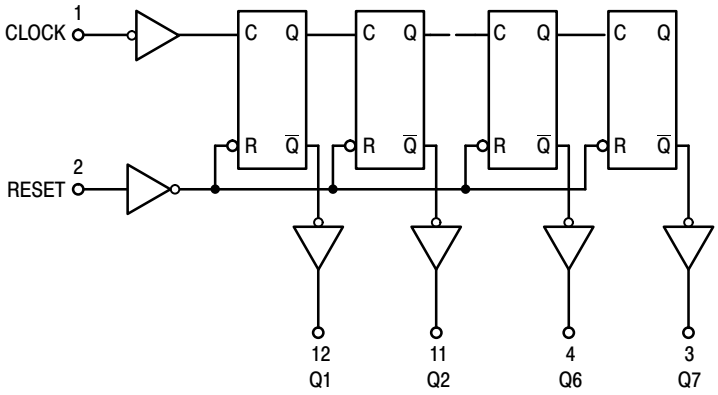
Clock	Reset	State
0	0	No Change
0	1	All Outputs Low
1	0	No Change
1	1	All Outputs Low
↗	0	No Change
↗	1	All Outputs Low
↘	0	Advance One Count
↘	1	All Outputs Low

PIN ASSIGNMENT



V_{DD} = PIN 14
V_{SS} = PIN 7
NC = NO CONNECTION

LOGIC DIAGRAM



Q3 = PIN 9
Q4 = PIN 6
Q5 = PIN 5

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (4.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage “0” Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD} “1” Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage “0” Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	—	1.5	—	2.25	1.5	—	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
(V_O = 0.5 or 4.5 Vdc) “1” Level	V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.5 Vdc)		15	11	—	11	8.25	—	11	—	
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	– 3.0	—	– 2.4	– 4.2	—	– 1.7	—	
(V_{OH} = 4.6 Vdc)		5.0	– 0.64	—	– 0.51	– 0.88	—	− 0.36	—	
(V_{OH} = 9.5 Vdc)		10	– 1.6	—	− 1.3	– 2.25	—	– 0.9	—	
(V_{OH} = 13.5 Vdc)		15	– 4.2	—	− 3.4	− 8.8	—	− 2.4	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15	I_T = (0.31 µA/kHz) f + I_{DD} I_T = (0.60 µA/kHz) f + I_{DD} I_T = (1.89 µA/kHz) f + I_{DD}							µAdc

4. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

SWITCHING CHARACTERISTICS [7.] (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ [8.]	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	—	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	—	40	80	
Propagation Delay Time	t_{PLH},					ns
Clock to Q1	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 295 ns		5.0	—	380	600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 117 ns		10	—	150	230	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 85 ns		15	—	110	175	
Clock to Q7						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 915 ns		5.0	—	1000	2000	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 367 ns		10	—	400	750	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 275 ns		15	—	300	565	
Reset to Q_n						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	—	500	800	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 217 ns		10	—	250	400	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 155 ns		15	—	180	300	
Clock Pulse Width	t_{WH}	5.0	500	200	—	ns
		10	165	60	—	
		15	125	40	—	
Reset Pulse Width	t_{WH}	5.0	600	375	—	ns
		10	350	200	—	
		15	260	150	—	
Reset Removal Time	t_{rem}	5.0	625	250	—	ns
		10	190	75	—	
		15	145	50	—	
Clock Input Rise and Fall Time	t_{TLH}, t_{THL}	5.0	—	—	1.0	s
		10	—	—	8.0	ms
		15	—	—	200	μs
Input Pulse Frequency	f_{cl}	5.0	—	2.5	1.0	MHz
		10	—	8.0	3.0	
		15	—	12	4.0	

7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

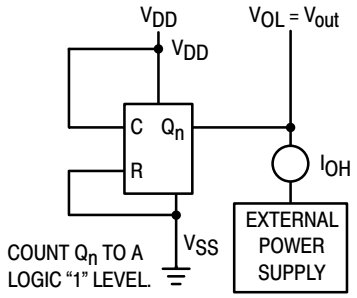


Figure 1. Typical Output Source Characteristics Test Circuit

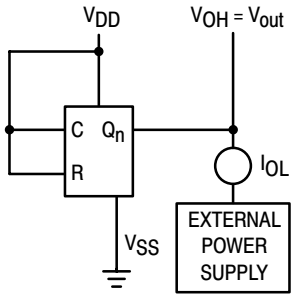


Figure 2. Typical Output Sink Characteristics Test Circuit

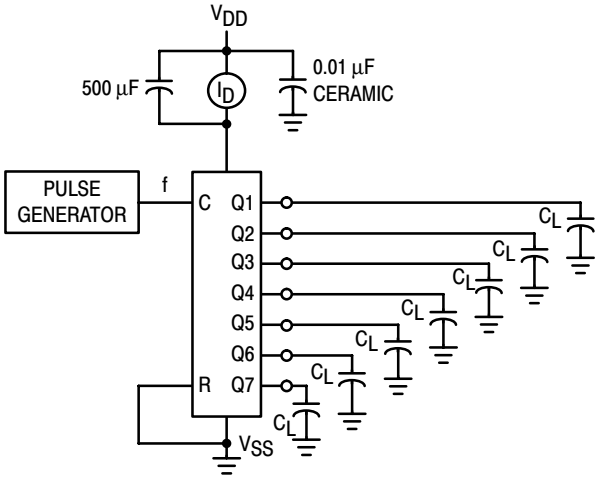


Figure 3. Power Dissipation Test Circuit

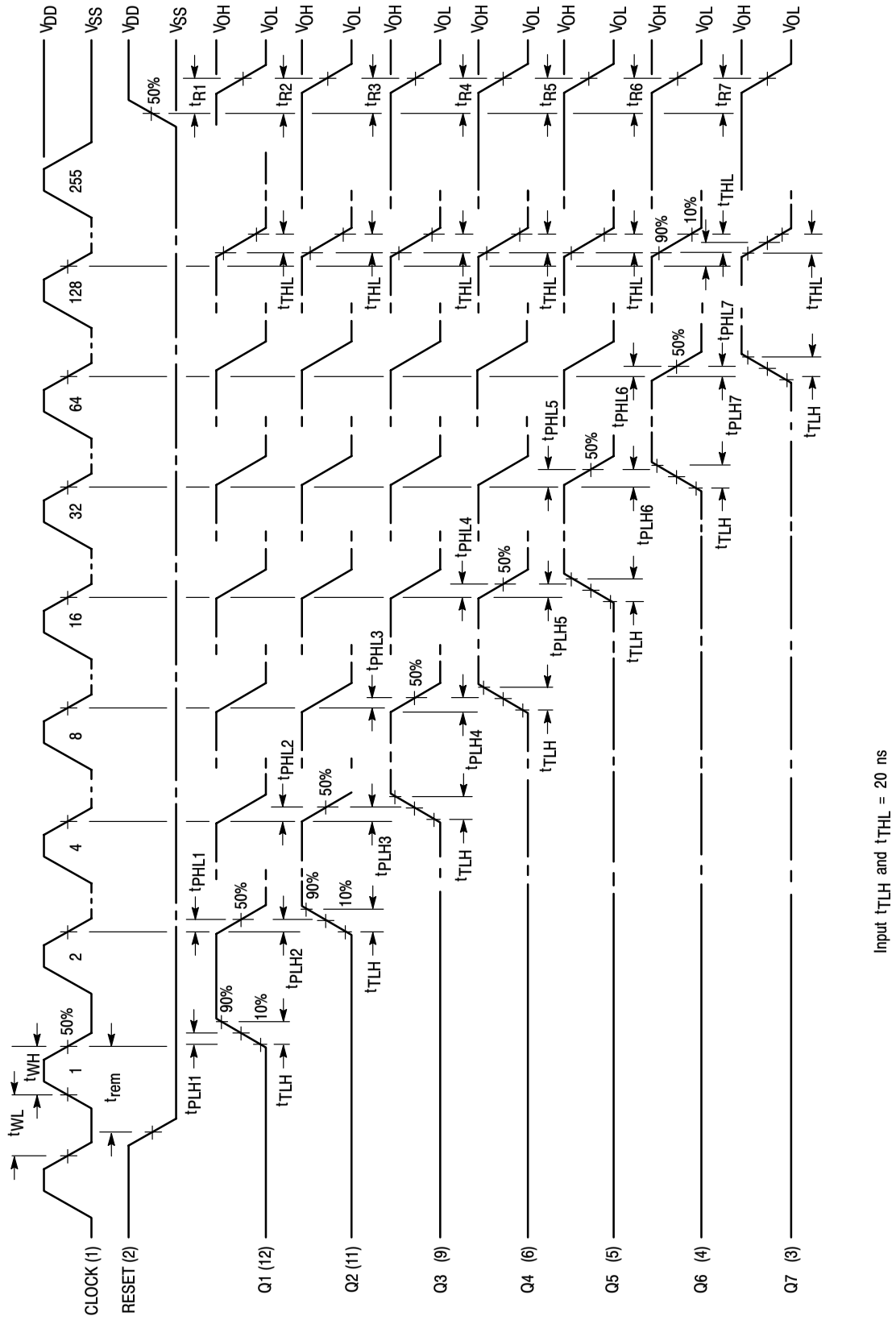


Figure 4. Functional Waveforms