60-V, 5-A, Non-Synchronous Step-Down DC/DC Converter

Features

- High Efficiency at Light Loads with Pulse Skipping
- 80-mΩ High-Side MOSFET
- 160-μA Operating Quiescent Current and 1-μA Shutdown Current
- 100-kHz to 2.5-MHz Adjustable Switching Frequency
- Integrated PLL to Synchronize with External Clock
- Adjustable UVLO Voltage and Hysteresis
- Under-voltage and Over-voltage Power Good Output
- Adjustable Soft-Start and Sequencing
- 0.8-V 1.5% Internal Voltage Reference
- DFN4X4-10 with Exposed Pad Package
- –40°C to 125°C Operation Ambient Temperature Range

Applications

- 12-V, 24-V, 48-V Industrial Power Application
- Telecom & Communication Equipment Power Applications

Description

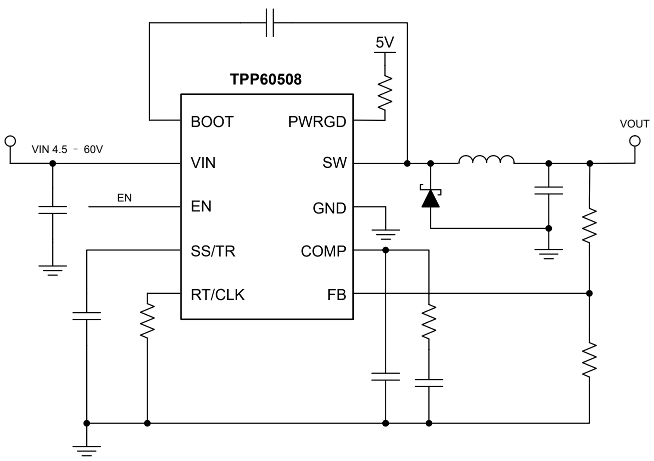
The TPP60508 is a 60-V, 5-A output, non-synchronous, step-down, and switch-mode converter with integrated high-side power MOSFET.

The TPP60508 employs current-mode control supporting simple external compensation and flexible component selection. It also supports low quiescent current mode with pulse-skipping and ultra-low sleep current.

With the integrated phase-locked loop, the TPP60508 can synchronize with an external clock source with wide frequency selection, optimized for efficiency, physical dimensions, and electromagnetic interference (EMI).

Protection and diagnostic features protect the device as well as the system power supply. By using open-drain power-good output, the user system is able to distinguish if the output supply is within the target voltage range. The soft-start feature, which controls the output ramping, can be set independently with external resistors to soft-start or sequencing/tracking mode. Current limit, frequency foldback, and over-temperature protection improve system-level robustness.

Typical Application Circuit



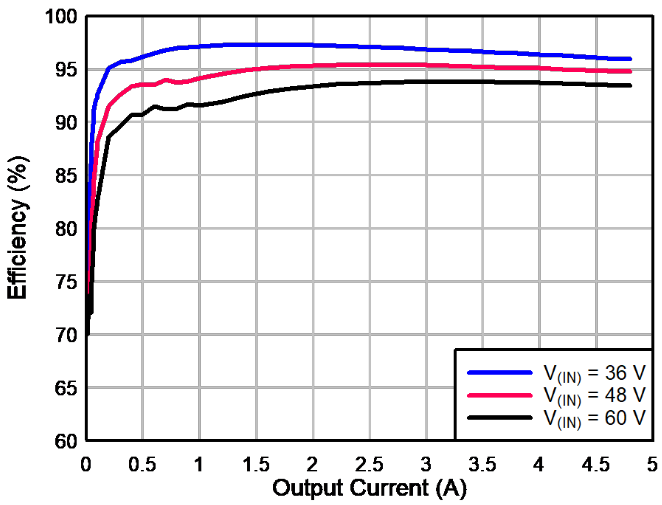


Table of Contents

Product Family Table

Order Number	Package
TPP60508L1-DF9R-S	DFN4X4-10
TPP60508L1-DF9R	DFN4X4-10

Revision History

Date	Revision	Notes
2022-02-10	Rev.A.0	Initial release version
2022-09-02	Rev.A.1	Miscellaneous correction
2023-05-31	Rev.A.2	Added minimal on-time description
2023-07-31	Rev.A.3	Minor correction on OTP description and SW abs max voltage
2023-08-16	Rev.A.4	Converted to new format

Pin Configuration and Functions

TPP60508
DFN4X4-10
Top View

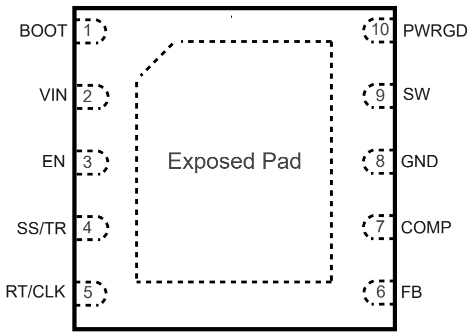


Table 1. Pin Functions: TPP60508

Pin No	Pin Name	I/O	Description
1	BOOT	I	Bootstrap capacitor between BOOT and SW, recommend to use a 0.1-μF ceramic capacitor with 10-V or higher voltage rating.
2	VIN	O	Supply voltage with 4.5-V to 60-V operating range
3	EN	O	Device enable pin with internal pull-up current source. Threshold can be increased via external resistors.
4	SS/TR	I	Soft-start and tracking input. When using soft-start mode, an external capacitor connected to this pin sets output ramping time; When using track/sequence mode, the voltage on this pin overrides internal voltage reference thus sets the output voltage.
5	RT/CLK	–	Frequency selection and external clock input. When using it as frequency setting mode, an external connected resistor sets switching frequency; When using it as clock synchronization input, the input is a high impedance clock input for internal PLL.
6	FB	I	Feedback input, connected to internal inverting input of gm error amplifier
7	COMP	I/O	Error amplifier output and input to the PWM comparator, Connect frequency compensation network to this pin
8	GND	G	Device ground pin
9	SW	O	Switching output
10	PWRGD	O	Open-drain power good output
11	Exposed Pad	G	Device exposed pad, must be connected to GND with heat sink area for thermal dissipation.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
VIN	Supply Voltage	−0.3	65	V
SW	Switching Node Voltage	−0.6	VIN + 0.3	V
	Switching Node Voltage, SW 5-ns Transient	−7	VIN + 0.3	V
	Switching Node Voltage, SW 10-ns Transient	−2	VIN + 0.3	V
BOOT – SW	Bootstrap Voltage	−0.3	6.5	V
FB	Feedback Voltage	−0.3	3	V
COMP	Compensation Voltage	−0.3	3	V
EN	Enable Input Voltage	−0.3	8.4	V
SS/TR	Soft start / Tracking Input Voltage	−0.3	3	V
RT/CLK	Switching frequency setting / PLL Input	−0.3	3	V
T_J	Operating Junction Temperature Range	−40	150	°C
T_A	Ambient Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering, 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Max	Unit
VIN	Supply Voltage	−0.3	65	V
SW	Switching Node Voltage	−0.3	VIN + 0.3	V
	Switching Node Voltage, SW 5-ns Transient	−7	VIN + 0.3	V
	Switching Node Voltage, SW 10-ns Transient	−2	VIN + 0.3	V
BOOT – SW	Bootstrap Voltage	−0.3	6.5	V
FB	Feedback Voltage	−0.3	3	V

Parameter		Min	Max	Unit
COMP	Compensation Voltage	−0.3	3	V
EN	Enable Input Voltage	−0.3	8.4	V
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T_L	Lead Temperature (Soldering, 10 sec)		260	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
DFN4X4-10	40	20	°C/W

(1) This data was taken with the JEDEC low effective thermal conductivity test board.
(2) This data was taken with the JEDEC standard multilayer test boards.

Electrical Characteristics

All test conditions: V_{IN} = 4.5 V to 60 V, T_J = −40°C to 150°C, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Power Supply						
V_{IN}	Operating Voltage Range		4.5		60	V
$V_{(UVLO)}$	Internal Under-voltage Lockout Threshold	Rising threshold	4.1	4.3	4.48	V
$V_{(UVLO,hys)}$				325		mV
I_Q	Quiescent Supply Current	EN = 5 V, T_A = 25 °C, $V_{(FB)}$ = 0.9 V		152	200	μA
I_{QSD}	Shut-down Supply Current	EN = 0 V, T_A = 25 °C		10.8	18	μA
VFB Voltage						
V_{FB}	V_{FB}Threshold Voltage		0.788	0.8	0.812	V
MOSFFET						
HS_{RDSON}	HS Switching On-Resistance	V_{IN} = 12 V, BOOT − SW = 5 V		80	185	mΩ
Current Limit						
I_{Limit}	Current Limit	Full voltage and temperature range, Open-Loop	6.3	7.9	10	A
		Full temperature range, V_{IN} = 12 V, Open-Loop	6.6	7.9	8.9	A
		T_A = 25 °C, V_{IN} = 12 V, Open-Loop	6.7	7.9	8.7	A
Error Amplifier						
$I_{(FB)}$	Input Current			50		nA
g_m	Error Amplifier Transconductance	−2 μA < I_{COMP} < 2 μA, V_{COMP} = 1 V		350		μMhos
g_m	Error Amplifier Transconductance during Soft-Start	−2 μA < I_{COMP} < 2 μA, V_{COMP} = 1 V , V_{FB}= 0.4 V		77		μMhos
A_{DC}	Error Amplifier Gain	$V_{(FB)}$ = 0.8 V		10000		V/V
$f_{(GBW),min}$	Minimal Unity Gain Bandwidth			2500		kHz
$I_{(COMP)}$	Error Amplifier Output Current Capability	$V_{(COMP)}$ = 1 V, 100-mV overdrive		±31		μA
$g_{COMP-SW}$	COMP to SW Current Transconductance			17		A/V
Thermal Shutdown						
T_{SD}	Thermal Shutdown Temperature			165		°C
T_{HYS}	Thermal Hysteresis			15		°C
Power Good (PWRGD)						

Parameter		Conditions	Min	Typ	Max	Unit
$V_{th(UV-falling)}$	Output undervoltage falling threshold			90		%
$V_{th(UV-rising)}$	Output undervoltage rising threshold			93		%
$V_{th(OV-falling)}$	Output overvoltage falling threshold			108		%
$V_{th(OV-rising)}$	Output overvoltage rising threshold			106		%
$V_{th(hys)}$	Output hysteresis	FB falling		2.5		%
$I_{lkg(PWRGD)}$	PWRGD leakage current	$V_{(PWRGD)}$ = 5.5 V, T_A = 25 °C		10		nA
$R_{dson(PWRGD)}$	PWRGD on-resistance	$I_{(PWRGD)}$ = 3 mA, V_{FB} < 0.79 V		6.5		Ω
$V_{(minVIN,PWRGD)}$	Minimal VIN for defined output	$V_{(PWRGD)}$ < 1.5 V, $I_{(PWRGD)}$ = 1.5 mA		2	2.5	V
Soft Start and Tracking (SS/TR)						
$I_{(SS/TR)}$	Soft-start charging current	$V_{(SS/TR)}$ = 0.4V		1.7		μA
$\Delta V_{(SS/TR)}$	SS/TR to FB matching error	$V_{(SS/TR)}$ = 0.4V		42		mV
$I_{(SS/TR),disch}$	Max SS/TR discharge current	$V_{(FB)}$ = 0 V, $V_{(SS/TR)}$ = 0.4V		1		mA
$V_{(SS/TR),disch}$	SS/TR discharge voltage	$V_{(FB)}$ = 0 V		54		mV
$V_{(SS/TR), th}$	SS/TR to reference cross-over threshold			1.2		V
LOGIC						
V_{EN}	EN Threshold Voltage		1.1	1.2	1.3	V
I_{EN}	EN Threshold + 50 mV			−4.6		μA
	EN Threshold -50 mV		−0.58	−1.2	−1.8	μA
$I_{EN,hys}$	EN Threshold hysteresis		−2.2	−3.4	−4.5	μA
$V_{th(RT/CLK),rising}$	RT/CLK Rising Threshold			1.55	2	V
$V_{th(RT/CLK),falling}$	RT/CLK Falling Threshold		0.5	1.2		V
Timing Characteristics						
t_{OCP}	Over-Current Protection Delay			60		ns
$t_{d,EN}$	Enable to COMP Delay			540		μs
$t_{CLK,min}$	Minimal CLK Input Pulse Width			15		ns
$t_{d,CLK}$	RT/CLK Falling Edge to SW Rising Edge Delay	f_{SW} = 500 kHz		55		ns
f_{SW}	Switching requency	R_T = 200 kΩ	450	500	550	kHz
	Switching Frequency using RT Mode		100		2500	kHz

Parameter		Conditions	Min	Typ	Max	Unit
	Switching Frequency using CLK Mode		160		2300	kHz
t_{PLL}	PLL Lock in Time	f_{SW} = 500 kHz		78		μs
t_{min_on}	Minimal on-time	VIN = 60 V		175		ns

Typical Performance Characteristics

All test conditions: V_{IN} = 48 V, T_A = +25°C, unless otherwise noted.

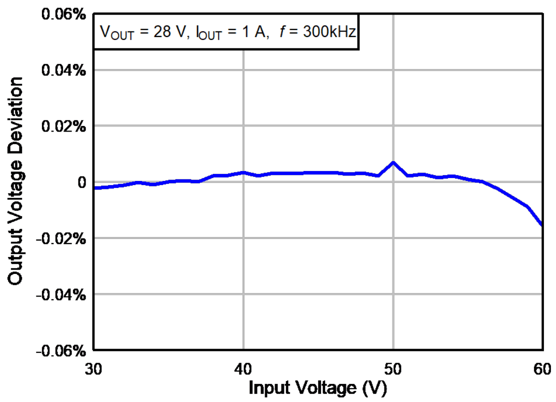


Figure 1. Line Regulation

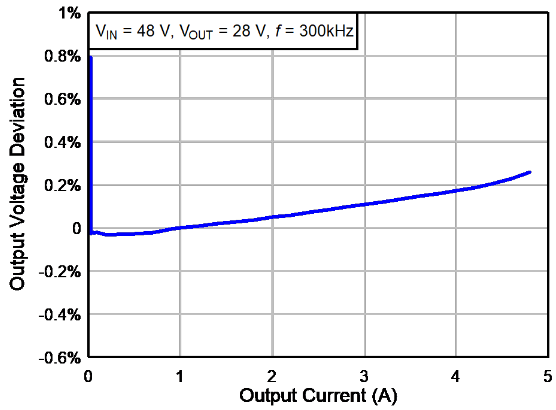
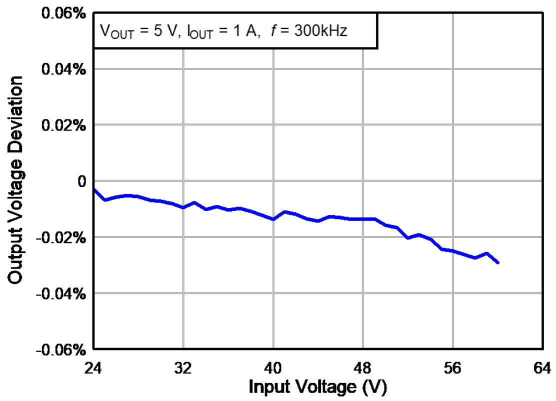
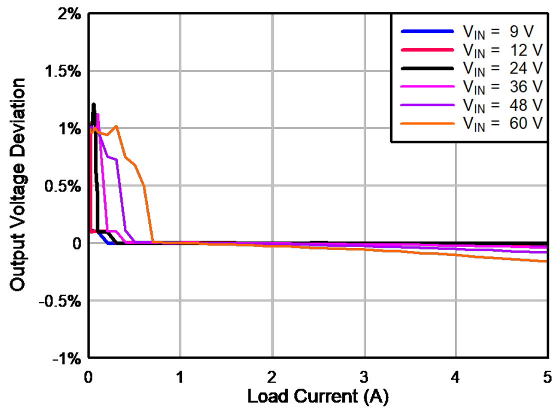


Figure 2. Load Regulation



f = 420 kHz T_A = 25 °C

Figure 3. Line Regulation



f = 420 kHz T_A = 25 °C

Figure 4. Load Regulation

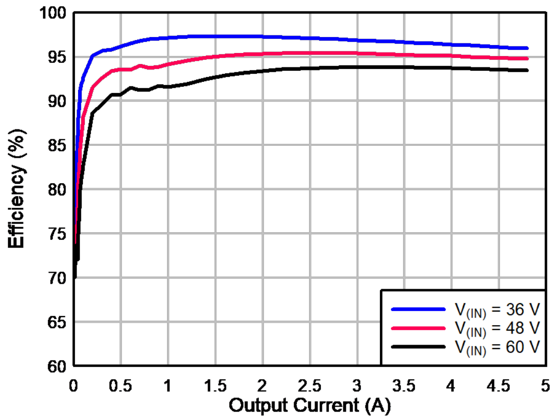


Figure 5. Efficiency

f = 300 kHz T_A = 25 °C

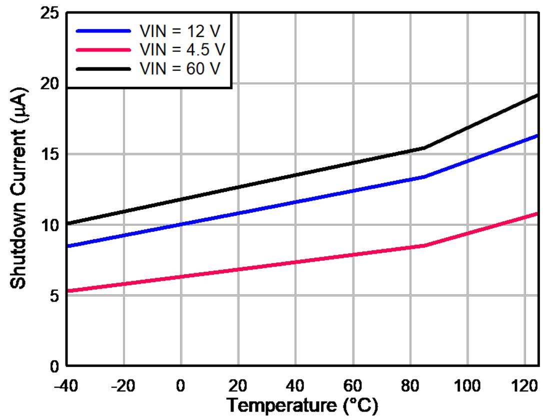


Figure 6. Device Shutdown Current vs Junction Temperature

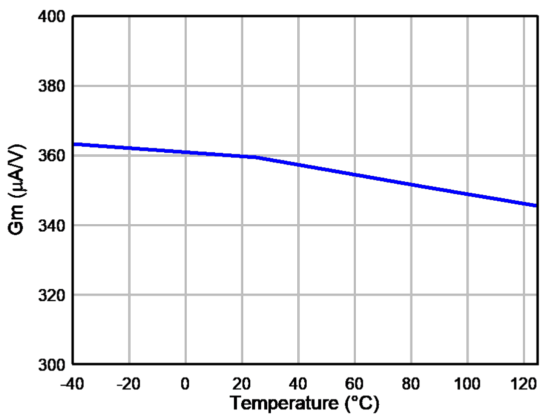


Figure 7. Error Amplifier Transconductance vs Junction Temperature

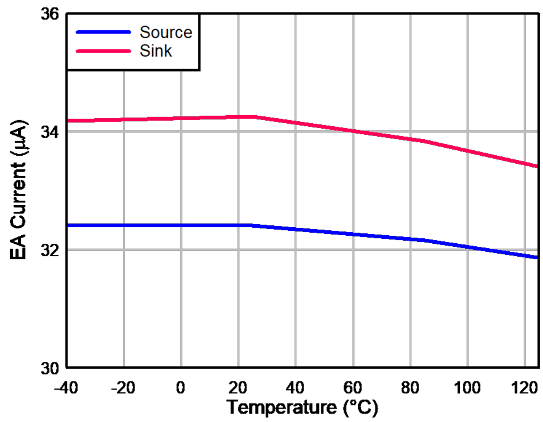


Figure 8. Device Shutdown Current vs Junction Temperature

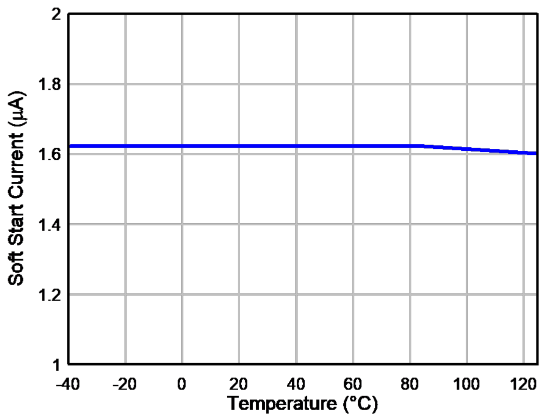


Figure 9. Soft Start Charge Current vs Junction Temperature

V_{IN} = 48 V T_A = 25 °C

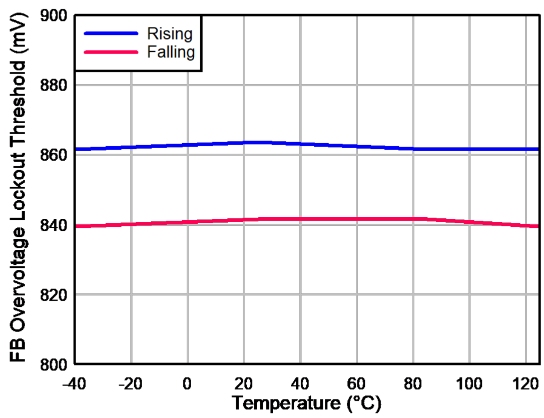


Figure 10. FB Overvoltage Lockout Threshold vs Temperature

I_{OUT} = 0 A

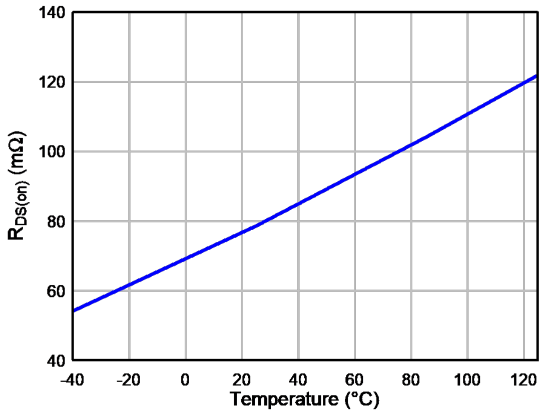


Figure 11. Power Transistor On-Resitance vs Temperature

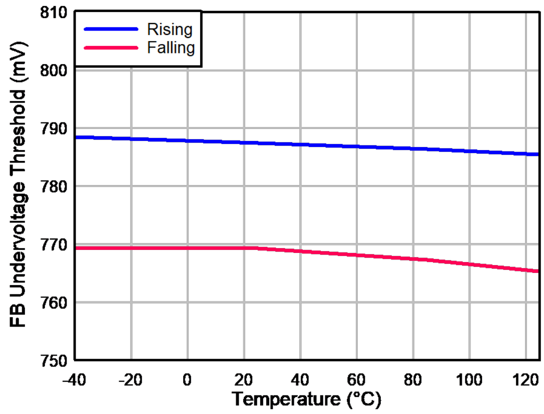


Figure 12. FB Undervoltage Lockout Threshold vs Temperature

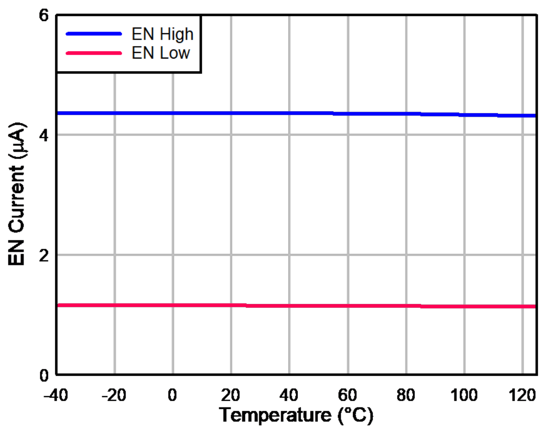


Figure 13. EN Current vs Junction Temperature

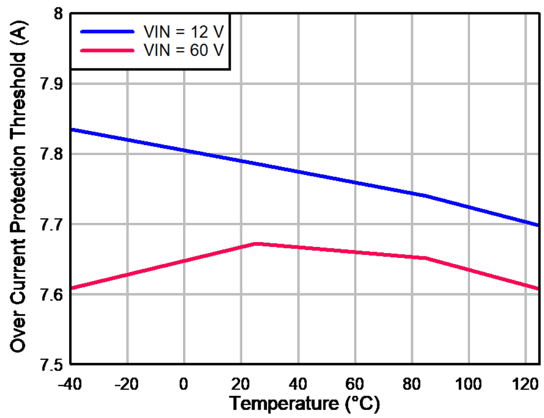


Figure 14. Over Current Protection Threshold vs Junction Temperature

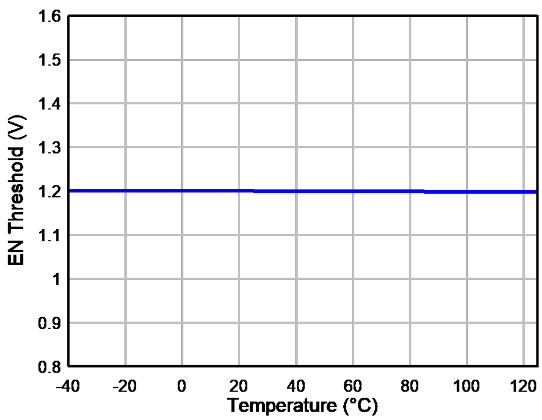


Figure 15. EN Threshold vs Junction Temperature

V_{IN} = 12 V

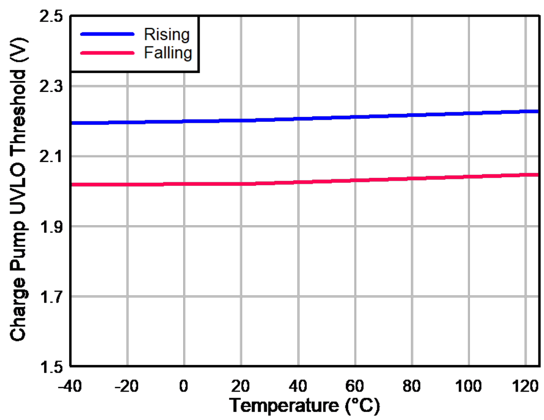


Figure 16. BOOT-SW UVLO vs Junction Temperature

V_{IN} = 12 V

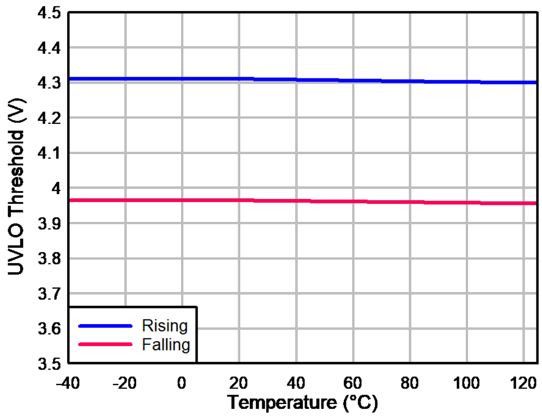


Figure 17. UVLO Threshold vs Junction Temperature

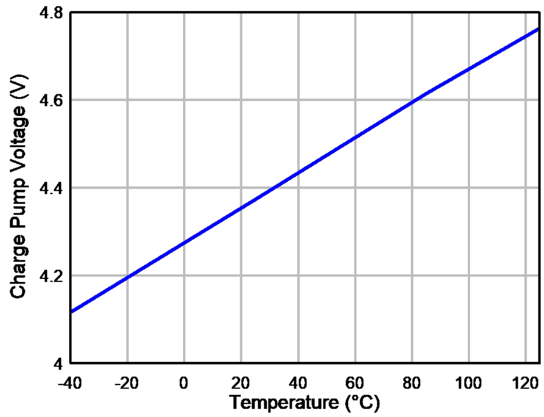


Figure 18. BOOT-SW Voltage vs Temperature

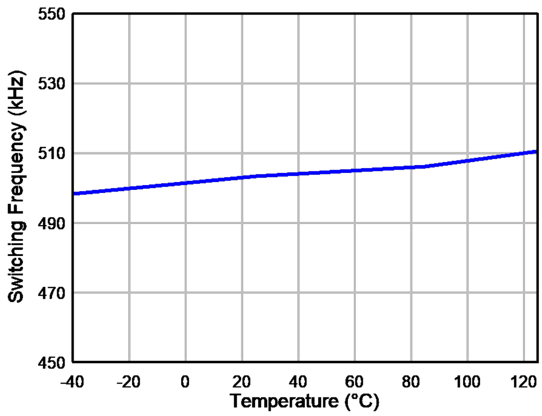


Figure 19. Switching Frequency vs Junction Temperature

R_{RT} = 200 kΩ

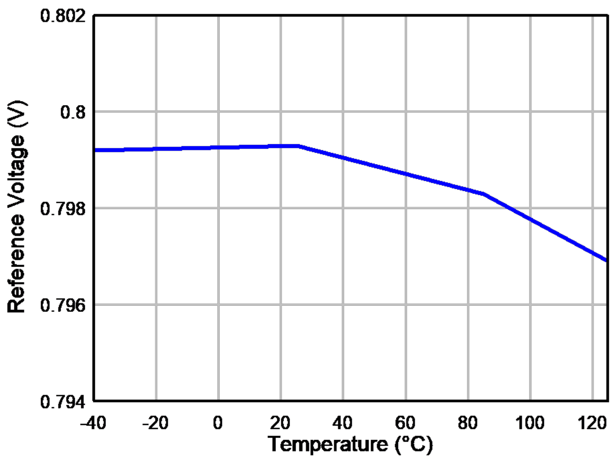


Figure 20. Reference Voltage vs Junction Temperature

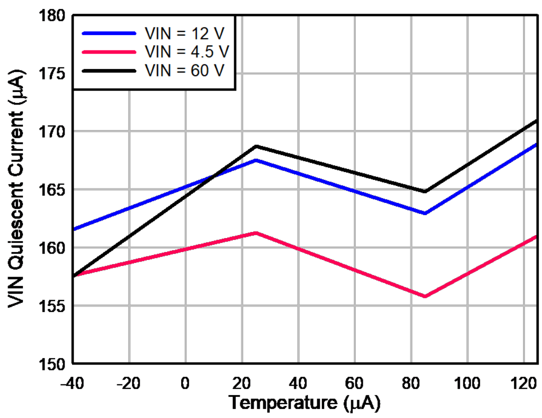


Figure 21. Device Quiescent Current vs Junction Temperature

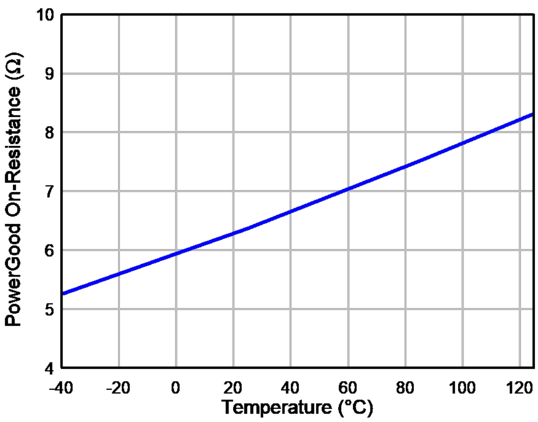


Figure 22. PWRGD On-resistance vs Junction Temperature

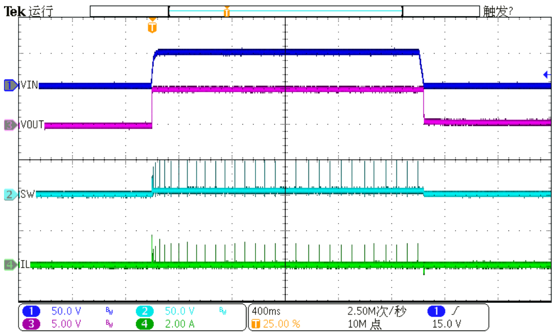


Figure 23. Power Cycle Without Load Current

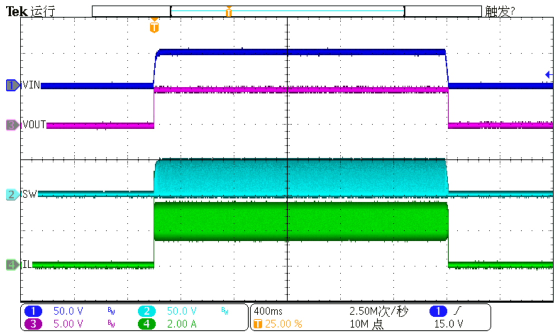


Figure 24. Power Cycle With 2.5-A Load Current

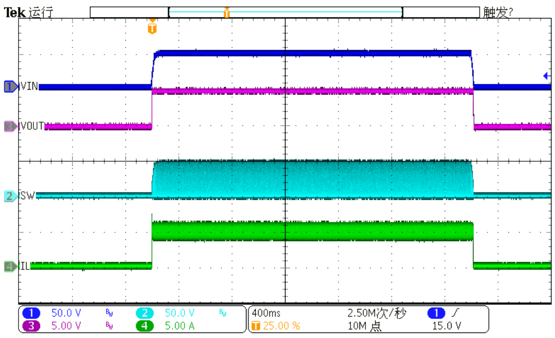


Figure 25. Power Cycle With 5-A Load Current

V_{IN} = 48 V I_{OUT} = 5 A T_A = 25 °C

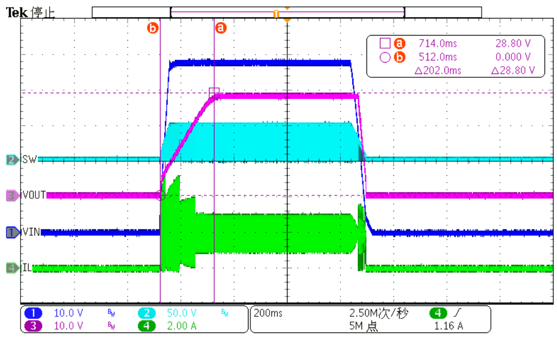


Figure 26. Power Cycle With 5 V Output

V_{IN} = 48 V T_A = 25 °C

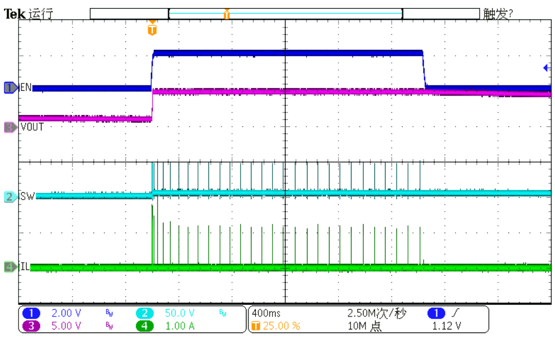


Figure 27. EN Cycle Without Load Current

V_{IN} = 48 V I_{OUT} = 0 A T_A = 25 °C

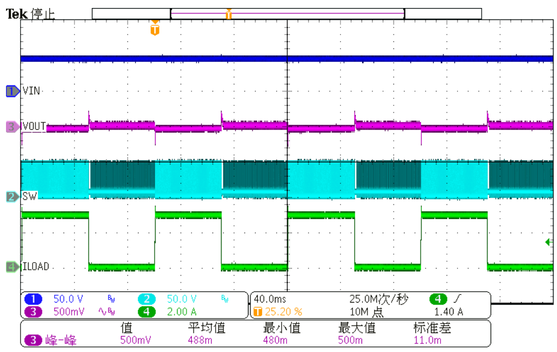


Figure 28. Load Transient

V_{IN} = 48 V I_{OUT} = 0 A to 3 A, 1 A/μs T_A = 25 °C

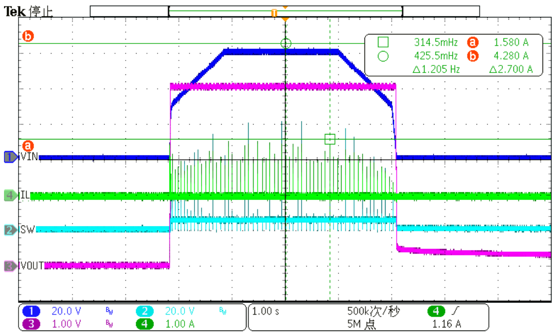


Figure 29. Line Transient without Output Current

V_{IN} = 30 V to 65 V I_{OUT} = 0 A T_A = 25 °C

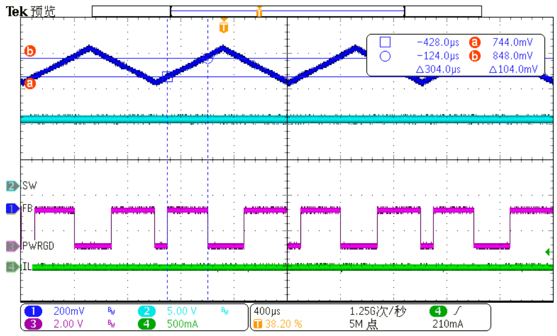


Figure 30. Under-voltage and Over-voltage Protection

V_{IN} = 48 V I_{OUT} = 0 A T_A = 25 °C

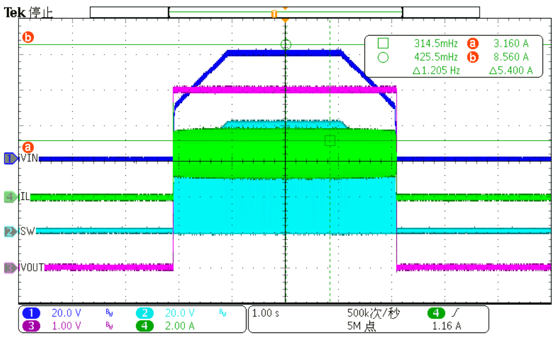


Figure 31. Line Transient Without Load Current

V_{IN} = 30 V to 65 V I_{OUT} = 2.5 A T_A = 25 °C

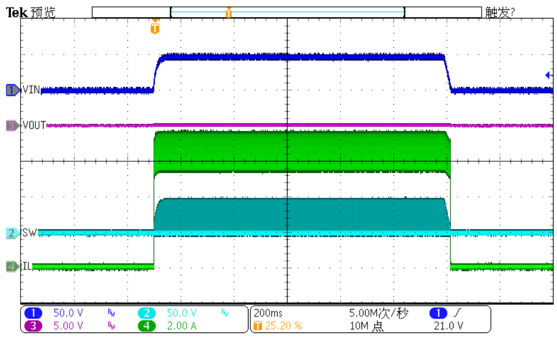


Figure 32. Power Cycle With Output Short To GND

V_{IN} = 48 V I_{OUT} = 0 A T_A = 25 °C

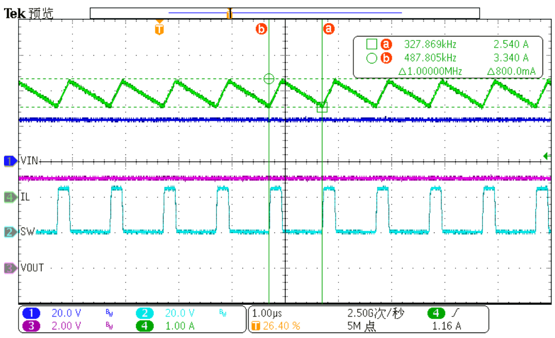


Figure 33. Switching at 1 MHz

RT = 91 kΩ I_{OUT} = 3 A T_A = 25 °C

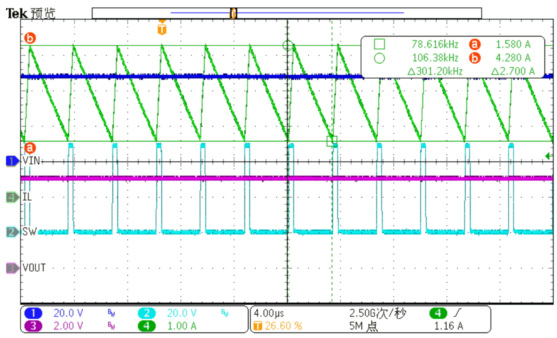


Figure 34. Switching at 300 kHz

RT = 330 kΩ I_{OUT} = 3 A T_A = 25 °C

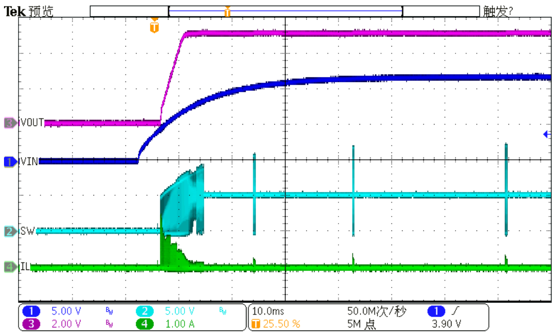


Figure 35. Soft-Start

V_{IN} = 12 V I_{OUT} = 0 A T_A = 25 °C

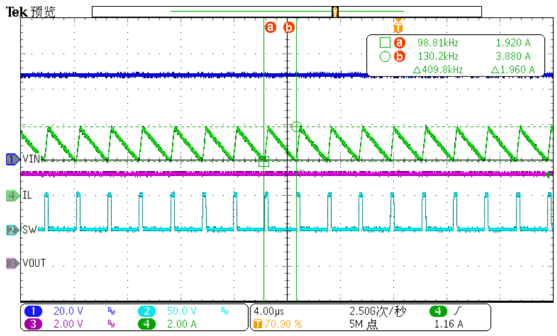


Figure 36. Switching at 400kHz

Detailed Description

Overview

The TPP60508 is a 60-V, 5-A output, non-synchronous, step-down, and switch-mode converter with integrated high-side power MOSFET.

The TPP60508 employs current-mode control supporting simple external compensation and flexible component selection. It also supports low quiescent current mode with pulse-skipping and ultra-low sleep current.

With the integrated phase-locked loop, the TPP60508 can synchronize with an external clock source with wide frequency selection, optimized for efficiency, physical dimensions, and electromagnetic interference (EMI).

Protection and diagnostic features protect the device as well as the system power supply. By using open-drain power-good output, the user system is able to distinguish if the output supply is within the target voltage range. The soft-start feature, which controls the output ramping, can be set independently with external resistors to soft-start or sequencing/tracking mode. Current limit, frequency foldback, and over-temperature protection improve system-level robustness.

Functional Block Diagram

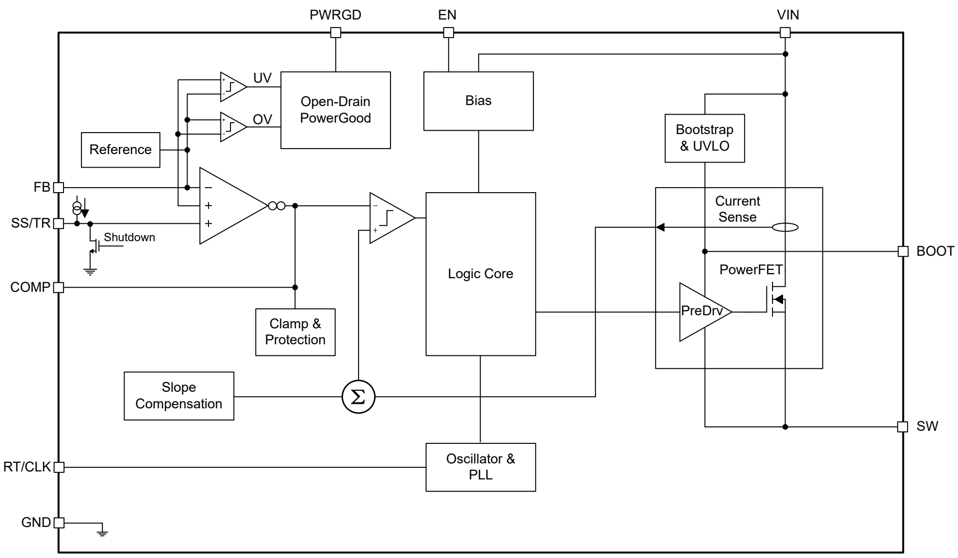


Figure 37. Functional Block Diagram

Feature Description

Fixed Frequency Peak Current Mode Control

The TPP60508 uses peak current mode control with adjustable switching frequency. The feedback voltage is sensed through the FB pin to compare with the internal voltage reference by an error amplifier. The output of the error amplifier is compared by the PWM comparator with internal voltage ramp and controls the high-side power switch. Internal oscillator controls the frequency of switching high-side MOSFET.

The high-side switching current is sensed internally as part of the voltage ramp. The internal voltage ramp compensates control loop from sub-harmonic oscillations when duty-cycles are greater than 50%. Once the PWM comparator detects peak switching current reaches the threshold level set by the COMP voltage, the high-side MOSFET is switched off. The COMP pin is also clamped for current limiting and pulse-skipping mode.

The transconductance error amplifier converts the error voltage between the FB pin voltage and the internal voltage, whichever lower of the soft-start voltage or internal voltage reference V_{FB}, to current with transconductance gm of 350 μMhos during normal operation conditions. During soft-start operation, transconductance is reduced to ensure smooth soft-start. It is recommended to connect compensation network between the COMP pin and the GND pin to ensure stability across all working ranges. The details are discussed in the application chapter.

Setting Output Voltage

The precision internal voltage reference produces a 0.8-V voltage reference with ±1.5% tolerance across operating temperature and voltage ranges. The resistor divider from the output voltage to the FB pin sets the output voltage.

$$R_H = R_L \times \left(\frac{V_{OUT} - V_{FB}}{V_{FB}}\right) \tag{1}$$

Pulse-Skipping Light-Load Operation

The TPP60508 enters pulse-skipping operation when peak switching current is below the internal threshold. In the pulse-skipping mode, the device clamps COMP at 0.6 V and stops switching high-side MOSFET. As the output voltage falls and differential input voltage increase, the error amplifier output increases. When the COMP voltage rises above the pulse skipping threshold, the device resumes switching the high-side MOSFET.

The current threshold is equivalent to the current of a nominal COMP voltage at 1 V. As the device uses peak switching current for pulse-skipping threshold, the threshold is also dependent on the output inductance.

Soft-Start with Pre-Biased Capability

The device uses the SS/TR node to implement a programmable soft-start feature by controlling ramping up reference voltage. The reference voltage will be the lower of internal reference voltage and SS/TR voltage. The timing of soft-start is programmable via external capacitor connected to the SS/TR node.

An internal constant-current source of 1.7 μA charges up the external SS/TR capacitor to an internally clamped 2.7 V. The timing can be calculated as below equation, measured from 10% to 90%.

$$T_{ss} = \frac{V_{REF} \times C_{SS} \times (90\% - 10\%)}{I_{SS}} \tag{2}$$

To ensure proper start-up, the device will discharge the SS/TR voltage upon powering up if the SS/TR voltage is above 54 mV. During any case the device stops switching, such as undervoltage lockout (UVLO), EN pulled low, or over temperature protection, the device will discharge SS/TR below 54 mV before switching.

The device also supports using SS/TR input for tracking as well as power supply sequencing. Sequencing needs to be carefully designed to ensure the system can recover from any fault.

RT/CLK

The device supports wide switching frequency from 100 kHz to 2500 kHz. The frequency is programmable via resistor connected between RT/CLK and GND. The switching frequency will affect solution size, efficiency, and minimal duty cycle. It is suggested that all factors taken care of when selecting switching frequency. The resistor can be calculated via the following equation:

$$f = \frac{k}{R_{RT}} \tag{3}$$

$k=10^{11}$

The device switching clock supports external clock sources for synchronization. Once a square wave is applied at the RT/CLK pin, the rising edge of SW synchronizes to the falling edge of RT/CLK. It is also suggested to connect a frequency set resistor to RT/CLK pin in case the external clock source is not available.

The first rising edge of RT/CLK sets the device from free-running frequency mode to synchronization mode. The internal 0.5-V voltage source is removed and the RT/CLK is set to the high impedance mode. It takes 78 μs to lock on external clock frequency. When the external clock source stops, the device will switch back to the free running frequency mode with frequency set by the external resistor. During the transition, the device frequency will stay at 70 kHz and then switch to the free-running frequency.

The device will foldback frequency by 1, 2, 4, and 8 depending on the FB voltage. This is to ensure that during normal start-up and fault conditions, the device is able to increase its period and off time. This is helpful when output is short-circuit to GND, the longer off time allows the inductor current to decay.

When selecting the switching frequency, the device minimal on-time needs to be taken into considerations. The device T_{min_on} is 175 ns typical, measured at 60 V. When the device is desired on-time less than minimal on-time, the device may skip pulses and lowers switching frequency.

Protection

Undervoltage Lockout (UVLO)

The device has a undervoltage lockout feature with a default rising threshold of 4.3 V. It can be adjusted by using the EN pin with external resistors. A weak current source of 1.2 μA pulls up the EN pin to the internal voltage rail. Another 3.4-μA hysteresis current source provides the hysteresis voltage between the rising and falling threshold. The resistor values can be calculated via below equations.

$V_{SYS\_UVLO\_H}$ is the desired system-level undervoltage protection rising threshold voltage, $V_{SYS\_UVLO\_L}$ is the desired system-level undervoltage protection falling threshold voltage. RUVLOH and RUVLOL are depicted in the Figure 38.

$$R_{UVLOH} = \frac{V_{SYS\_UVLO\_H} - V_{SYS\_UVLO\_L}}{I_{EN\_hys}} \tag{4}$$

$$R_{UVLOL} = \frac{V_{EN}}{\frac{V_{SYS\_UVLO\_H} - V_{EN}}{R_{UVLOH}} + I_{EN}} \tag{5}$$

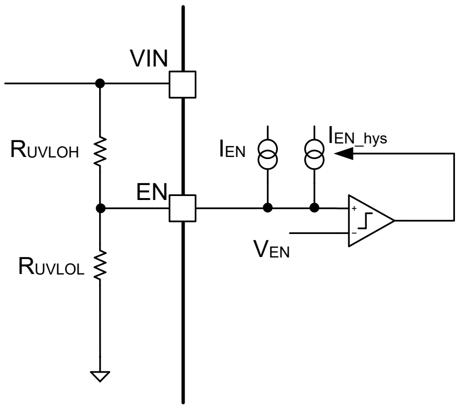


Figure 38. Using EN as UVLO Threshold Adjustment

Over-Current Protection

The device employs peak current mode control by controlling the peak current of the internal high-side power transistor. The high-side transistor current is converted to a voltage signal and compared to the COMP pin. When the peak switching current is above the threshold set by the COMP voltage, the device turns off the high-side power transistor.

When the device is in the over-current scenario, the output voltage is pulled low, and device will increase switching current threshold until it reaches the internal current limit threshold. Once the switching current is above the threshold, the device will turn off the transistor as current limit. Delay needs to be taken in to account that may cause the peak inductor current slightly higher than the open-loop current limit.

Once the over-current load is removed, the device will resume normal operation in the following cycle.

Power Good

The device uses an open-drain output PWRGD to signal if the output voltage is operating within the boundaries. If the FB voltage is within the 93% and 106% of internal reference voltage, the PWRGD pull-down will be disabled and pulled up by externally resistor. The external pull up voltage source is recommended to be less than 5.5 V with a 1-kΩ resistor. If FB voltage is lower than 90% or greater than 108% of internal reference voltage, the PWRGD will be pulled low.

If UVLO, over temperature protection or EN going low, the PWRGD will also be pulled low. When supply voltage is below 2 V, the PWRGD may not be at any defined state.

Over-Voltage Protection

The device stops high-side FET switching when it detects the FB voltage is above the over-voltage protection (OVP) rising threshold (108% of internal reference voltage). When the voltage falls below the falling threshold (106% of internal reference voltage), it resumes switching high-side FET. With the OVP feature, the device is able to minimize the voltage overshoot during the load transient with low-output capacitance.

Over-Temperature Shutdown

When the device senses the junction temperature is above the internal rising threshold of 165°C, the device stops the high-side FET switching. Once the device junction temperature falls below the falling threshold of 150°C, the device restarts the device with power-up sequence.

The device will discharge the SS/TR to GND as part of power-up sequence. Care must be taken that the SS/TR is able to be pulled low to avoid a deadlock scenario that may prevent the device from re-start.

Application and Implementation

Note
Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPP60508 is a non-synchronous 60-V 5-A step-down regulator with the integrated high-side FET. The device is capable to support a wide range of voltage rails including 12 V, 24 V, and 48 V. It is widely used in communication, industrial, and automotive applications.

Typical Application

The figure below shows the typical application schematic.

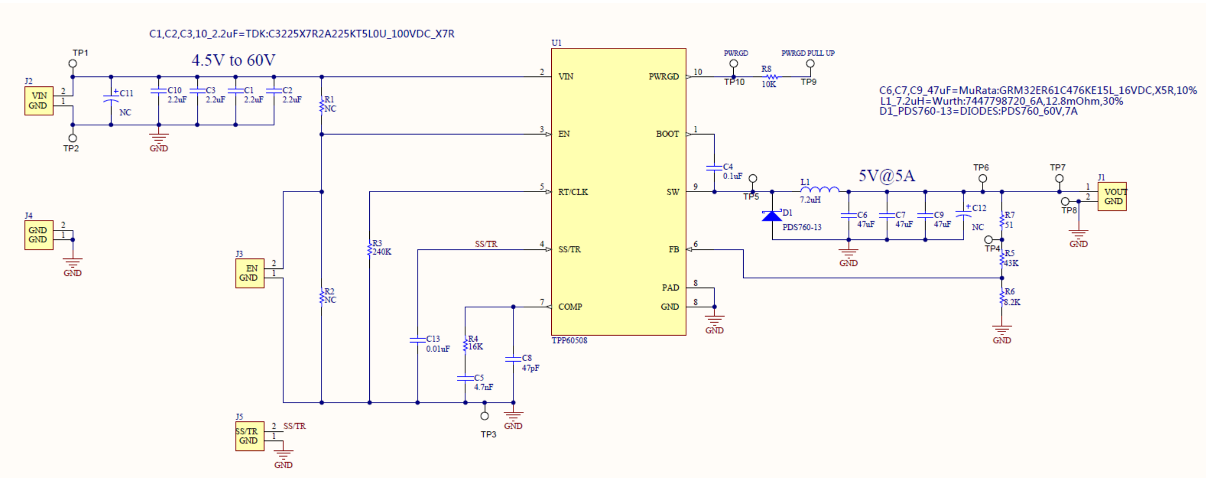
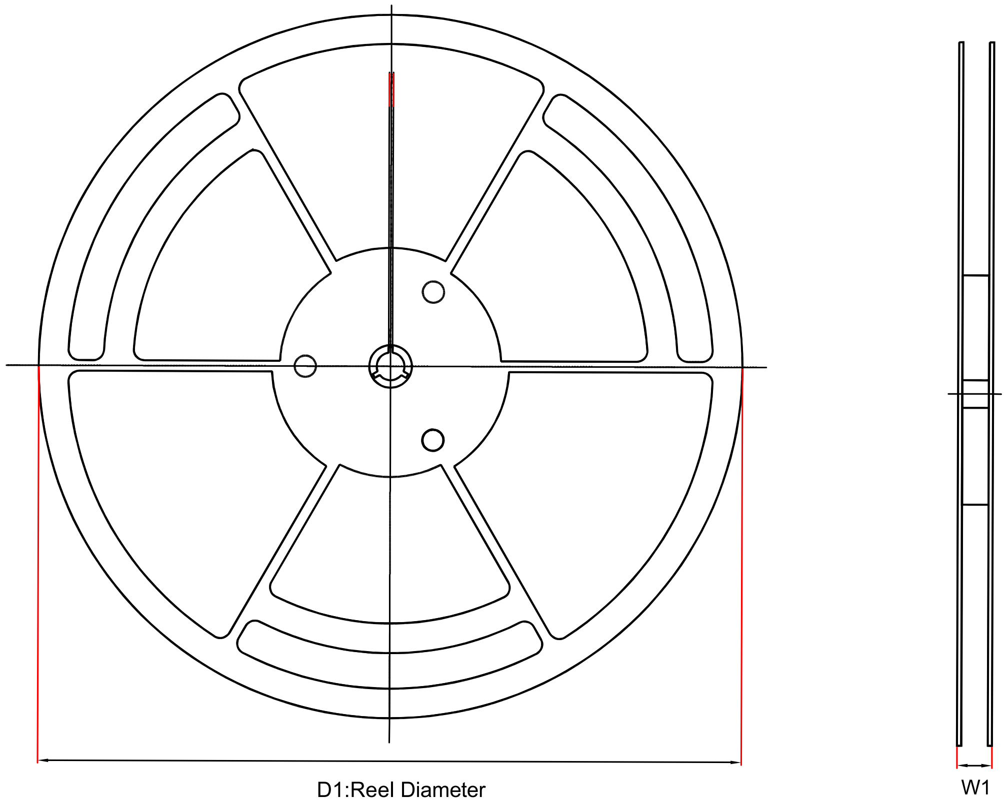
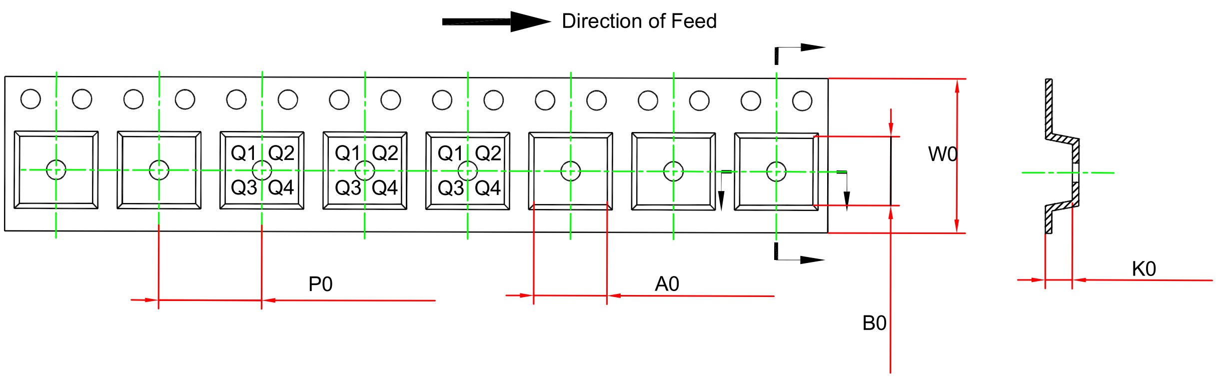


Figure 39. Typical Application Circuit

Tape and Reel Information



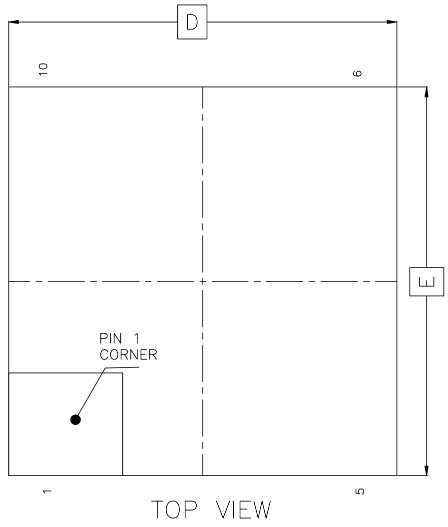


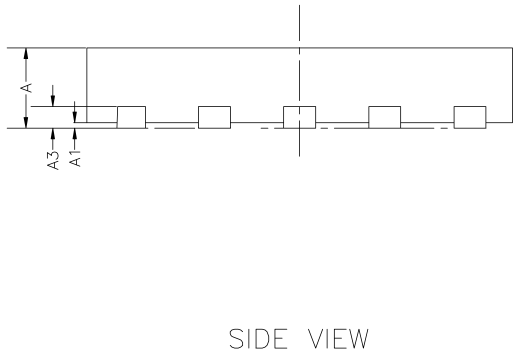
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPP60508L1-DF9R-S	DFN4X4-10	330	17.6	4.2	4.2	1.1	8.0	12	Q2
TPP60508L1-DF9R	DFN4X4-10	330	17.6	4.2	4.2	1.1	8.0	12	Q2

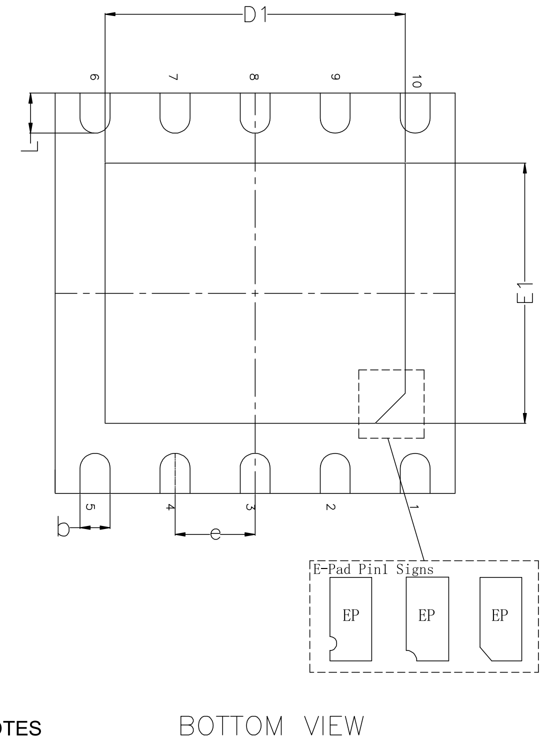
Package Outline Dimensions

DFN4X4-10-A

Package Outline Dimensions DF9(DFN4X4-10-A)







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
b	0.250	0.350	0.010	0.014
A3	0.150	0.250	0.006	0.010
D	3.900	4.100	0.154	0.161
D1	2.950	3.050	0.116	0.120
E	3.900	4.100	0.154	0.161
E1	2.550	2.650	0.100	0.104
e	0.800 BSC		0.031 BSC	
L	0.350	0.450	0.014	0.018

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Order Information

Order Number	Operating Ambient Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPP60508L1-DF9R-S	−40°C to 125°C	DFN4X4-10	P658	Level 1	Tape & Reel, 3000	Green
TPP60508L1-DF9R	−40°C to 125°C	DFN4X4-10	P658	Level 1	Tape & Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

IMPORTANT NOTICE AND DISCLAIMER

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