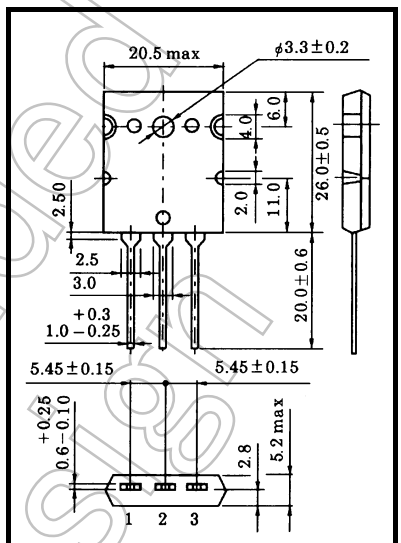
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (L^2−π−MOSIII)

2SK1382

Relay Drive, Motor Drive and DC−DC Converter Applications

- 4-V gate drive
- Low drain−source ON resistance : $R_{DS\ (ON)}$ = 15 mΩ (typ.)
- High forward transfer admittance : $|Y_{fs}|$ = 47 S (typ.)
- Low leakage current : I_{DSS} = 100 μA (max) (V_{DS} = 100 V)
- Enhancement mode : V_{th} = 0.8 to 2.0 V (V_{DS} = 10 V, I_D = 1 mA)

Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	2-21F1B

Weight: 9.75 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain−source voltage		V_{DSS}	100	V
Drain−gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	100	V
Gate−source voltage		V_{GSS}	±20	V
Drain current	DC (Note 1)	I_D	60	A
	Pulse (Note 1)	I_{DP}	240	
Drain power dissipation (Tc = 25°C)		P_D	200	W
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

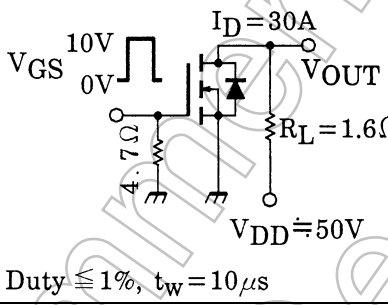
Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th\ (ch-c)}$	0.625	°C / W
Thermal resistance, channel to ambient	$R_{th\ (ch-a)}$	35.7	°C / W

Note 1: Ensure that the channel temperature does not exceed 150°C.

This transistor is an electrostatic-sensitive device.
Please handle with caution.

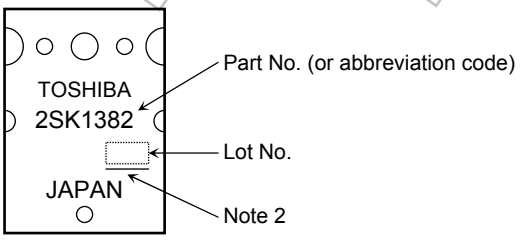
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V	—	—	±100	nA
Drain cut−off current		I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V	—	—	100	μA
Drain−source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	100	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	0.8	—	2.0	V
Drain−source ON resistance		$R_{DS\ (ON)}$	V_{GS} = 4 V, I_D = 30 A	—	20	29	mΩ
			V_{GS} = 10 V, I_D = 30 A	—	15	20	
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 30 A	30	47	—	S
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	7000	—	pF
Reverse transfer capacitance		C_{rss}		—	400	—	
Output capacitance		C_{oss}		—	2700	—	
Switching time	Rise time	t_r		—	16	—	ns
	Turn−on time	t_{on}		—	55	—	
	Fall time	t_f		—	80	—	
	Turn−off time	t_{off}		—	280	—	
Total gate charge (Gate−source plus gate−drain)		Q_g	V_{DD} ≈ 80 V, V_{GS} = 10 V, I_D = 60 A	—	176	—	nC
Gate−source charge		Q_{gs}		—	132	—	
Gate−drain (“miller”) charge		Q_{gd}		—	44	—	

Source−Drain Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	60	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	240	A
Forward voltage (diode)	V_{DSF}	I_{DR} = 60 A, V_{GS} = 0 V	—	—	−1.6	V
Reverse recovery time	t_{rr}	I_{DR} = 60 A, V_{GS} = 0 V dI_{DR} / dt = 50 A / μs	—	300	—	ns
Reverse recovered charge	Q_{rr}		—	0.75	—	μC

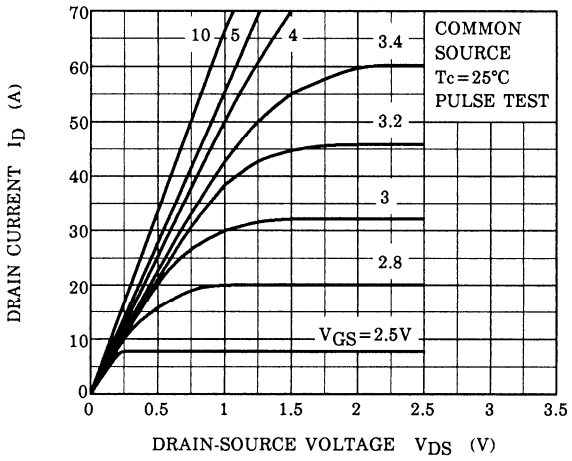
Marking



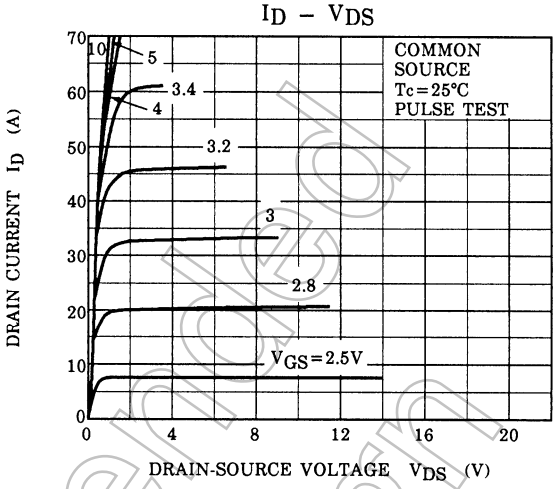
Note 2: A line under a Lot No. identifies the indication of product Labels.
Not underlined: [[Pb]]/INCLUDES > MCV
Underlined: [[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. The RoHS is the Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

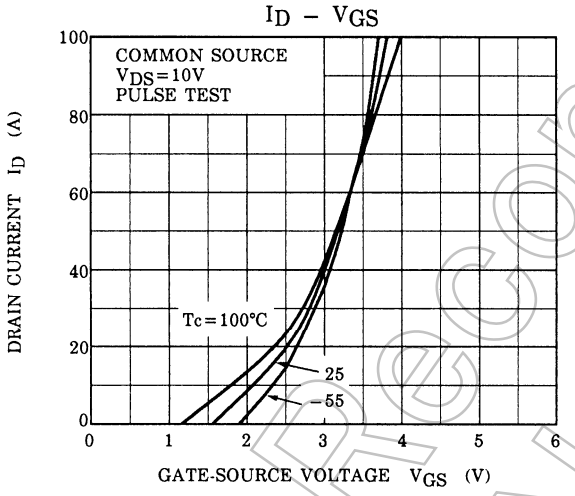
$I_D - V_{DS}$



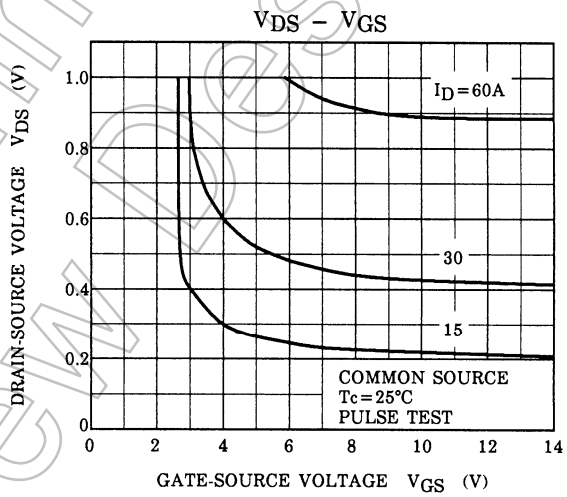
$I_D - V_{DS}$



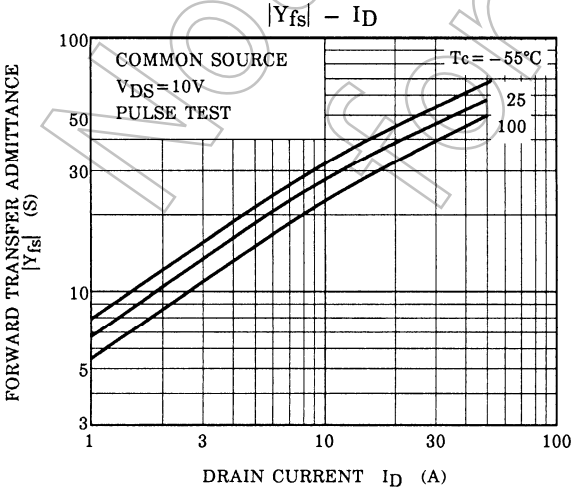
$I_D - V_{GS}$



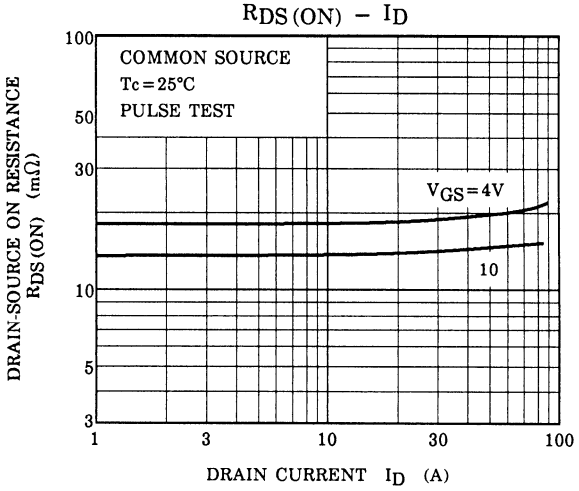
$V_{DS} - V_{GS}$



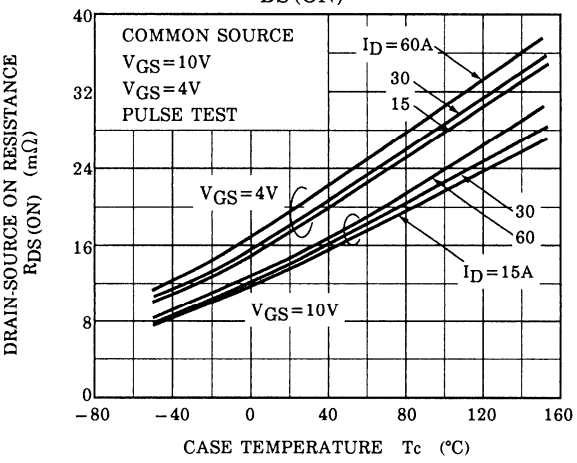
$|Y_{fs}| - I_D$



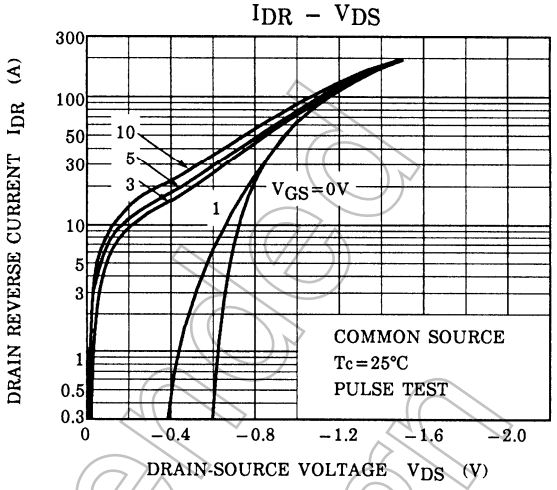
$R_{DS\,(ON)} - I_D$



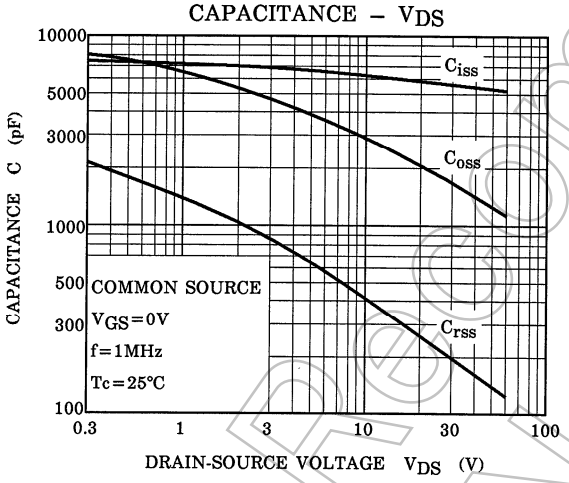
$R_{DS(ON)}$ – Tc



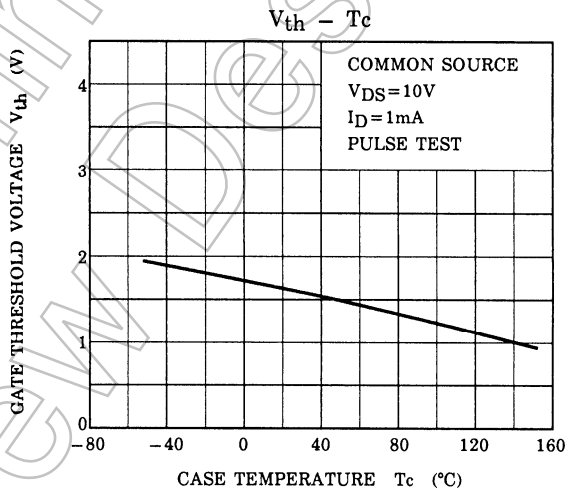
I_{DR} – V_{DS}



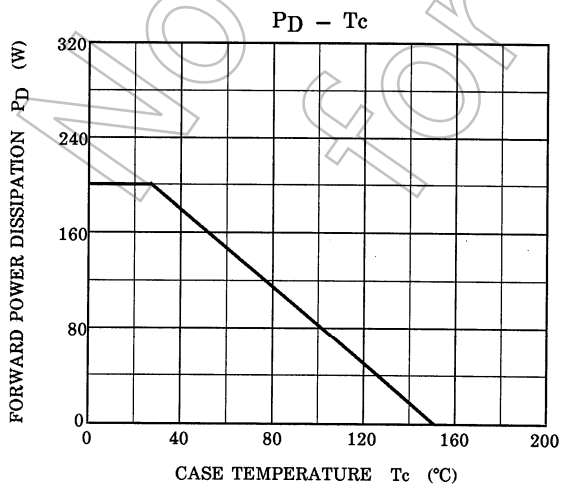
CAPACITANCE – V_{DS}



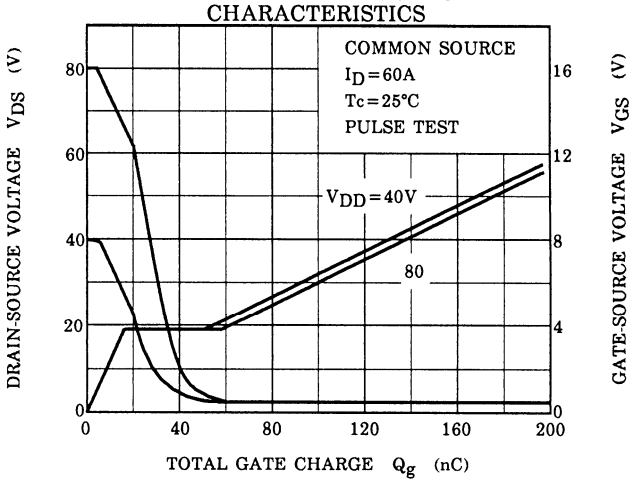
V_{th} – Tc

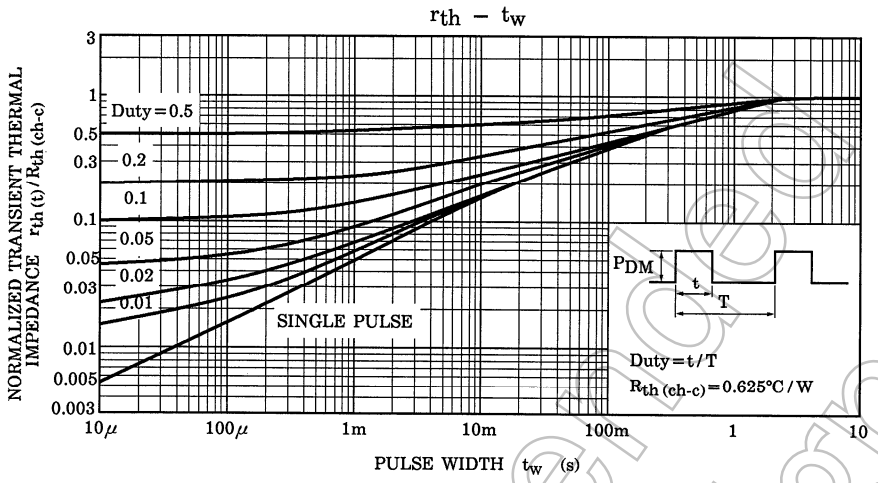


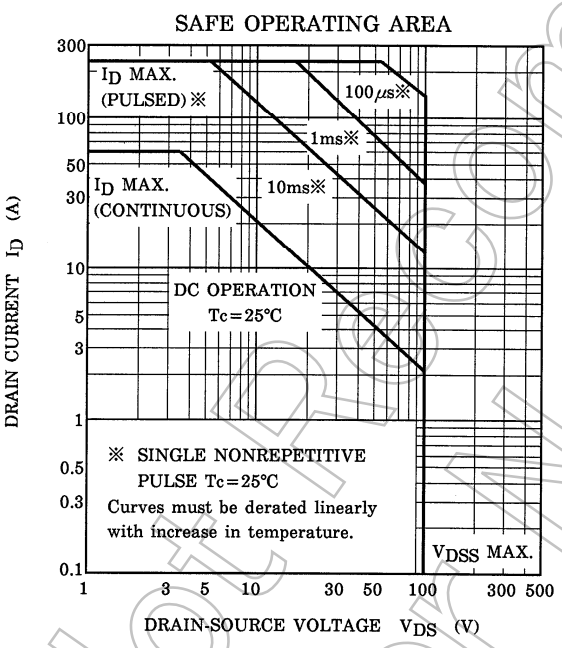
P_D – Tc



DYNAMIC INPUT / OUTPUT CHARACTERISTICS







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