OPA814 600-MHz, High-Precision, Unity-Gain Stable, FET-Input Operational Amplifier

1 Features

- Wide bandwidth:
  - Gain-bandwidth product: 250 MHz
  - Bandwidth (G = 1 V/V): 600 MHz
  - Large-signal bandwidth (2 V_{PP}): 200 MHz
  - Slew rate: 750 V/µs
- High precision:
  - Input offset voltage: 250 µV (maximum)
  - Input offset voltage drift: 3.5 µV/°C (maximum)
- Input voltage noise: 5.3 nV/√Hz
- Input bias current: 2 pA
- Low distortion (R_L = 100 Ω, V_O = 2 V_{PP}):
  - HD2, HD3 at 10 MHz: –75 dBc, –85 dBc
- Supply range: 6 V to 12.6 V
- Supply current: 16 mA
- Performance upgrade to OPA656

2 Applications

- High-speed data acquisition (DAQ)
- Active probes
- Oscilloscopes
- Optical communication modules
- Test and measurement front-ends
- Medical and chemical analyzers
- Optical time-domain reflectometry (OTDR)

3 Description

The OPA814 is a unity-gain stable, voltage-feedback operational amplifier for high-speed, high-precision, and wide-dynamic-range applications.

The OPA814 has a low-noise junction gate field-effect transistor (JFET) input stage that features a wide gain bandwidth of 250 MHz and a supply range from 6 V to 12.6 V. The fast slew rate of 750 V/µs allows a wide large-signal bandwidth and low distortion when used as high impedance buffer in high-speed digitizers, active probes, and other test and measurement applications.

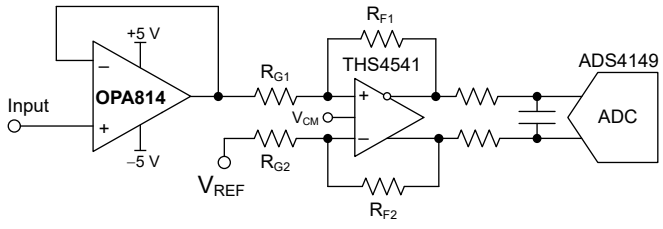
The OPA814 offers extremely low input offset voltage of ±250 µV and offset voltage drift of ±3.5-µV/°C. The combination of picoamperes of input bias current and low input voltage noise (5.3 nV/√Hz) makes the OPA814 an excellent wideband transimpedance amplifier in optical test and communication equipment, as well as medical and scientific instrumentation.

The OPA814 is available in an 8-pin SOIC package. This device is specified to operate over the industrial temperature range of –40°C to +85°C.

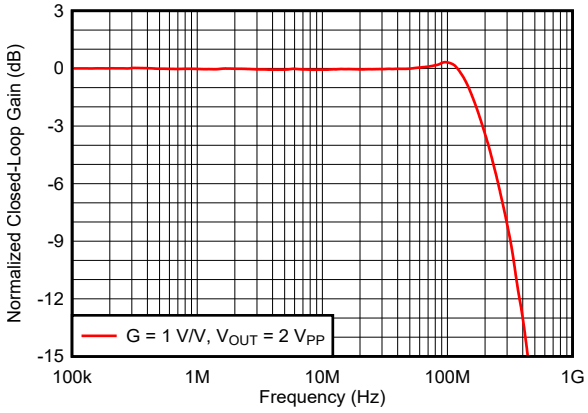
Package Information

PART NUMBER(1)	PACKAGE(2)	PACKAGE SIZE(3)
OPA814	D (SOIC, 8)	4.9 mm × 6 mm
	DBV (SOT-23, 5)	2.9 mm × 2.8 mm

(1) See the *Device Comparison Table*.
(2) For more information, see Section 11.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.



High-Input-Impedance Digitizer Front End



Large-Signal Frequency Response

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4 Device Comparison Table

DEVICE	SUPPLY VOLTAGE (V)	GBW (MHz)	INPUT	SLEW RATE (V/µs)	VOLTAGE NOISE (nV/√Hz)	MINIMUM STABLE GAIN (V/V)
OPA814	±6.3	250	FET	750	5.3	1
OPA817	±6.3	400	FET	1000	4.5	1
OPA818	±6.5	2700	FET	1400	2.2	7
OPA656	±5	230	FET	290	7	1
OPA858	±2.5	5500	CMOS	2000	2.5	7
OPA859	±2.5	900	CMOS	1150	3.3	1
THS4631	±15	210	FET	1000	7	1

5 Pin Configuration and Functions

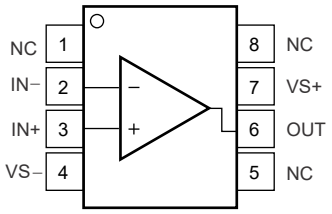


Figure 5-1. D Package, 8-Pin SOIC (Top View)

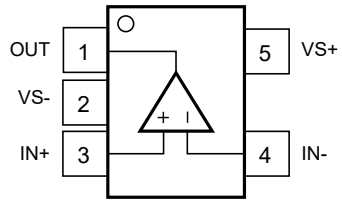


Figure 5-2. DBV Package, 5-Pin SOT-23 (Top View)

Table 5-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	NO.			
	D (SOIC)	DBV (SOT-23)		
IN–	2	4	Input	Inverting input
IN+	3	3	Input	Noninverting input
NC	1, 5, 8	—	—	No internal connection to the die.
OUT	6	1	Output	Output of amplifier
VS–	4	2	Power	Negative power supply
VS+	7	5	Power	Positive power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Total supply voltage (V_{S+}– $V_{S–}$)		13	V
	dV_S/dT for supply turn-on and turn-off(2)		1	V/µs
V_I	Input voltage	$V_{S–}$	V_{S+}	V
V_{ID}	Differential input voltage	$V_{S–}$	V_{S+}	V
I_I	Continuous input current(3)		±10	mA
I_O	Continuous output current(4)		±30	mA
	Continuous power dissipation	See *Thermal Information*		
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Staying below this specification makes sure that the edge-triggered ESD absorption devices across the supply pins remain off.
(3) Continuous input current limit for the ESD diodes to supply pins.
(4) Long-term continuous current for electromigration limits.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{S+} – $V_{S–}$	Total supply voltage	6	10	12.6	V
T_A	Ambient temperature	–40	25	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA814		UNIT
		D (SOIC)	DBV (SOT-23)	
		8 PINS	5 PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance	122.9	154	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	63.1	88.7	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	66.3	55.4	°C/W
$Ψ_{JT}$	Junction-to-top characterization parameter	16.1	33.7	°C/W
Y_{JB}	Junction-to-board characterization parameter	65.5	55.1	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics:

at T_A ≅ 25°C, V_S = ±5 V, G = 1 V/V, R_F = 0 Ω, R_F = 250 Ω for G ≥ 2 V/V, R_L = 100 Ω, and input and output referenced to mid-supply (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	V_{OUT} = 200 mV_{PP}, G = 1 V/V		600		MHz
		V_{OUT} = 200 mV_{PP}, G = 2 V/V		250		
		V_{OUT} = 200 mV_{PP}, G = 10 V/V		25		
	Gain-bandwidth product	G >= 10 V/V		250		MHz
LSBW	Large-signal bandwidth	V_{OUT} = 2 V_{PP}, G = 1 V/V		200		MHz
		V_{OUT} = 2 V_{PP}, G = 2 V/V		165		
		V_{OUT} = 4 V_{PP}, G = 1 V/V		110		
	Bandwidth for 0.1-dB flatness	V_{OUT} = 2 V_{PP}		70		MHz
	Peaking at G = 1 V/V	V_{OUT} = 200 mV_{PP}		0.6		dB
SR	Slew rate	V_{OUT} = 1-V step, G = 2 V/V		550		V/µs
		V_{OUT} = 4-V step, G = 1 V/V		750		
t_R, t_F	Rise, fall time	V_{OUT} = 200-mV step, G = 1 V/V, 10%–90%		0.8		ns
		V_{OUT} = 200-mV step, G = 2 V/V, 10%–90%		1.3		
	Settling time to 0.1%	V_{OUT} = 2-V step, G = 1 V/V		7		ns
	Settling time to 0.02%	V_{OUT} = 2-V step, G = 2 V/V		16		ns
	Overshoot	V_{OUT} = 2-V step		6		%
	Undershoot	V_{OUT} = 2-V step		10		%
	Output overdrive recovery time	V_{IN} = ±2.5 V, G = 2 V/V		30		ns
HD2	Second-order harmonic distortion	f = 1 MHz, V_{OUT} = 2 V_{PP}, R_L = 1 kΩ		–119		dBc
HD3	Third-order harmonic distortion			–130		
HD2	Second-order harmonic distortion	f = 10 MHz, V_{OUT} = 2 V_{PP}, R_L = 100 Ω		–75		dBc
HD3	Third-order harmonic distortion			–85		
e_N	Input voltage noise	f > 100 kHz		5.3		nV/√Hz
	Voltage noise 1/f corner frequency			2		kHz
	Input current noise	f > 100 kHz		11		fA/√Hz
DC PERFORMANCE						
A_{OL}	Open-loop voltage gain	V_O = ±0.5 V	75	80		dB
		V_O = ±0.5 V, T_A = –40°C to +85°C	70			
V_{OS}	Input-referred offset voltage	SOIC		50	±250	µV
		SOIC, T_A = –40°C to +85°C			±500	
		SOT-23		100	±350	
		SOT-23, T_A = –40°C to +85°C			±600	
	Input offset voltage drift[1]	T_A = –40°C to +85°C		1	±3.5	µV/°C
I_B	Input bias current			2	±20	pA
		T_A = –40°C to +85°C			±1000	
I_{OS}	Input offset current			1	±20	pA
		T_A = –40°C to +85°C			±500	

6.5 Electrical Characteristics: (continued)

at T_A ≅ 25°C, V_S = ±5 V, G = 1 V/V, R_F = 0 Ω, R_F = 250 Ω for G ≥ 2 V/V, R_L = 100 Ω, and input and output referenced to mid-supply (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
CMIR	Most positive input voltage	CMRR > 77 dB	2.1	2.7		V
		T_A = –40°C to +85°C, CMRR > 77 dB	2			
		CMRR > 53 dB	2.6	3.1		
		T_A = –40°C to +85°C, CMRR > 53 dB	2.4			
	Most negative input voltage	CMRR > 77 dB		–4.3	–3.9	V
		T_A = –40°C to +85°C, CMRR > 77 dB			–3.7	
		CMRR > 53 dB		–4.4	–4	
		T_A = –40°C to +85°C, CMRR > 53 dB			–3.8	
CMRR	Common-mode rejection ratio	V_{CM} = ±0.5 V	84	100		dB
		V_{CM} = ±0.5 V, T_A = –40 to +85°C	83			
	Input impedance common-mode			12 || 2.5		GΩ || pF
	Input impedance differential mode			1000 || 0.2		GΩ || pF
OUTPUT						
	Voltage output swing	No load	±3.7	±3.9		V
		SOIC, R_L = 100 Ω	±3.4	±3.7		
		SOT-23, R_L = 100 Ω	±3.35	±3.7		
		T_A = –40°C to +85°C, R_L = 100 Ω	±3.3			
	Linear output drive (sourcing and sinking)	V_{OUT} = ±1 V, ΔV_{OS} < 2 mV	52	70		mA
		T_A = –40 to +85°C, V_{OUT} = ±1 V, ΔV_{OS} < 3 mV	45			
	Short-circuit current			90		mA
Z_O	Closed loop output Impedance	f = 100 kHz, G = 1 V/V		0.01		Ω
POWER SUPPLY						
I_Q	Quiescent current		15.3	16	16.7	mA
		T_A = –40°C to +85°C	15.2		16.8	
PSRR+	Power-supply rejection ratio (positive)	SOIC, V_{S+} = 4.5 V to 5.5 V	79	100		dB
		SOIC, V_{S+} = 4.5 V to 5.5 V, T_A = –40°C to +85°C	76			
		SOT-23, V_{S+} = 4.5 V to 5.5 V	77	100		
		SOT-23, V_{S+} = 4.5 V to 5.5 V, T_A = –40°C to +85°C	74			
PSRR–	Power-supply rejection ratio (negative)	SOIC, $V_{S–}$ = –4.5 V to –5.5 V	79	100		dB
		SOIC, $V_{S–}$ = –4.5 V to –5.5 V, T_A = –40°C to +85°C	76			
		SOT-23, $V_{S–}$ = –4.5 V to –5.5 V	77	100		
		SOT-23, $V_{S–}$ = –4.5 V to –5.5 V, T_A = –40°C to +85°C	74			

(1) Based on electrical characterization of 32 devices. Minimum and maximum values are not specified by final automated test equipment (ATE) nor by QA sample testing. Typical specifications are ±1 sigma.

6.6 Typical Characteristics

at T_A ≅ 25°C , V_S = ±5 V, G = 1 V/V, R_F = 0 Ω, R_F = 250 Ω for other gains, R_L = 100 Ω, and input and output referenced to mid-supply (unless otherwise noted)

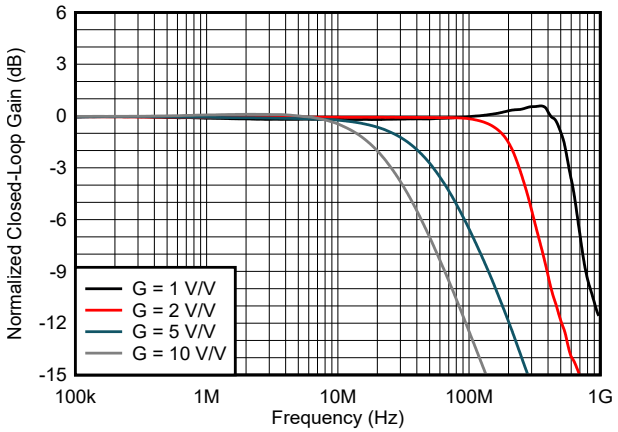


Figure 6-1. Noninverting Small-Signal Frequency Response

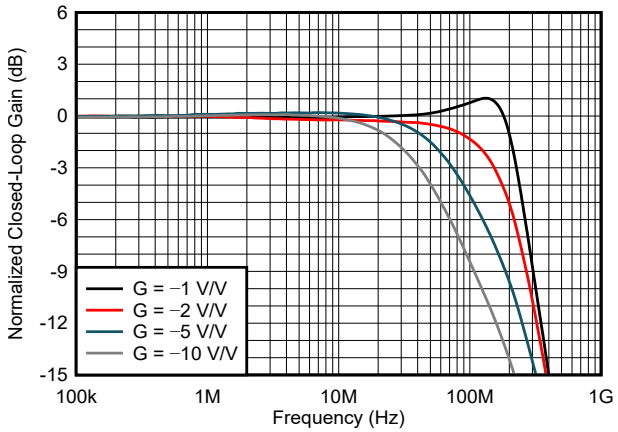


Figure 6-2. Inverting Small-Signal Frequency Response

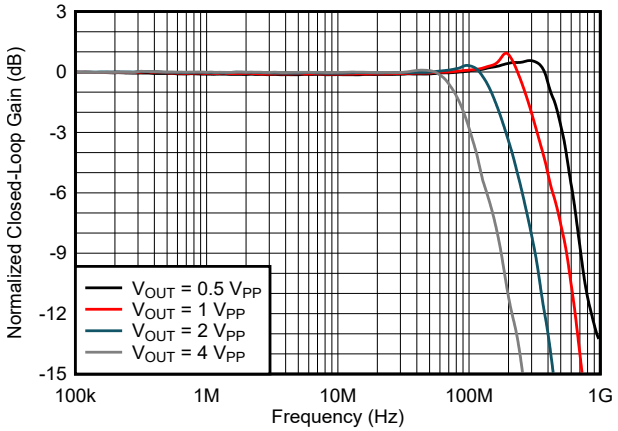


Figure 6-3. Noninverting Large-Signal Frequency Response

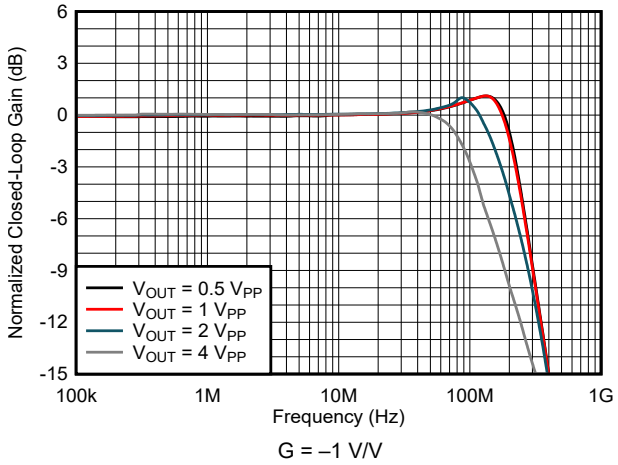


Figure 6-4. Inverting Large-Signal Frequency Response

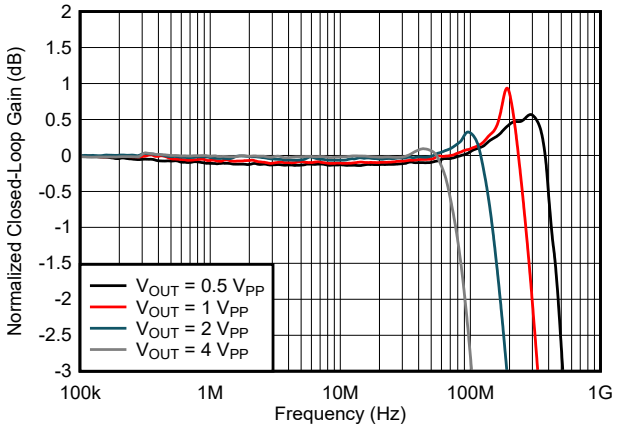


Figure 6-5. Gain Flatness vs Frequency

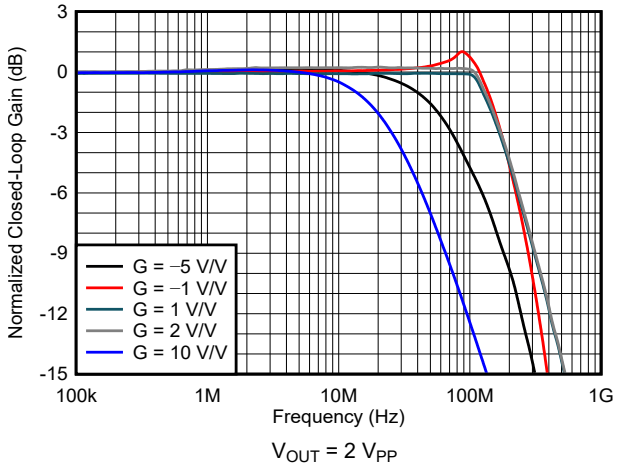
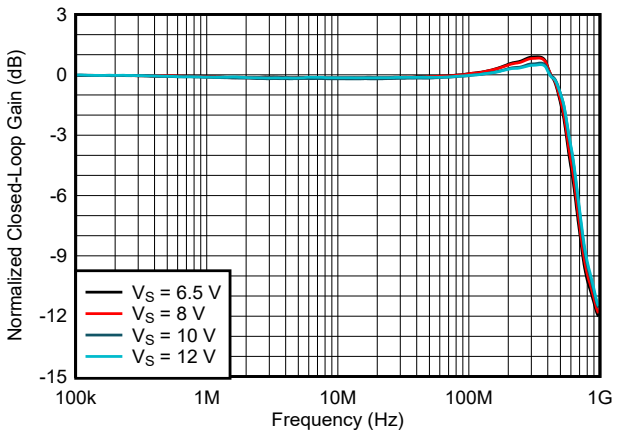


Figure 6-6. Large-Signal Frequency Response Over Gain

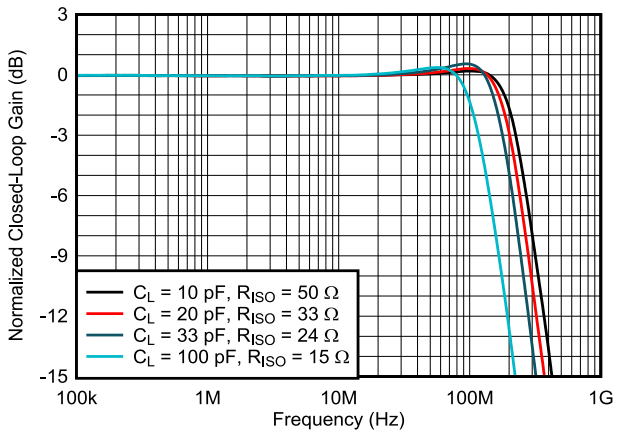
6.6 Typical Characteristics (continued)

at $T_A \cong 25°C$, $V_S = \pm 5$ V, G = 1 V/V, $R_F = 0\ \Omega$, $R_F = 250\ \Omega$ for other gains, $R_L = 100\ \Omega$, and input and output referenced to mid-supply (unless otherwise noted)



V_{OUT} = 200 mV_{PP}

Figure 6-7. Noninverting Small-Signal Frequency Response Over Supply



V_{OUT} = 200 mV_{PP}

Figure 6-8. Frequency Response vs Capacitive Load

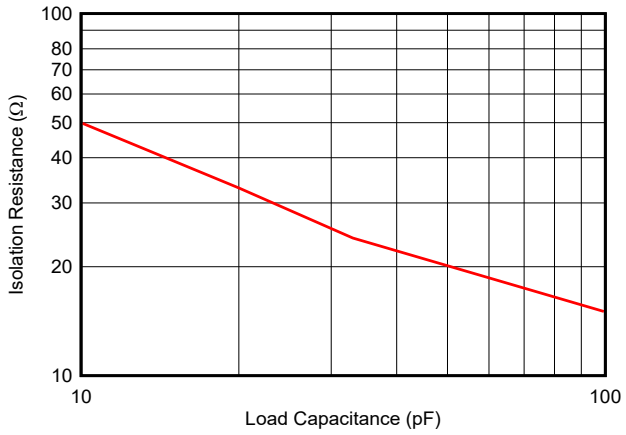


Figure 6-9. Recommended Isolation Resistor vs Capacitive Load

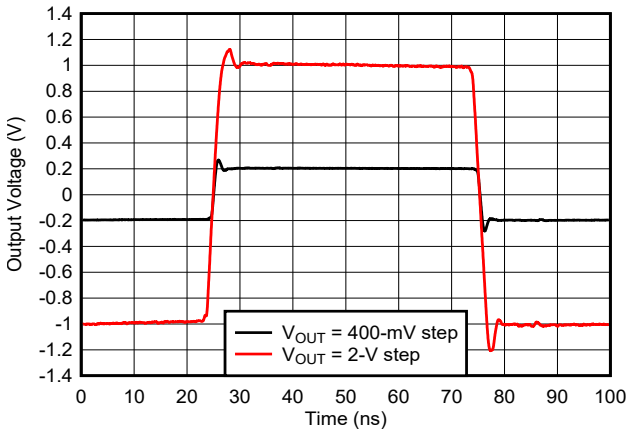
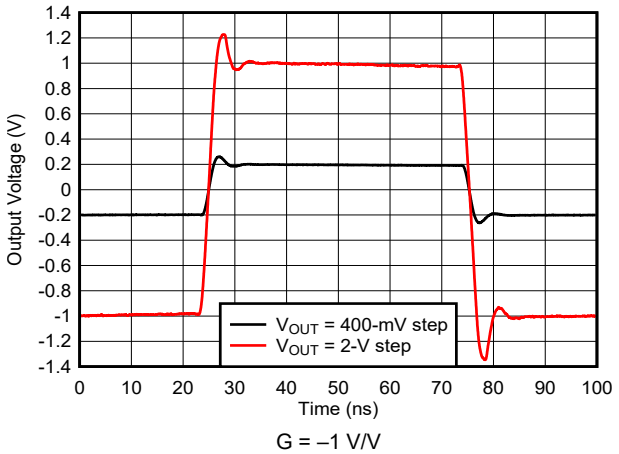
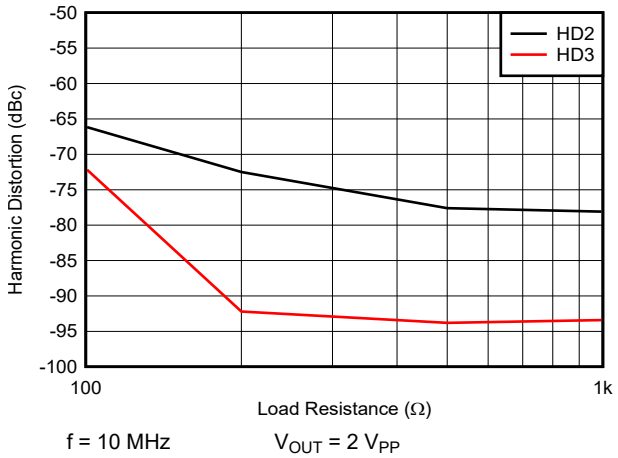


Figure 6-10. Noninverting Large-Signal Pulse Response



G = –1 V/V

Figure 6-11. Inverting Large-Signal Pulse Response

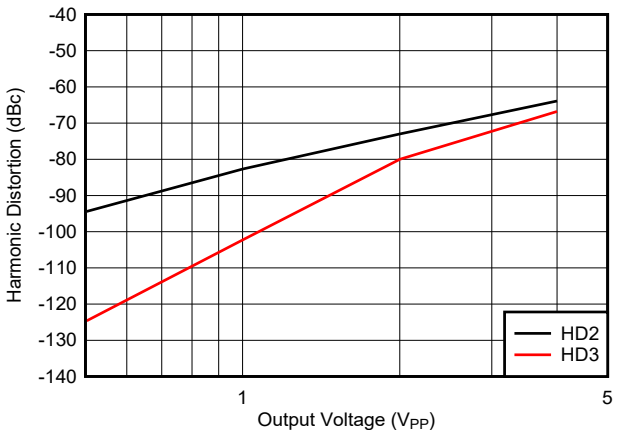


f = 10 MHz V_{OUT} = 2 V_{PP}

Figure 6-12. Harmonic Distortion vs Load Resistance

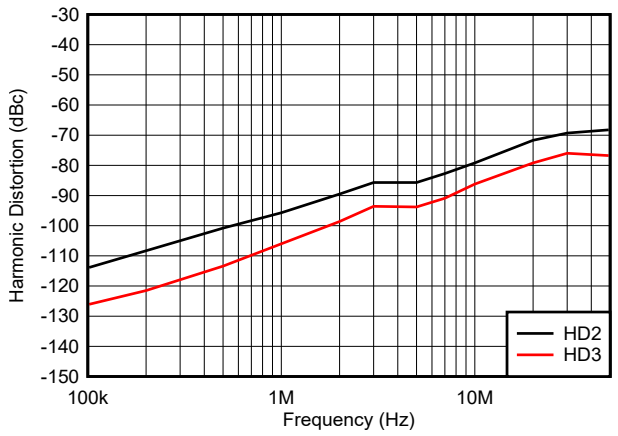
6.6 Typical Characteristics (continued)

at T_A ≅ 25°C , V_S = ±5 V, G = 1 V/V, R_F = 0 Ω, R_F = 250 Ω for other gains, R_L = 100 Ω, and input and output referenced to mid-supply (unless otherwise noted)



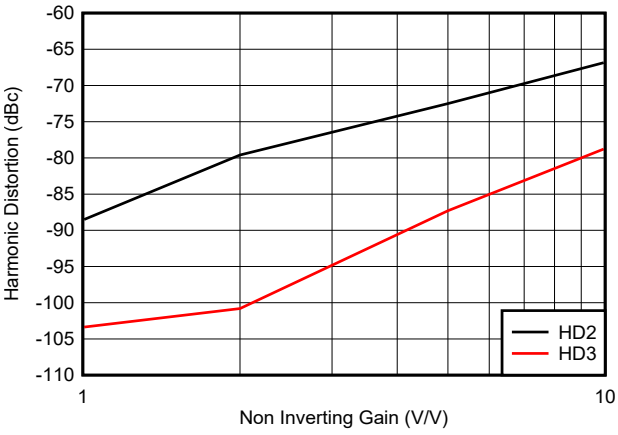
f = 10 MHz

Figure 6-13. Harmonic Distortion vs Output Voltage



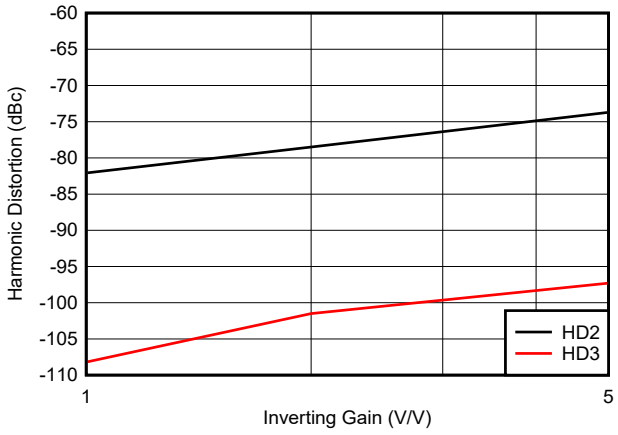
V_{OUT} = 2 V_{PP}

Figure 6-14. Harmonic Distortion vs Frequency



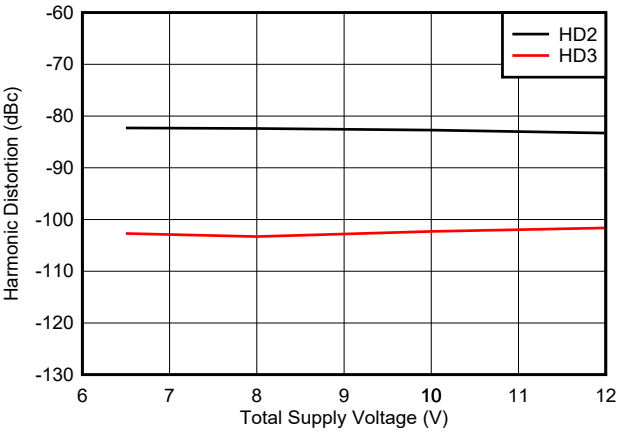
f = 5 MHz V_{OUT} = 2 V_{PP} R_L = 200 Ω

Figure 6-15. Harmonic Distortion vs Noninverting Gain



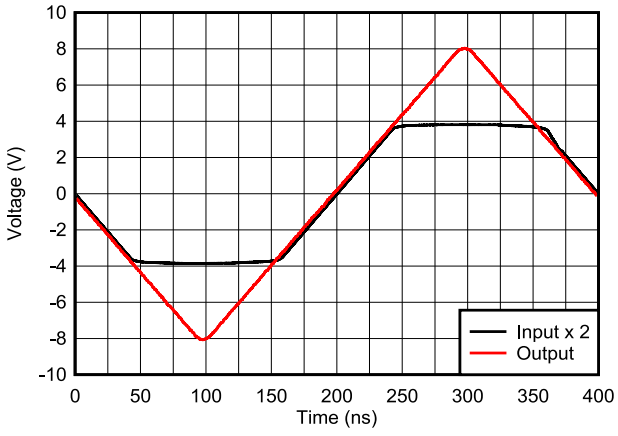
f = 5 MHz V_{OUT} = 2 V_{PP} R_L = 200 Ω

Figure 6-16. Harmonic Distortion vs Inverting Gain



f = 10 MHz V_{OUT} = 1 V_{PP}

Figure 6-17. Harmonic Distortion vs Supply Voltage



G = 2 V/V

Figure 6-18. Noninverting Output Overdrive Recovery

6.6 Typical Characteristics (continued)

at $T_A \cong 25°C$, $V_S = \pm 5$ V, G = 1 V/V, $R_F = 0\ \Omega$, $R_F = 250\ \Omega$ for other gains, $R_L = 100\ \Omega$, and input and output referenced to mid-supply (unless otherwise noted)

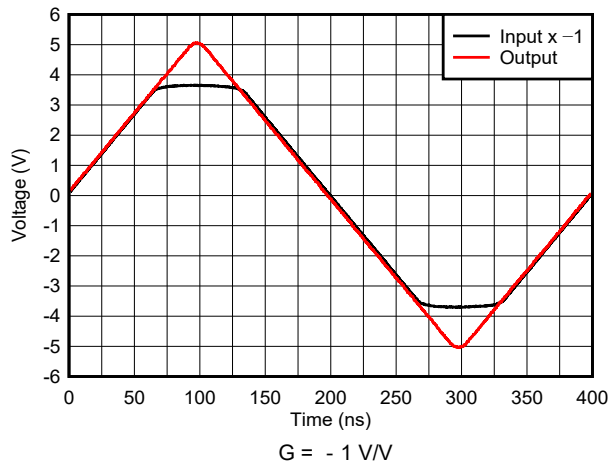


Figure 6-19. Inverting Output Overdrive Recovery

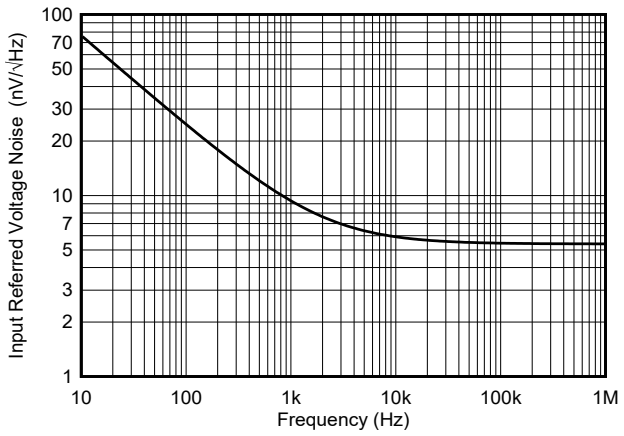


Figure 6-20. Voltage Noise Density vs Frequency

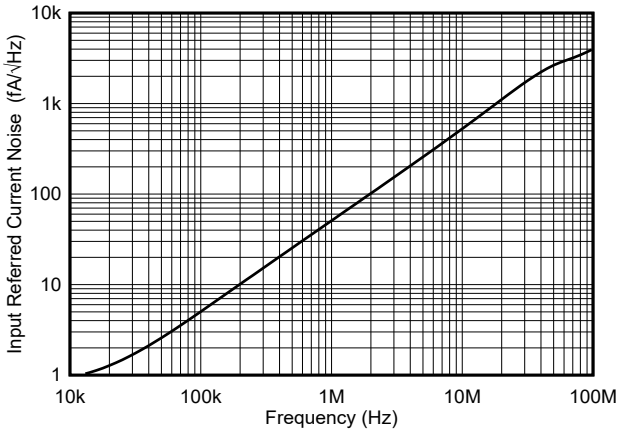


Figure 6-21. Current Noise Density vs Frequency

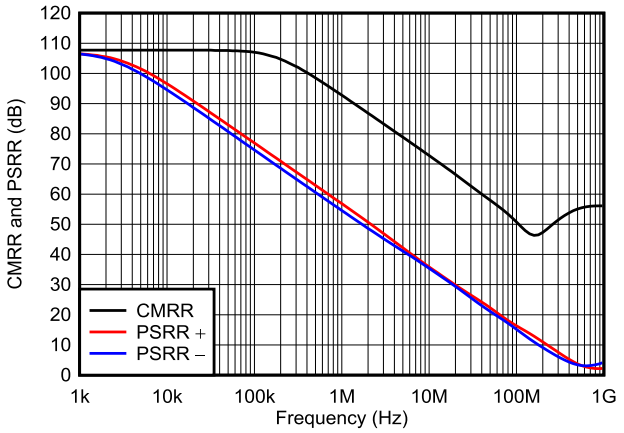


Figure 6-22. Common-Mode and Power-Supply Rejection Ratio vs Frequency

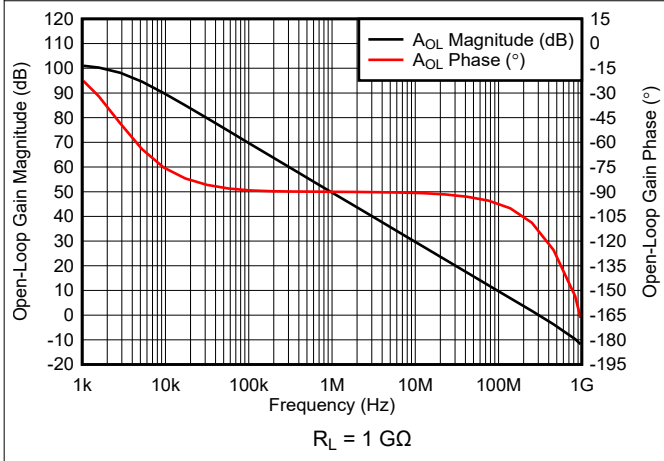


Figure 6-23. Open-Loop Gain Magnitude and Phase vs Frequency

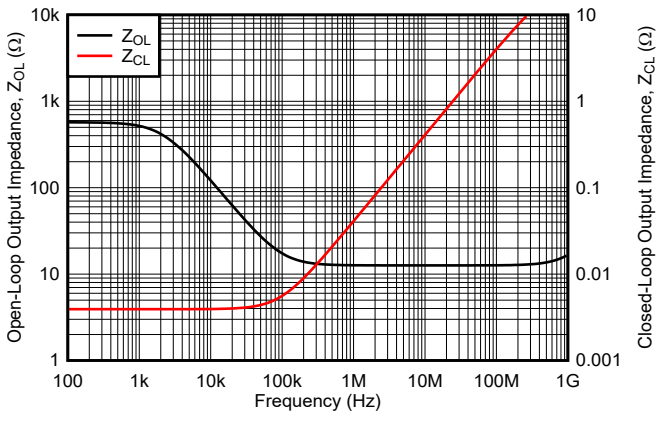


Figure 6-24. Open-Loop and Closed-Loop Output Impedance vs Frequency

6.6 Typical Characteristics (continued)

at T_A ≅ 25°C , V_S = ±5 V, G = 1 V/V, R_F = 0 Ω, R_F = 250 Ω for other gains, R_L = 100 Ω, and input and output referenced to mid-supply (unless otherwise noted)

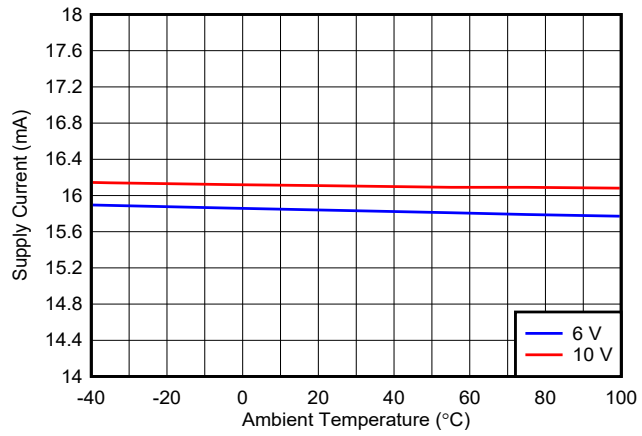


Figure 6-25. Quiescent Current Over Temperature

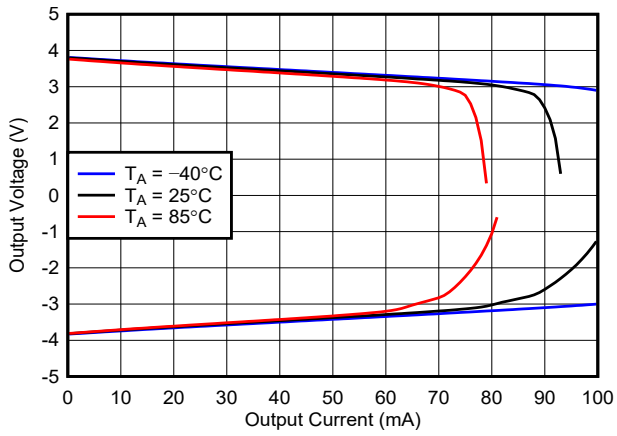
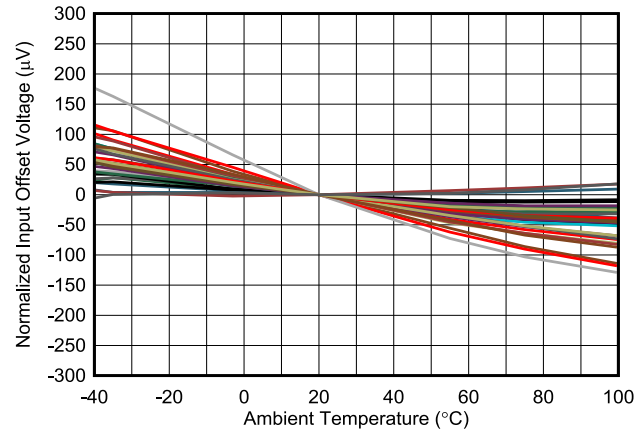
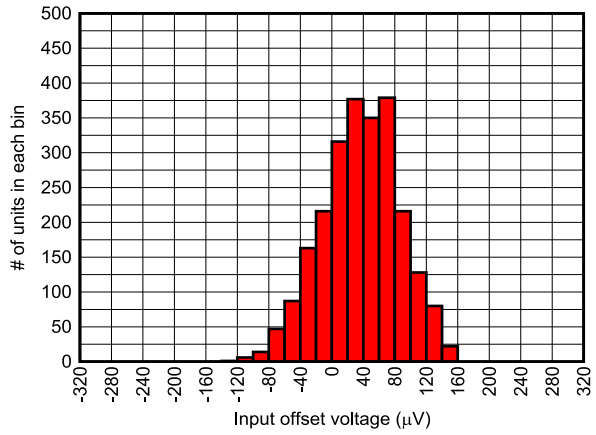


Figure 6-26. Output Voltage vs Output Current Over Temperature



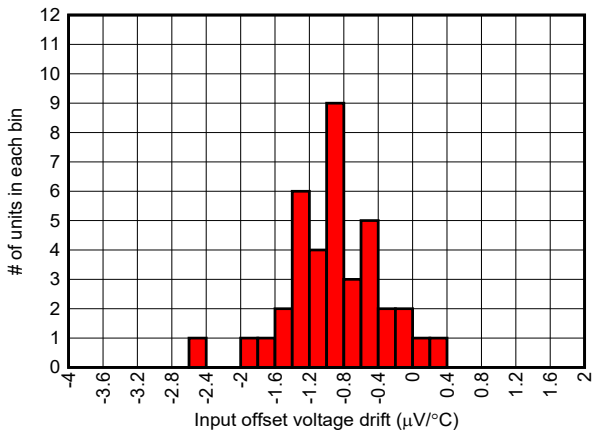
33 units, delta from 25°C

Figure 6-27. Input Offset Voltage vs Temperature



2400 units, µ = 37 µV, σ = 49 µV

Figure 6-28. Input Offset Voltage Histogram



38 units, µ = - 0.9 µV/°C, σ = 0.55 µV/°C

Figure 6-29. Input Offset Voltage Drift Histogram

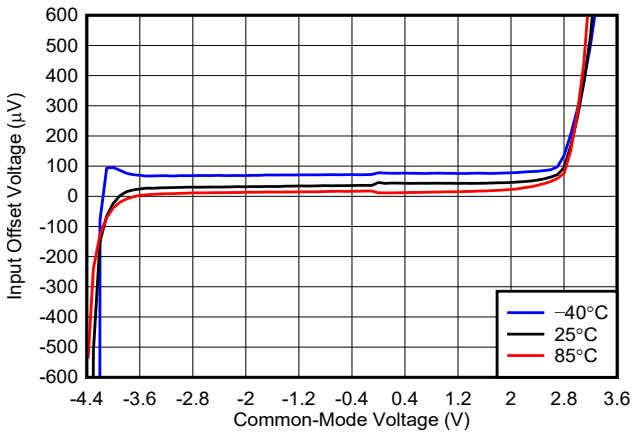


Figure 6-30. Input Offset Voltage vs Common-Mode Voltage Over Temperature

6.6 Typical Characteristics (continued)

at T_A ≅ 25°C , V_S = ±5 V, G = 1 V/V, R_F = 0 Ω, R_F = 250 Ω for other gains, R_L = 100 Ω, and input and output referenced to mid-supply (unless otherwise noted)

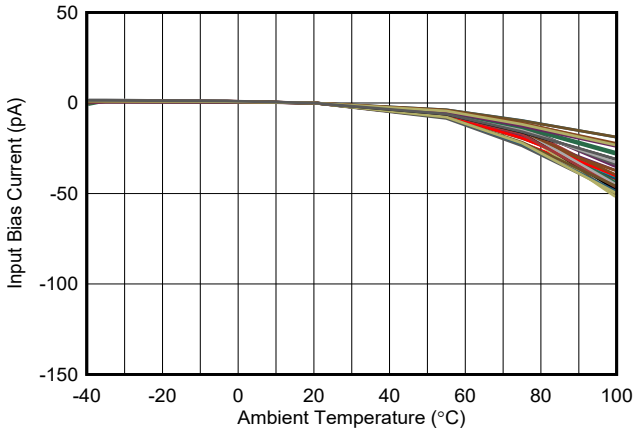


Figure 6-31. Input Bias Current vs Temperature

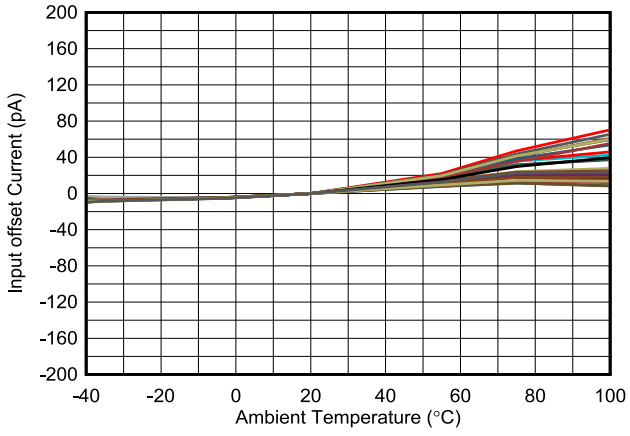


Figure 6-32. Input Offset Current vs Temperature

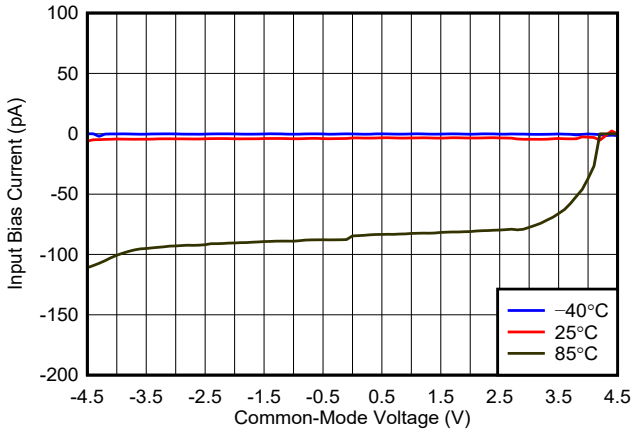


Figure 6-33. Input Bias Current vs Common-Mode Voltage Over Temperature

7 Detailed Description

7.1 Overview

The OPA814 is a high-voltage, unity-gain-stable, 250-MHz gain bandwidth product (GBWP), voltage-feedback operational amplifier (op amp) featuring a 5.3-nV/√Hz, low-noise JFET input stage. The low offset voltage (250 µV, maximum), offset voltage drift (3.5 µV/°C, maximum), and unity gain bandwidth of 600 MHz makes this device an excellent choice for high input impedance, high-speed data acquisition front-ends. The high-voltage capability combined with the 750-V/µs slew rate enables applications needing wide output swings (9 V_{PP} at V_S = 12 V) for high-frequency signals such as those often found in medical instrumentation, optical front-ends, test, and measurement applications. The low-noise JFET input with picoamperes of bias current makes this device attractive in high-gain TIA applications, and in test and measurement front-ends.

The OPA814 is built using TI's proprietary high-voltage, high-speed, complementary bipolar SiGe process.

7.2 Functional Block Diagram

The OPA814 is a conventional voltage-feedback op amp with two high-impedance inputs and a low-impedance output. Figure 7-1 and Figure 7-2 show two standard amplifier configuration examples that are supported for this device. The reference voltage (V_{REF}) level shifts the dc operating point for each configuration, which is typically set to mid-supply in single-supply operation. V_{REF} is typically set to ground in split-supply applications.

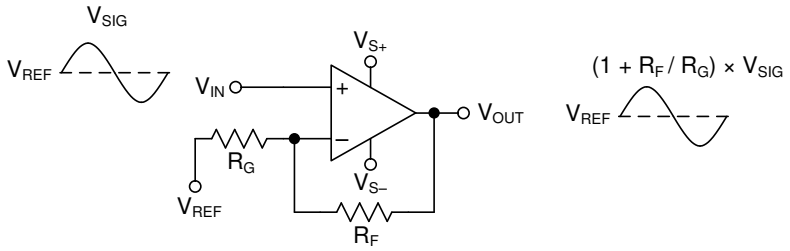


Figure 7-1. Noninverting Amplifier

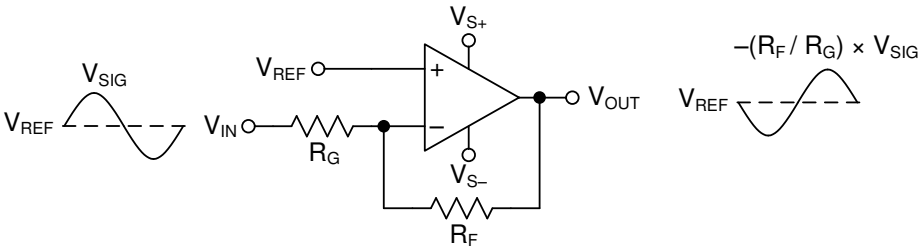


Figure 7-2. Inverting Amplifier

7.3 Feature Description

7.3.1 Input and ESD Protection

The OPA814 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the *Absolute Maximum Ratings*. As Figure 7-3 shows, all device pins are protected with internal ESD protection diodes to the power supplies.

The diodes provide moderate protection to input overdrive voltages beyond the supplies as well. The protection diodes can typically support a 10-mA continuous current. Where higher currents are possible (for example, in systems with ±12-V power supplies driving into the OPA814), add current limiting series resistors in series with the two inputs to limit the current. Keep these resistor values as low as possible because high values degrade both noise performance and frequency response. There are no back-to-back ESD diodes between V_{IN+} and $V_{IN–}$. As a result, the differential input voltage between V_{IN+} and $V_{IN–}$ is entirely absorbed by the V_{GS} of the input JFET differential pair and must not exceed the voltage ratings shown in the *Absolute Maximum Ratings*.

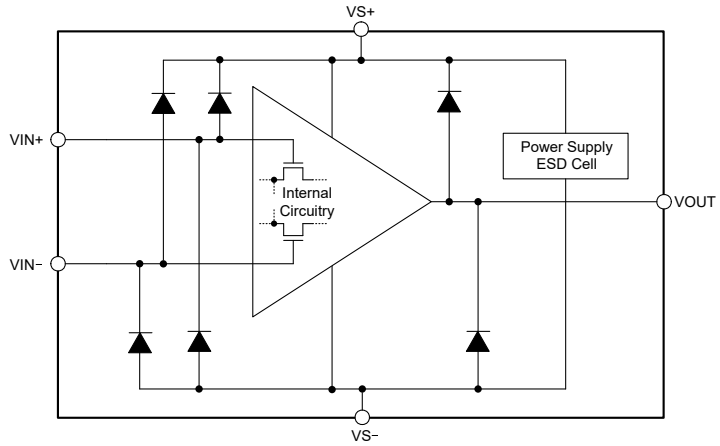


Figure 7-3. Internal ESD Protection

7.3.2 FET-Input Architecture With Wide Gain-Bandwidth Product

Figure 7-4 shows the open-loop gain and phase response of the OPA814. The GBWP of an op amp is measured in the 20-dB/decade constant slope region of the A_{OL} magnitude plot. The open-loop gain of 60 dB for the OPA814 is along this 20-dB/decade slope, and the corresponding frequency intercept is at 250 kHz. Converting 60 dB to linear units (1000 V/V) and multiplying the open-loop gain with the 250-kHz frequency intercept gives the GBWP of OPA814 as 250 MHz. As is inferred from the A_{OL} Bode plot, the second pole in the A_{OL} response occurs after A_{OL} magnitude drops to less than 0 dB (1 V/V). This occurrence results in a phase change of less than 180° at 0-dB A_{OL}, indicating that the amplifier is stable in a gain of 1 V/V. Amplifiers such as the OPA814 that are JFET input, low noise, and unity-gain stable can be used as high input-impedance buffers and gain stages with minimal degradation in SNR. The OPA814 has 600 MHz of SSBW in gain of 1-V/V configuration with approximately 65° of phase margin.

The low input offset voltage and offset voltage drift of the OPA814 make the device an excellent amplifier for high-precision, high input-impedance, wideband data-acquisition-system front-ends. Figure 8-2 shows that the system benefits from the low-noise JFET input stage with picoamperes of input bias current to achieve higher precision at the 1-MΩ input impedance setting, and higher SNR at the 50-Ω input impedance setting simultaneously in a typical data-acquisition front-end circuit.

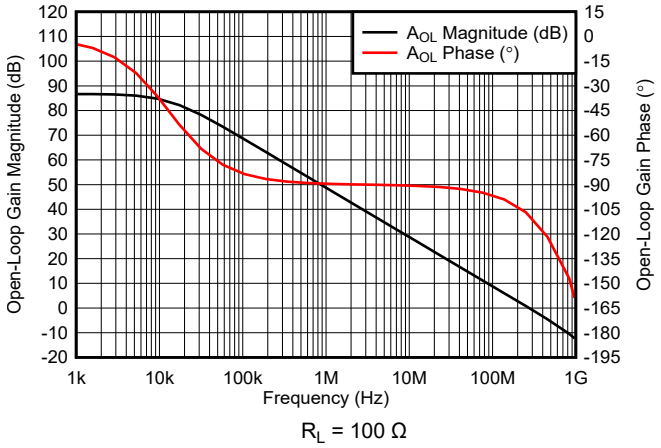


Figure 7-4. Open-Loop Gain Magnitude and Phase vs Frequency

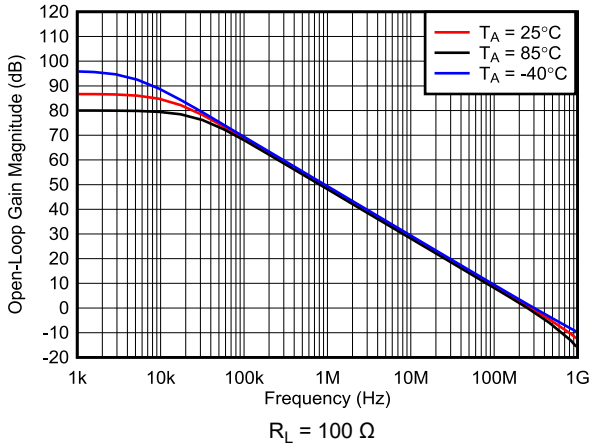


Figure 7-5. Open-Loop Gain Magnitude vs Temperature

7.4 Device Functional Modes

The OPA814 has a single functional mode and is operational when the power-supply voltage is greater than 6 V. The maximum power supply voltage for the OPA814 is 12.6 V (±6.3 V). The OPA814 can be operated on both single and dual supplies.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Wideband, High-Input Impedance DAQ Front-End

The OPA814 features a unique combination of high GBWP, low-input voltage noise, and the dc precision of a trimmed JFET-input stage to provide a high input impedance for a voltage-feedback amplifier. Figure 8-2 shows how the very high GBWP of 250 MHz and high large signal bandwidth of 200 MHz are used to either deliver wide signal bandwidths at high gains or to extend the achievable bandwidth or gain in typical high-speed, high-input-impedance data-acquisition front-end applications. To achieve the full performance of the OPA814, careful attention to the printed circuit board (PCB) layout and component selection is required, as discussed in the following sections of this data sheet. The OPA814 also features a wider supply range, thereby enabling a wider common-mode input range to support higher input-signal swings.

Figure 8-1 shows the noninverting gain of a +2-V/V circuit used as the basis for most of the *Typical Characteristics*. Most of the curves are characterized using signal sources with 50-Ω driving impedance, and with measurement equipment presenting a 50-Ω load impedance. As Figure 8-1 shows, the 49.9-Ω shunt resistor at the V_{IN} terminal matches the source impedance of the test generator, while the 49.9-Ω series resistor at the V_O terminal provides a matching resistor for the measurement equipment load. Generally, data-sheet voltage-swing specifications are at the output pin (V_O in Figure 8-1); whereas, output power specifications are at the matched 50-Ω load. Figure 8-1 shows that the total 100-Ω load at the output combined with the 500-Ω total feedback network load presents the OPA814 with an effective output load of 83.3 Ω for the circuit.

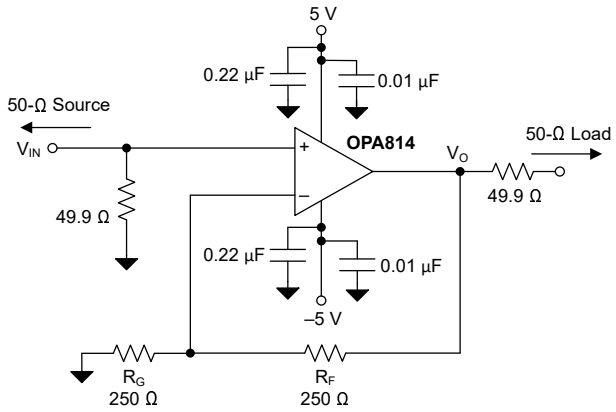


Figure 8-1. Noninverting G = +2 V/V Configuration and Test Circuit

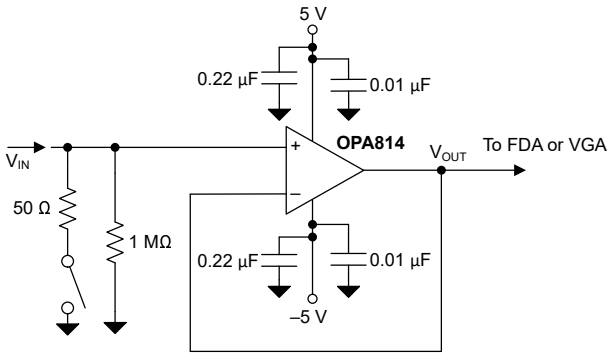


Figure 8-2. High Input Impedance DAQ Front-End

Voltage-feedback operational amplifiers, unlike current-feedback amplifiers, use a wide range of resistor values to set the gain. As Figure 8-1 shows, the parallel combination of R_F || R_G must always be kept to a lower value to retain a controlled frequency response for the noninverting voltage amplifier. In the noninverting configuration, the parallel combination of R_F || R_G form a pole with the parasitic input capacitance at the inverting node of the OPA814 (including layout parasitic capacitance). For best performance, this pole must be at a frequency greater than the closed-loop bandwidth for the OPA814.

8.1.2 Wideband, Transimpedance Design Using the OPA814

The OPA814 design is optimized for wideband, low-noise transimpedance applications with high GBWP, low input voltage, low current noise, and low input capacitance. The high-voltage capability allows greater flexibility of supply voltages along with wider output voltage swings. Figure 8-3 shows an example circuit of a typical photodiode amplifier circuit. Figure 8-3 shows that the photodiode is generally reverse biased in a TIA application, so that the photodiode current in the circuit flows into the op-amp feedback path. This polarity of the current results in an output voltage that reduces from V_{REF} with increasing photodiode current. In this type of configuration, and depending on the application needs, V_{REF} can be biased closer to V_{S+} to achieve the desired output swing. Consider the common-mode input range when V_{REF} bias is used so that the common-mode input voltage stays within the valid range of the OPA814.

The key design elements that determine the closed-loop bandwidth, $f_{–3dB}$, of the circuit are as follows:

1. The op amp GBWP
2. The transimpedance gain, R_F
3. The total input capacitance, C_{TOT}, that includes photodiode capacitance, input capacitance of the amplifier (common-mode and differential capacitance), and PCB parasitic capacitance

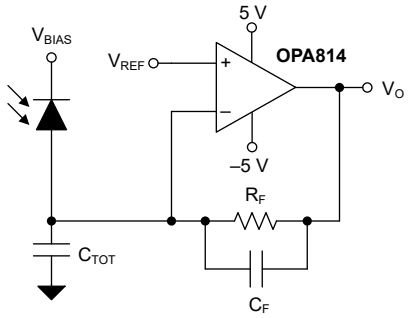


Figure 8-3. Wideband, Low-Noise, Transimpedance Amplifier

Equation 1 shows the relationship between the three key design elements for a Butterworth response.

$$f_{-3dB} = \sqrt{\frac{GBWP}{2 \times \pi \times R_F \times C_{TOT}}} \quad (1)$$

The feedback resistance (R_F) and the total input capacitance (C_{TOT}) form a zero in the noise gain, and results in instability if left uncompensated. To counteract the effect of the zero, a pole is inserted in the noise gain by adding the feedback capacitor (C_F). The *Transimpedance Considerations for High-Speed Amplifiers* application report discusses theories and equations that show how to compensate a transimpedance amplifier for a particular gain and input capacitance. The bandwidth and compensation equations from the application report are available in a Microsoft Excel™ calculator. A link to the calculator is provided in *What You Need To Know About Transimpedance Amplifiers – Part 1*. The details of maximizing the dynamic range of TIA front-ends are provided in the *Maximizing the Dynamic Range of Analog TIA Front-End* application note.

8.2 Typical Application

8.2.1 High-Input-Impedance, 180-MHz, Digitizer Front-End Amplifier

The OPA814 wide, large-signal bandwidth and high-slew rate along with high-input impedance make this device an excellent choice for data-acquisition systems. The trimmed dc precision of the OPA814 enables the device to be used directly as a front-end amplifier where low offset and offset voltage drift are required.

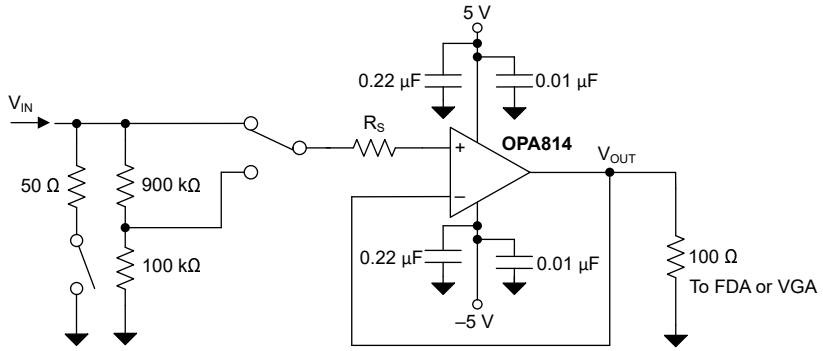


Figure 8-4. High-Input-Impedance, 180-MHz, Digitizer Front-End Amplifier

8.2.1.1 Design Requirements

Table 8-1 lists the design requirements for a high-input-impedance, 180-MHz, digitizer front-end amplifier.

Table 8-1. Design Requirements

PARAMETER		VALUE
Input impedance		1 MΩ or 50 Ω
Input range	1-MΩ setting	20 V_{PP}
	50-Ω setting	2 V_{PP}
Offset drift		3.5 µV/°C, maximum
Noise at highest resolution (50-Ω Input)		90 μV_{RMS}

8.2.1.2 Detailed Design Procedure

The following bullets list the considerations for this design example:

- **Input Impedance**: The JFET-input stage of the OPA814 offers gigaohms of input impedance, and therefore enables the front-end to be terminated with a 1-MΩ resistor while achieving excellent precision. A 50-Ω resistance can also be switched in, offering matched termination for high-frequency signals. Thus, the OPA814 enables the designer to use both 1-MΩ and 50-Ω termination in the same signal chain.
- **Noise**: The total noise of the front-end amplifier is a function of the voltage and current noise of the OPA814, input termination, and the resistors thermal noise. However, in 50-Ω mode, the dominant noise source is contributed by the voltage noise of the OPA814 due to the presence of voltage noise across the complete bandwidth. Therefore, the total RMS noise of the front-end amplifier is approximately equal to the voltage noise of the OPA814 over 180 MHz.

  The specified input-referred voltage noise of the OPA814 is 5.3 nV/√Hz; see also Section 6.5. The total integrated RMS noise at the input in a bandwidth of 180 MHz is given by the following equation:

$$E_{NRMS} = 5.3\ nV/\sqrt{Hz} \times \sqrt{(180\ MHz \times 1.57)} = 90\ \mu V_{RMS} \quad (2)$$

  The brickwall correction factor of 1.57 is applied, assuming the bandwidth is limited to 180 MHz with a single-pole RC filter before digitizing the signal with the ADC. Detailed calculations are found at TI Precision Labs – Op Amp Noise: Spectral Density.

- **Optimizing Overshoot**: The OPA814 features an internal slew-boost circuit to deliver fast rise-time in applications that require high slew rates, such as when configured as a transimpedance amplifier. For applications where overshoot must be limited, limit the input slew rates by introducing a series resistance (R_S); see also Figure 8-4. Resistor R_S forms a low-pass filter with an input capacitance of approximately 2.5 pF at the noninverting pin of the OPA814, thus limiting the input slew rate to the amplifier. Figure 8-5 shows how limiting the input slew rate to the amplifier results in good overshoot performance. Figure 8-6 shows how this configuration achieves a small-signal and large-signal bandwidth of 180 MHz.

8.2.1.3 Application Curves

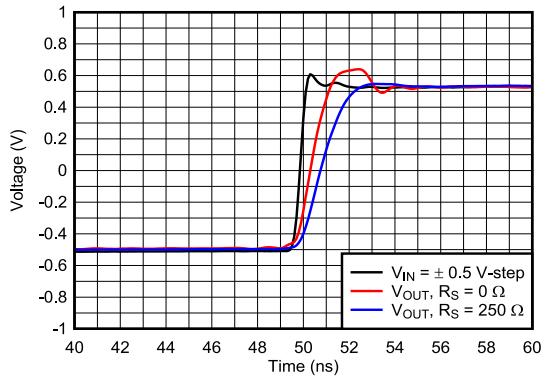


Figure 8-5. Step Response of Digitizer Front-End

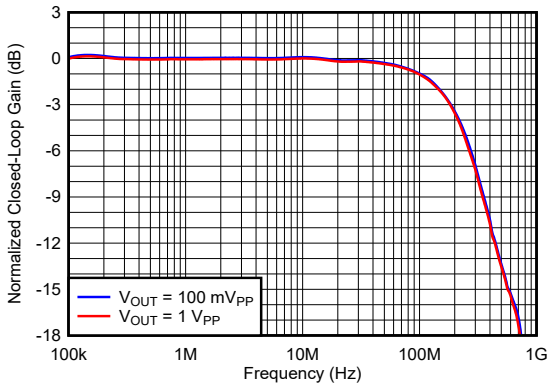


Figure 8-6. Frequency Response for R_S = 250 Ω

8.3 Power Supply Recommendations

The OPA814 is intended to operate on supplies ranging from 6 V to 12.6 V. The OPA814 supports single-supply, split, balanced, and unbalanced bipolar supplies. When operating at supplies less than 8 V, consider the input common-mode range of the amplifier. Under these supply conditions, the common-mode must be biased appropriately for linear operation. Therefore, the limit to lower supply-voltage operation is the usable input voltage range for the JFET-input stage.

8.4 Layout

8.4.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier like the OPA814 requires careful attention to board layout parasitics and external component types. Recommendations that optimize performance include the following:

1. **Minimize parasitic capacitance to any ac ground for all of the signal I/O pins.** Parasitic capacitance on the output and inverting input pins can cause instability. On the noninverting input, parasitic capacitance can react with the source impedance to cause unintentional band-limiting. Ground and power metal planes act as one of the plates of a capacitor, while the signal trace metal acts as the other separated by PCB dielectric. To reduce this unwanted capacitance, minimize the routing of the feedback network. A plane cutout around and underneath the inverting input pin on all ground and power planes is recommended. Otherwise, make sure that ground and power planes are unbroken elsewhere on the board.
2. **Minimize the distance (less than 0.25 inches) from the power-supply pins to high-frequency decoupling capacitors.** Use high-quality, 100-pF to 0.1-µF, C0G- and NPO-type decoupling capacitors. These capacitors must have voltage ratings at least three times greater than the amplifiers maximum power supplies to provide a low-impedance path to the amplifiers power-supply pins across the amplifiers gain bandwidth specification. At the device pins, do not allow the ground and power plane layout to be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Larger (2.2-µF to 6.8-µF) decoupling capacitors, effective at lower frequencies, must be used on the supply pins. These larger capacitors can be placed further from the device and shared among several devices in the same area of the PCB.
3. **Careful selection and placement of external components preserves the high-frequency performance of the OPA814.** Use low-reactance resistors. Small form-factor, surface-mount resistors work best and allow a tighter overall layout. The output pin and inverting input pin are the most sensitive to parasitic capacitance; therefore, always position the feedback and series output resistor, if any, as close as possible to the inverting input and the output pin, respectively.

   Place other network components, such as noninverting input termination resistors, close to the package. Even with a low parasitic capacitance at the noninverting input, high external resistor values can create significant time constants that can degrade performance. When the OPA814 is configured as a conventional voltage amplifier, keep the resistor values as low as possible and consistent with the load driving considerations. Decreasing the resistor values keeps the resistor noise terms low and minimizes the effect of the parasitic capacitance. However, lower resistor values increase the dynamic power consumption because R_F and R_G become part of the output load network of the amplifier.

8.4.1.1 Thermal Considerations

The OPA814 does not require heat sinks or airflow in most applications. The maximum allowed junction temperature sets the maximum allowed internal power dissipation, as described in the following paragraph. Do not allow the maximum junction temperature to exceed 150°C.

The operating junction temperature (T_J) is given by $T_A + P_D \times R_{\theta JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}), and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load, but for a grounded resistive load, P_{DL} is at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for balanced, bipolar supplies). Under this condition, $P_{DL} = V_S{}^2 / (4 \times R_L)$, where R_L includes feedback network loading.

Be aware that the power in the output stage, and not into the load, determines internal power dissipation.

As a worst-case example, compute the maximum T_J using OPA814 in the circuit of Figure 8-1 operating at the maximum specified ambient temperature of +85°C and driving a grounded 100-Ω load.

$$P_D = 10\ V \times 16\ mA + 5^2 / (4 \times (100\ \Omega \parallel 500\ \Omega)) \cong 235\ mW \quad (3)$$

$$\text{Maximum } T_J = +85°C + (0.235\ W \times 122.9°C/W) = 113.9°C. \quad (4)$$

All actual applications operate at a lower internal power and junction temperature.

8.4.2 Layout Example

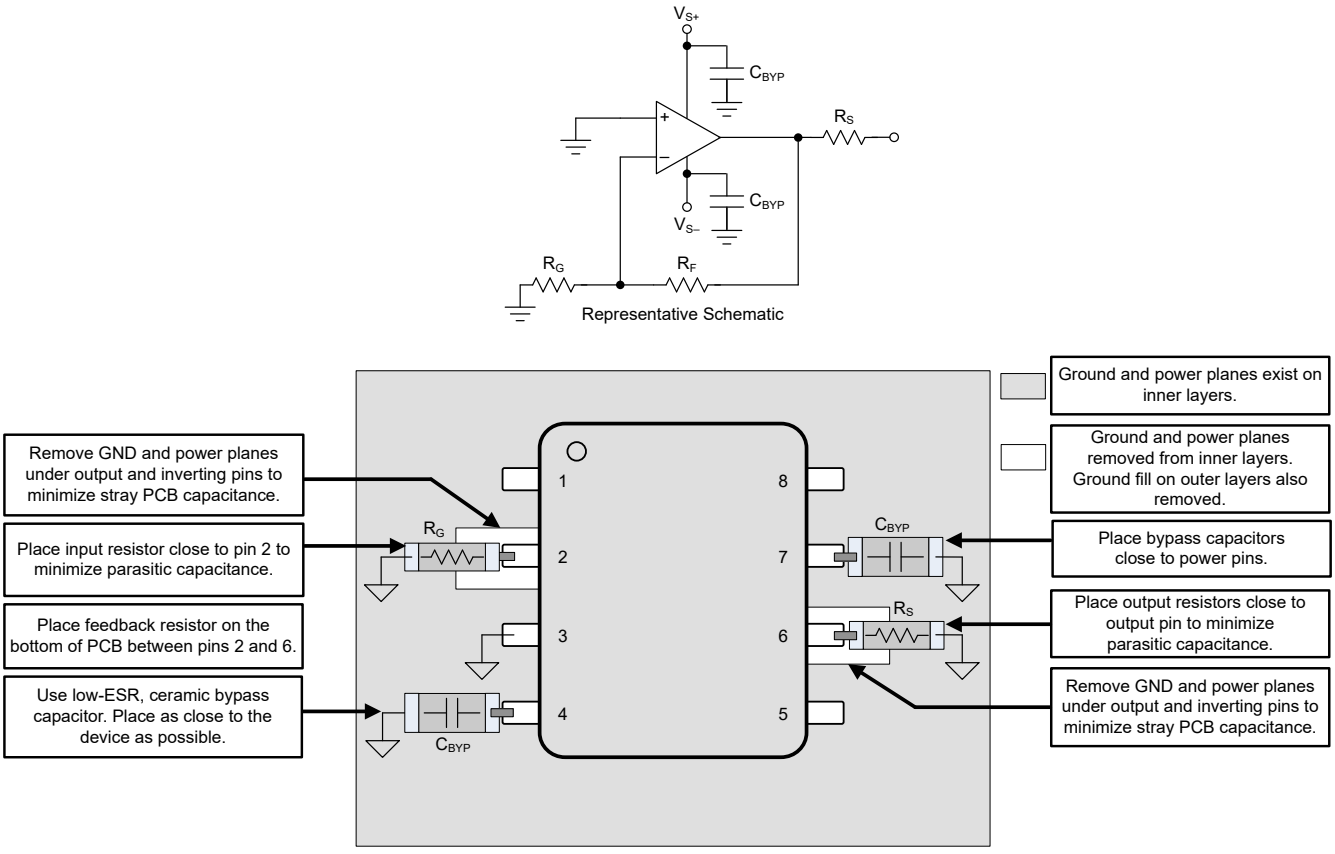


Figure 8-7. Layout Recommendation

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

- Texas Instruments, *Wide Bandwidth Optical Front-end Reference Design*

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Transimpedance Considerations for High-Speed Amplifiers* application report
- Texas Instruments, *Optical Front-End System Reference Design*
- Texas Instruments, *Maximizing the Dynamic Range of Analog TIA Front-End* technical brief
- Texas Instruments, *What You Need To Know About Transimpedance Amplifiers – Part 1*
- Texas Instruments, *What You Need To Know About Transimpedance Amplifiers – Part 2*
- Texas Instruments, *Training Video: How to Design Transimpedance Amplifier Circuits*
- Texas Instruments, *Training Video: High-Speed Transimpedance Amplifier Design Flow*

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

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9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (April 2023) to Revision A (November 2023)	Page
• Changed document status from mixed status to production data	1
• Changed DBV package status from preview to active	1
• Updated *Package Information* table to show package size instead of body size	1
• Added specifications for offset voltage, output swing and PSRR for SOT-23 package in the *Electrical Characteristics* table	5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA814DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	OP814	Samples
OPA814DR	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OPA814	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

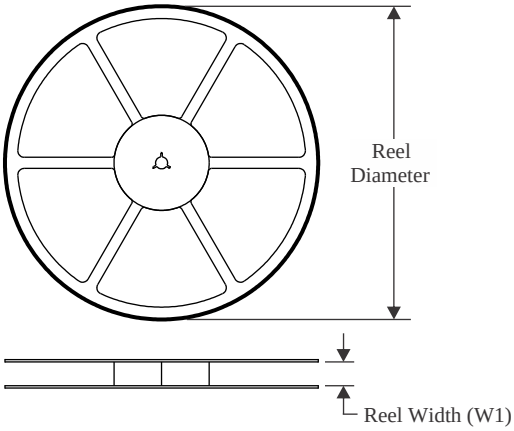
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

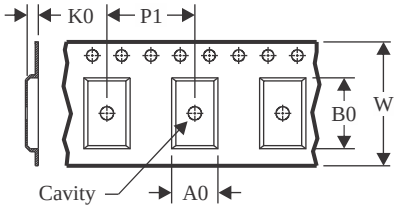
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

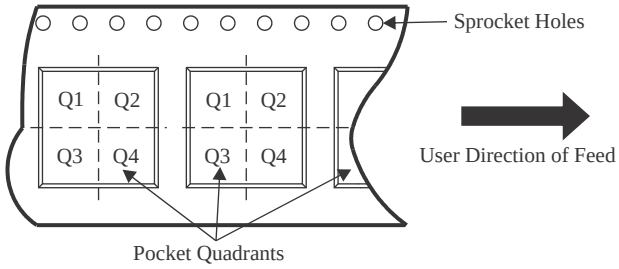


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

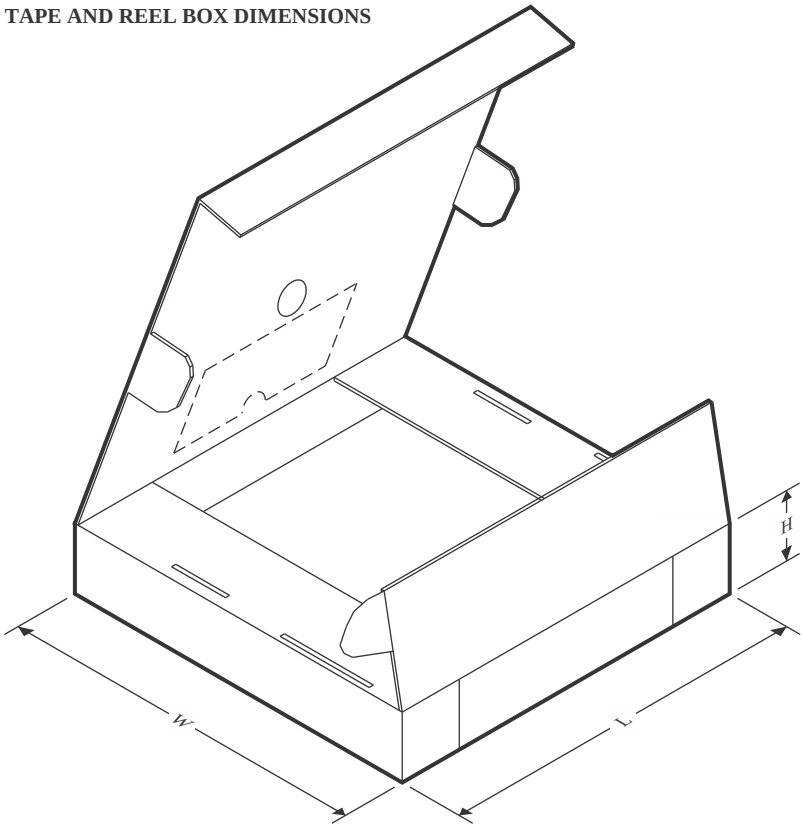
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

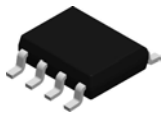
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA814DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA814DR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA814DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
OPA814DR	SOIC	D	8	3000	356.0	356.0	35.0

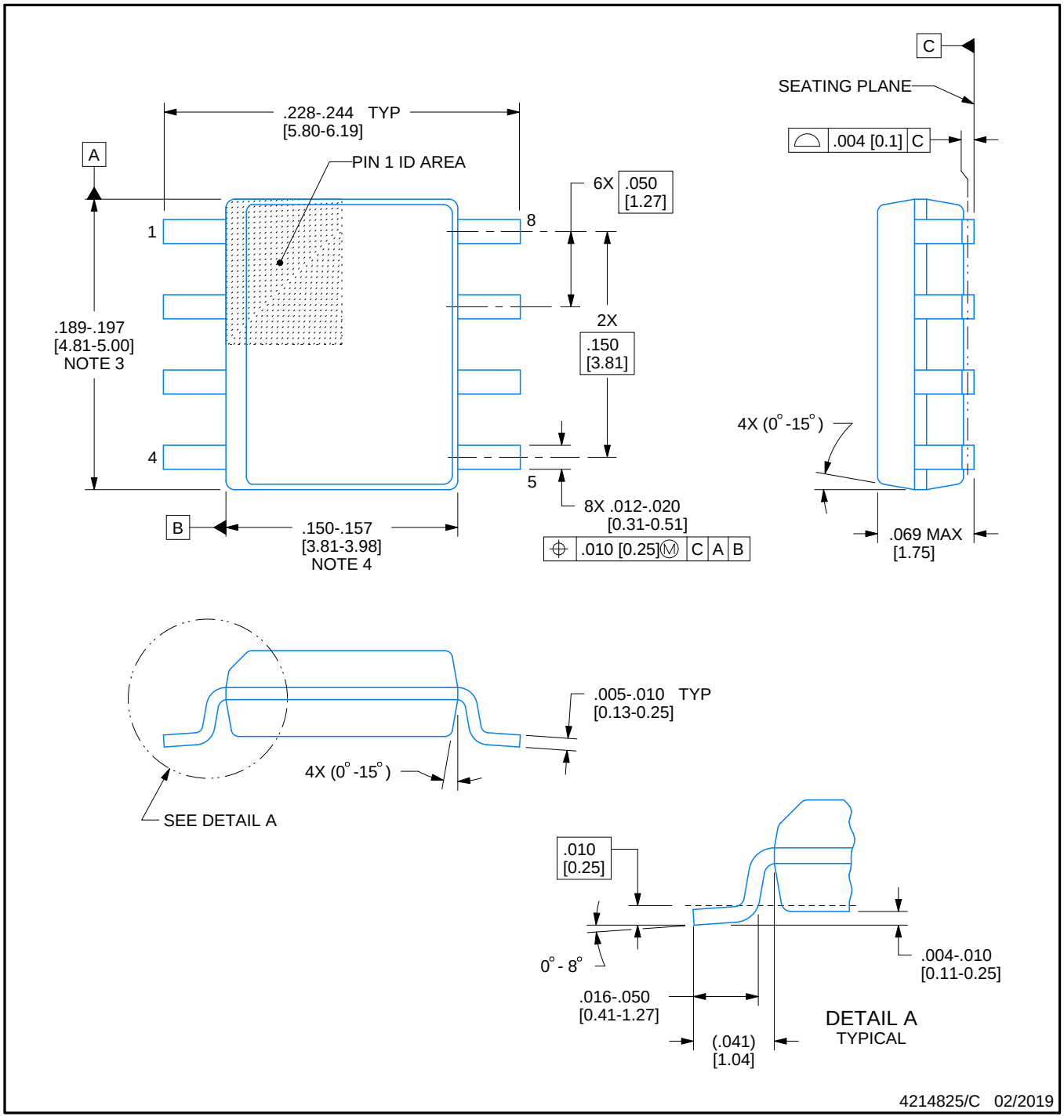


PACKAGE OUTLINE

D0008A

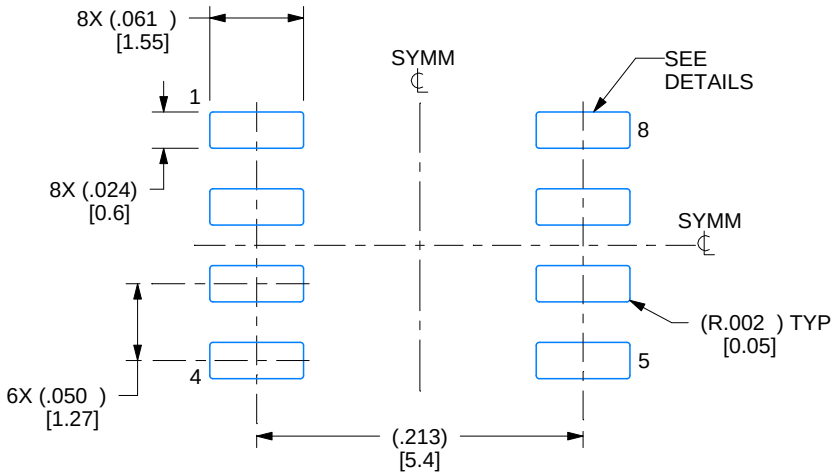
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

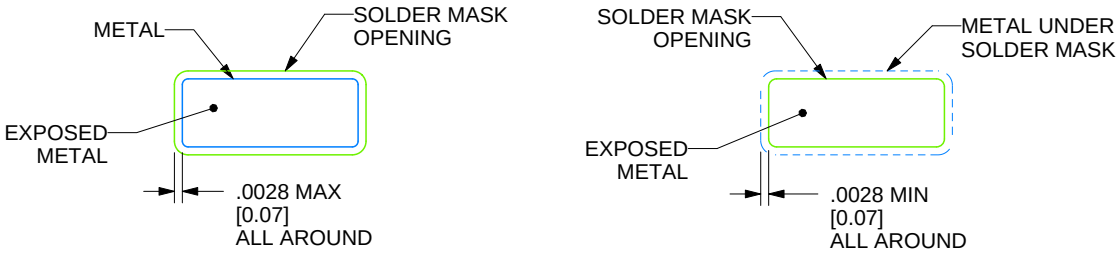


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

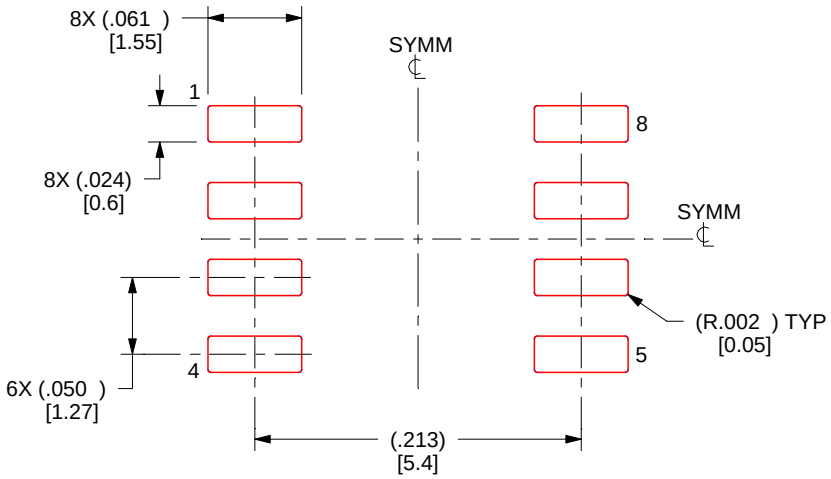
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

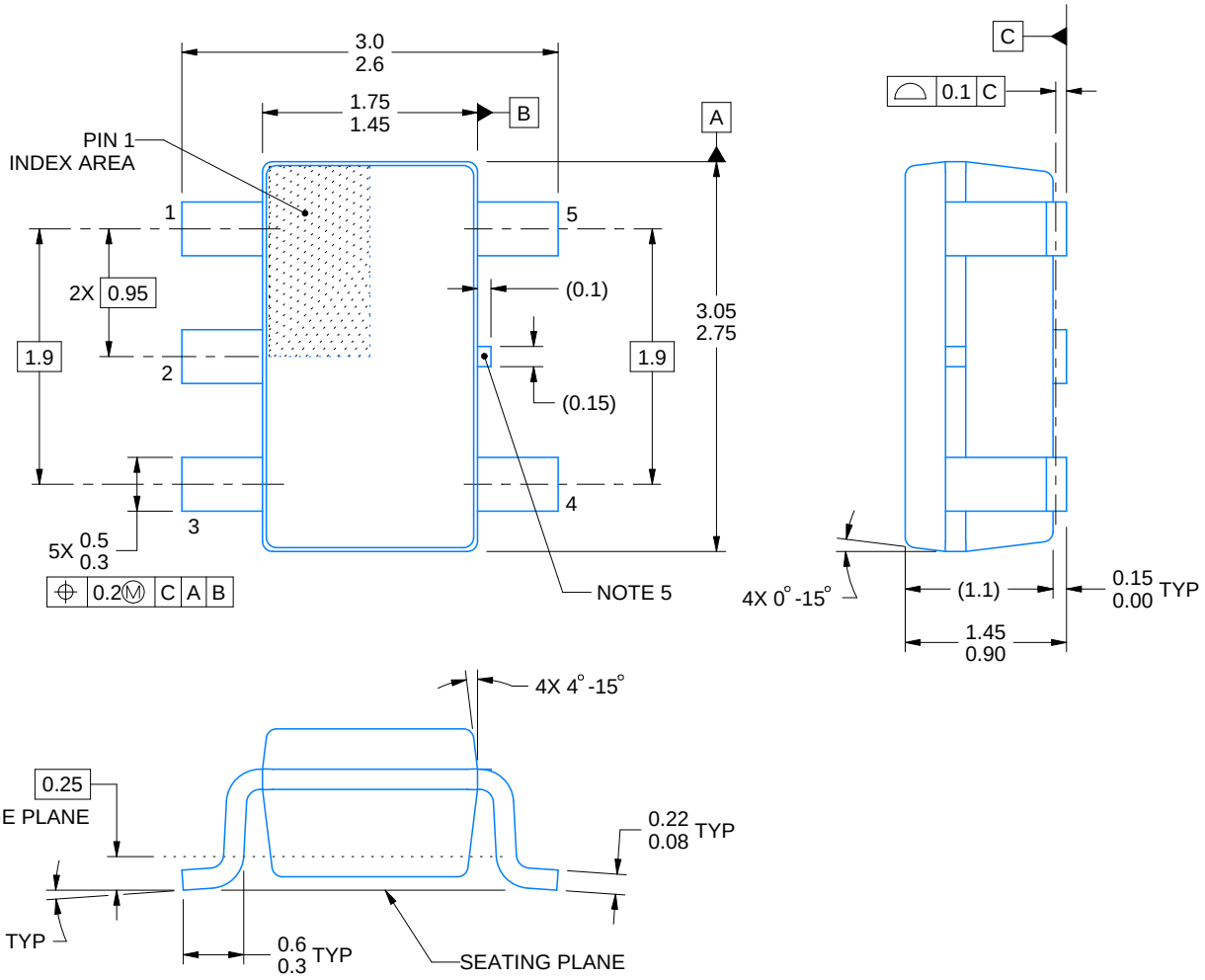
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

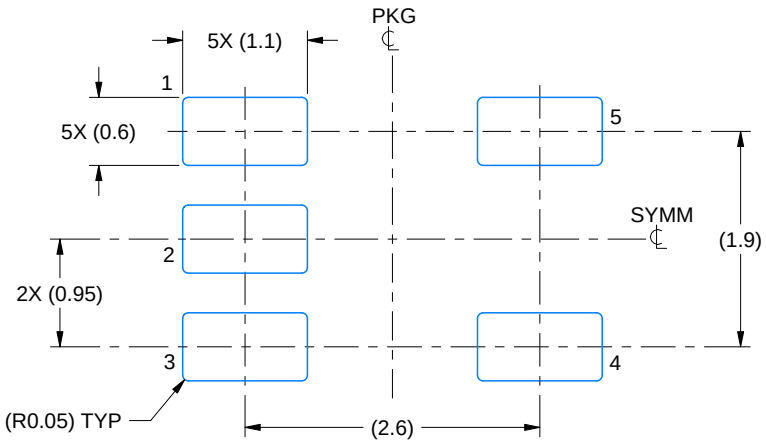
SMALL OUTLINE TRANSISTOR



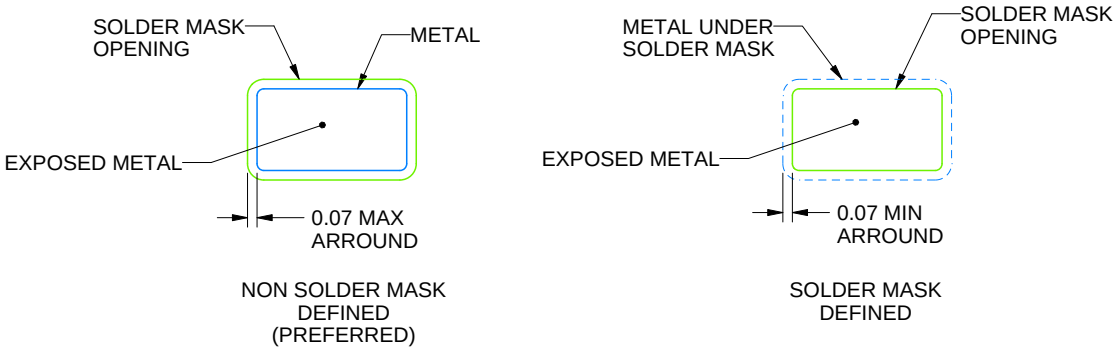
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

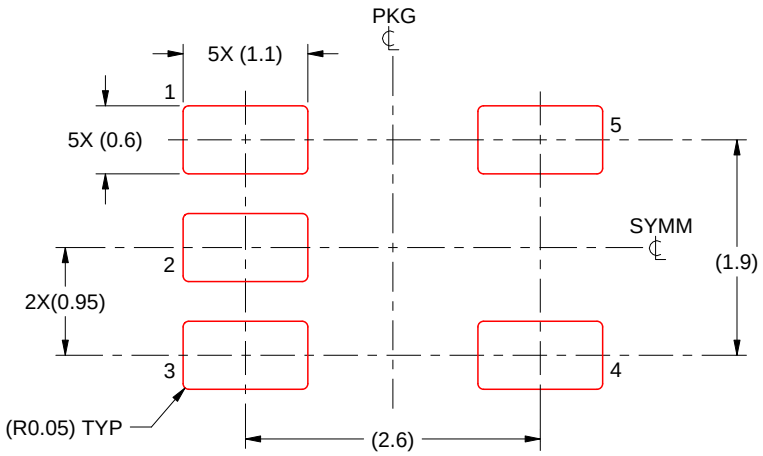


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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