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FEATURES

- **Compatible with Standards for Noise and Crosstalk in Telephony Systems**
- **Pin Compatible with DG508, HI-508A, LF11508**
- **JFET Switches Rather Than CMOS**
- **Low "ON" Resistance — 220Ω Typical**
- **Low Output Leakage Current — 100nA Max**
- **Digital Inputs Compatible with TTL and CMOS**
- **Input Overvoltage and Supply Loss Protected**

ORDERING INFORMATION†

R_{ON}	MODEL	TEMP RANGE
400Ω	MUX-88EQ	IND
520Ω	MUX-88FQ	IND

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages. For ordering information, see 1990/91 Data Book, Section 2.

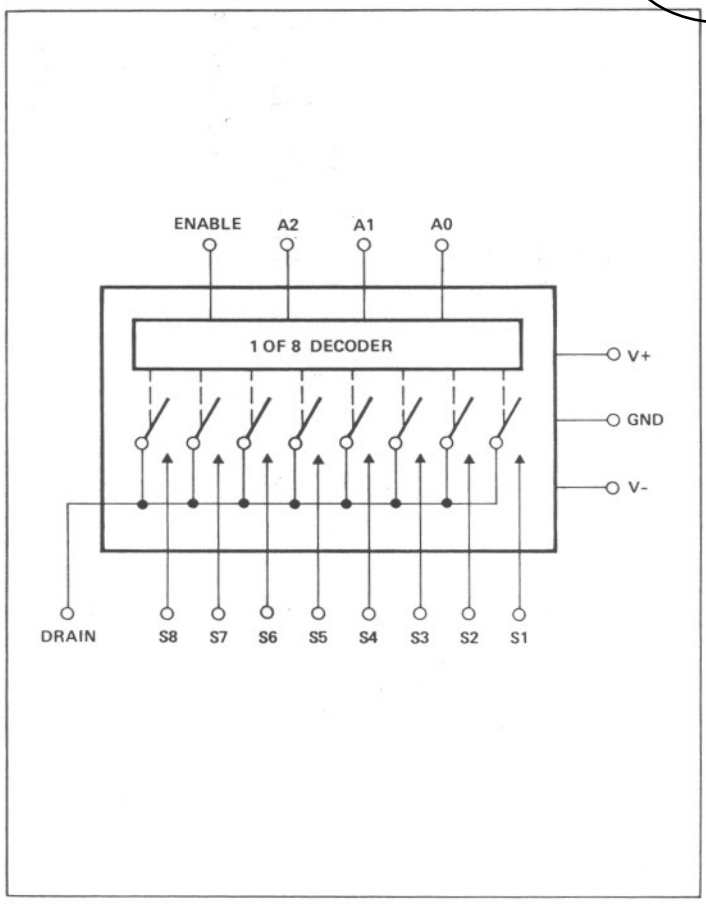
GENERAL DESCRIPTION

The MUX-88 is a monolithic eight-channel analog multiplexer ideally suited to shared-channel PCM CODEC systems. One-of-eight channels is selected upon the decoding of a 3 bit binary address. An enable input (E_n) disables all switches when logic low providing package select. All logic control inputs have true TTL input compatibility eliminating the need for pull-up resistors necessary for some CMOS equivalent products.

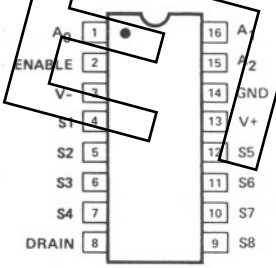
Fabricated with Precision Monolithics' high performance Bipolar-JFET technology, this device offers low "ON" resistance, low leakage, fast settling time and excellent crosstalk isolation (98dB @ 20kHz). These characteristics make this device suitable for meeting system level communication requirements in shared-channel PCM CODECs.

Additional ruggedization results from built-in overvoltage, supply loss, and latch-up free circuit characteristics.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



TOP VIEW
16-PIN HERMETIC DUAL-IN-LINE
(Q-Suffix)

TRUTH TABLE

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted)

Operating Temperature Range
MUX-88EQ, FQ ..... –25°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
V+ Supply to V– Supply 36V
V+ Supply to Ground 18V
Logic Input Voltage (Note 5) ..... (V– or –4V) to V+
Analog Input Voltage ..... V– Supply –20V to V+ Supply +20V

Maximum Current Through Any Pin 25mA

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
16-Pin Hermetic DIP (Z)	100	16	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP package.

ELECTRICAL CHARACTERISTICS for V+ = −15V and −25°C ≤ T_A ≤ 85°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MUX-88E MIN	MUX-88E TYP	MUX-88E MAX	MUX-88F MIN	MUX-88F TYP	MUX-88F MAX	UNITS
"ON" Resistance	R_{ON}	V_S = 0V, I_S = 200μA	—	—	400	—	—	520	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	−10V ≤ V_S ≤ 10V, I_S = 200μA	—	1.5	—	—	4.5	—	%
R_{ON} Match Between Switches	$R_{ON\ Match}$	V_S = 0V, I_S = 200μA	—	25	—	—	30	—	Ω
Source Current (Switch "OFF")	$I_{S(OFF)}$	V_S = 10V, V_D = −10V, (Note 1)	—	—	10	—	—	10	nA
Drain Current (Switch "OFF")	$I_{D(OFF)}$	V_S = 10V, V_D = −10V, (Note 1)	—	—	100	—	—	100	nA
Leakage Current (Switch "ON")	$I_{D(ON)}$, $I_{S(ON)}$	V_D = 10V, (Note 1)	—	—	100	—	—	100	nA
Digital "1" Input Voltage	V_{INH}	(Note 5)	2	—	—	2	—	—	V
Digital "0" Input Voltage	V_{INL}	(Note 5)	—	—	0.8	—	—	0.8	V
Digital Input Current	I_{IN}	V_{IN} = 0.7V to +5V	—	—	20	—	—	20	μA
Digital "0" Enable Current	$I_{INL(EN)}$	V_{EN} = 0.7V	—	—	20	—	—	20	μA
Positive Supply Current	I+	All Digital Inputs Logic "0"	—	—	15	—	—	15	mA
Negative Supply Current	I−	All Digital Inputs Logic "0"	—	—	5	—	—	5	mA
Switching Time (t_{TRAN})	t_{PHL}	Figure 1, (Note 2)	—	1.8	2.1	—	2.2	2.5	μs
	t_{PLH}		—	1.3	1.6	—	1.7	2.0	
Output Settling Time	t_S	10V Step 0.10%	—	1.3	—	—	1.7	—	μs
		10V Step 0.05%	—	1.5	—	—	1.9	—	
		10V Step 0.02%	—	2.3	—	—	2.5	—	
Break-Before-Make Delay	t_{OPEN}		—	0.8	—	—	1.0	—	μs
Enable Delay "ON"	$t_{ON(EN)}$		—	1.0	—	—	1.2	—	μs
Enable Delay "OFF"	$t_{OFF(EN)}$		—	0.2	—	—	0.2	—	μs
"OFF" Isolation	ISO_{OFF}	(Note 4)	—	88	—	—	88	—	dB
Crosstalk	CT	(Note 3)	—	98	—	—	98	—	dB
Source Capacitance	$C_{S(OFF)}$	Switch "OFF", V_S = 0V, V_D = 0V	—	2.5	—	—	2.5	—	pF
Drain Capacitance	$C_{D(OFF)}$	Switch "OFF", V_S = 0V, V_D = 0V	—	7	—	—	7	—	pF
Input to Output Capacitance	$C_{DS(OFF)}$	(Note 4)	—	0.3	—	—	0.3	—	pF

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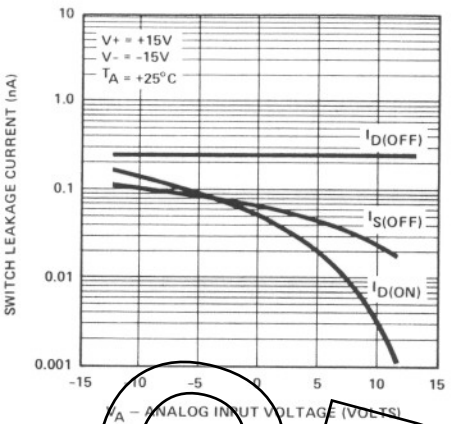
NOTES:
1. Conditions applied to leakage tests insure worst case leakages. Exceeding 11V on the analog input may cause an "OFF" channel to turn "ON".
2. Sample tested. The measurement conditions of Figure 1 insure worst case transition time.
3. Crosstalk is measured by driving channel 8 with channel 4 ON. R_L = 1MΩ, C_L = 10pF, V_S = 5V RMS, f = 20kHz. (See Figure 2)
4. OFF isolation is measured by driving channel 8 with ALL channels OFF. R_L = 1kΩ, C_L = 10pF, V_S = 5V RMS, f = 20kHz. C_{DS} is computed from the OFF isolation measurement.
5. Guaranteed by R_{ON} and leakage current testing. For normal operation maximum analog signal voltages should be restricted to less than (V+) −4V.

DICE

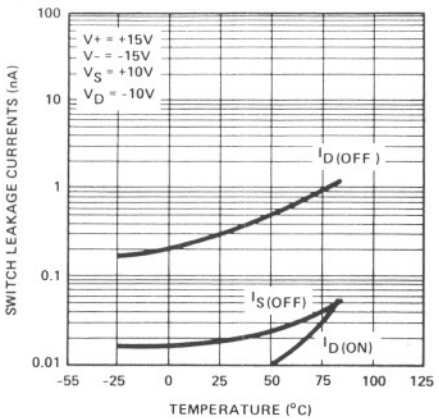
For applicable DICE information see MUX-08/MUX-24 data sheet.

TYPICAL PERFORMANCE CHARACTERISTICS

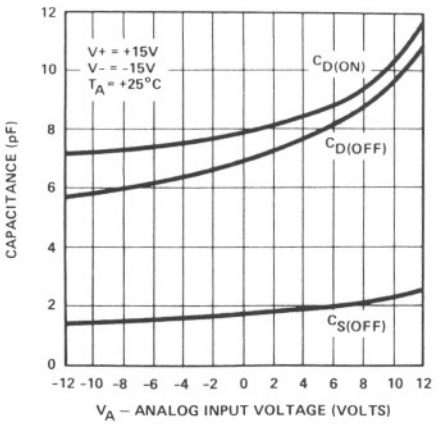
SWITCH LEAKAGE CURRENTS vs ANALOG INPUT VOLTAGE



SWITCH LEAKAGE CURRENTS vs TEMPERATURE



SWITCH CAPACITANCE vs ANALOG INPUT VOLTAGE



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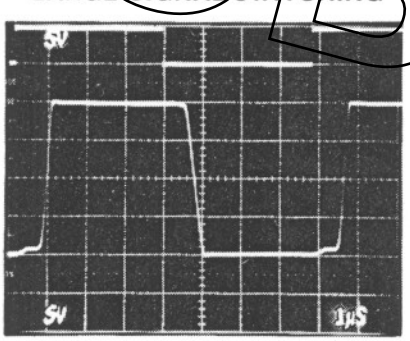
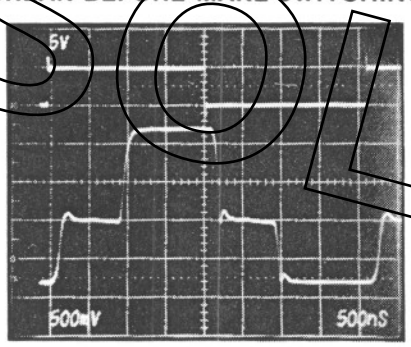
LARGE-SIGNAL SWITCHING



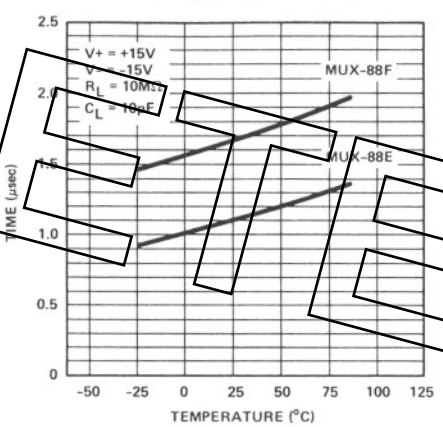
*R_L = 10MΩ, C_L = 10pF, V_1 = −10V, V_8 = +10V Voltage = 5V/Div, Time = 1μs/Div, See Transition Time Circuit of Figure 1.

BREAK-BEFORE-MAKE SWITCHING

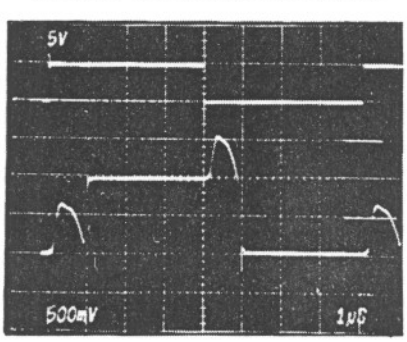


*Voltage = 500mV/Div, Time = 500ns/Div, See Break-Before-Make Circuit of Figure 3.

TRANSITION TIMES vs TEMPERATURE

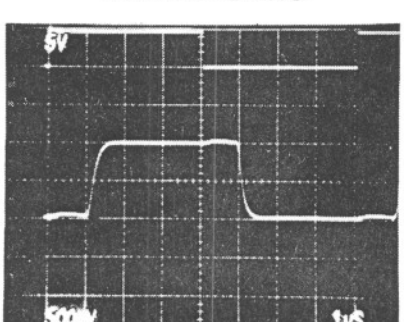


SMALL-SIGNAL SWITCHING



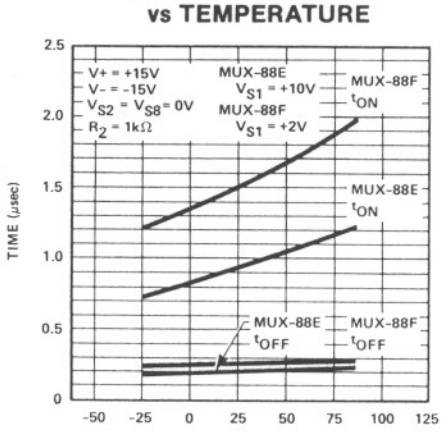
*R_L = 1MΩ, C_L = 10pF, V_1 = −500mV, V_{S8} = +500mV Voltage = 500mV/Div, Time = 1μs/Div, See Transition Circuit of Figure 1.

SMALL-SIGNAL SWITCHING WITH FILTERING



*R_L = 1MΩ, C_L = 500pF, V_1 = −500mV, V_{S8} = 500mV Voltage = 500mV/Div, Time = 1μs/Div, See Transition Time Circuit of Figure 1.

ENABLE DELAY TIME vs TEMPERATURE



NOTE:

*Top Waveforms: Digital Input 5V/Div
Bottom Waveforms: Multiplex Output

A.C. TEST CIRCUITS

TRANSITION TIME

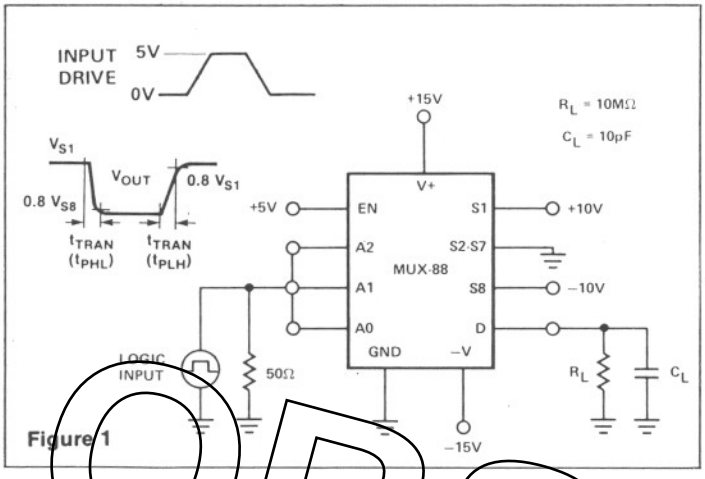


Figure 1

CROSSTALK MEASUREMENT CIRCUIT

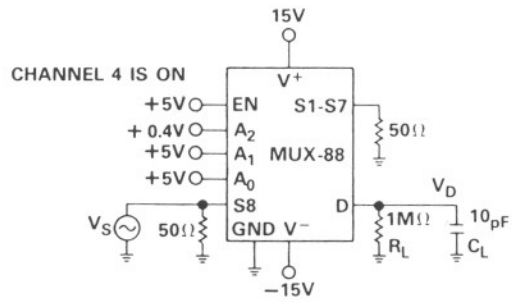


Figure 2

BREAK-BEFORE-MAKE DELAY

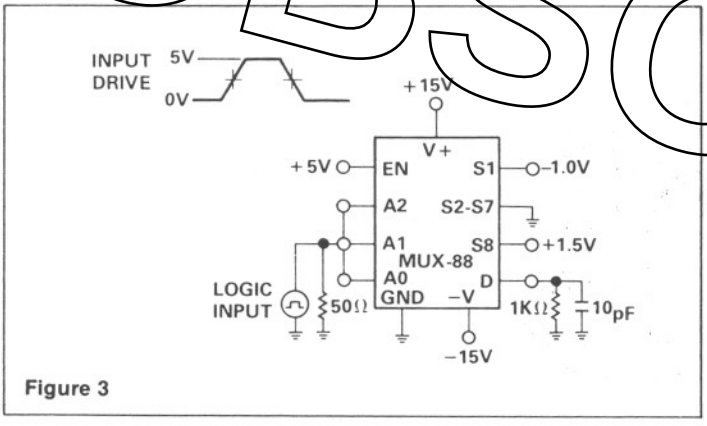


Figure 3

OFF ISOLATION MEASUREMENT CIRCUIT

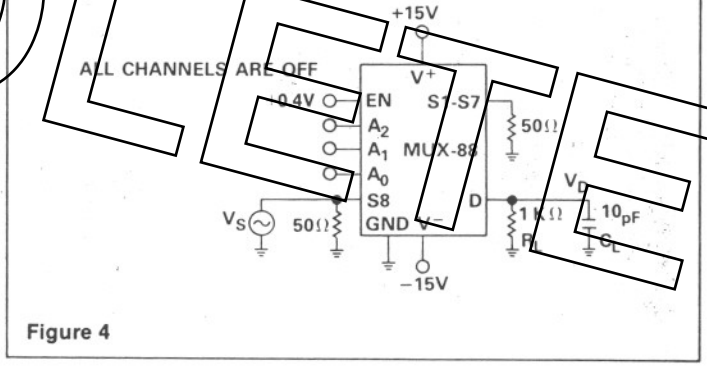


Figure 4

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APPLICATIONS INFORMATION

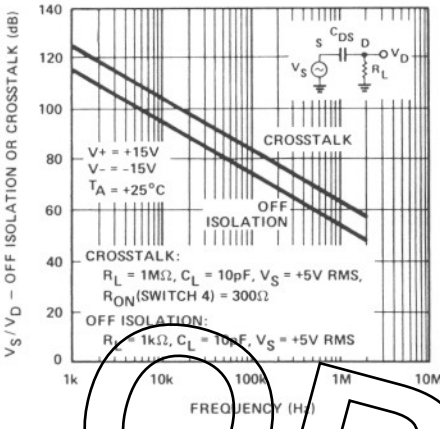
These analog multiplexers employ ion-implanted JFETs in a switch configuration designed to assure break-before-make action. The turn-off time is much faster than the turn-on time to guarantee this feature over the full operating temperature and input voltage range. Because the digital inputs only require a 2V logic "1" input level, power-consuming pull-up resistors are not required for TTL compatibility to insure break-before-make switching as is most often the case with CMOS multiplexers. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode (about 10nA) as the input voltage is raised above ≈ 1.4V.

The "ON" resistance, R_{ON}, of the analog switches is constant over the wide input voltage range of −15V to +11V with $V_{SUPPLY} = \pm 15V$. Higher input voltage is tolerable provided that some form of current limiting is employed (such as that of an op-amp output stage) to avoid exceeding junction temperature and power dissipation requirements. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply). This assures that the V_{GS} of an OFF switch remains greater than its V_P, and prevents that channel from being falsely turned ON.

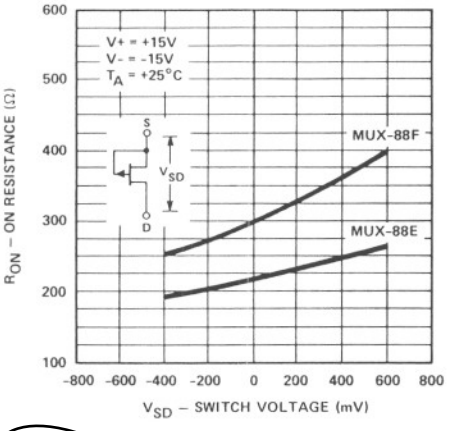
When operating with negative input voltages, the gate-to-channel diode will be turned on if the voltage drop across an ON switch exceeds −0.6V. While this condition will cause an error in the output, it will not damage the switch. In lab tests, the multiplexer output load capacitor has increased to 0.01μF in the Transition Time circuit, Figure 1. With $V_{S1} = -10V$ and $V_{S8} = +10V$, the logic input was driven at a 1kHz rate. The positive-going slew rate was 0.3V/μsec which is equivalent to a normal I_{DSS} of 3mA. The negative-going slew rate was 0.7V/μsec which is equivalent to a "reverse" I_{DSS} of 7mA. Note that when switch 1 is first turned ON it has a drop of −20V across its terminals. In spite of that fact, the current is limited to approximately twice its normal I_{DSS}.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

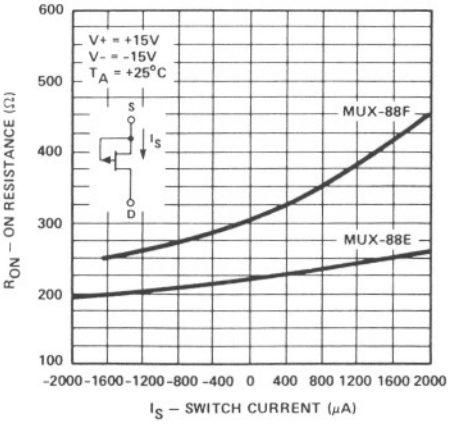
OFF PERFORMANCE OF CHANNEL 8



R_{ON} vs SWITCH VOLTAGE (V_{SD})



R_{ON} vs SWITCH CURRENT (I_S)



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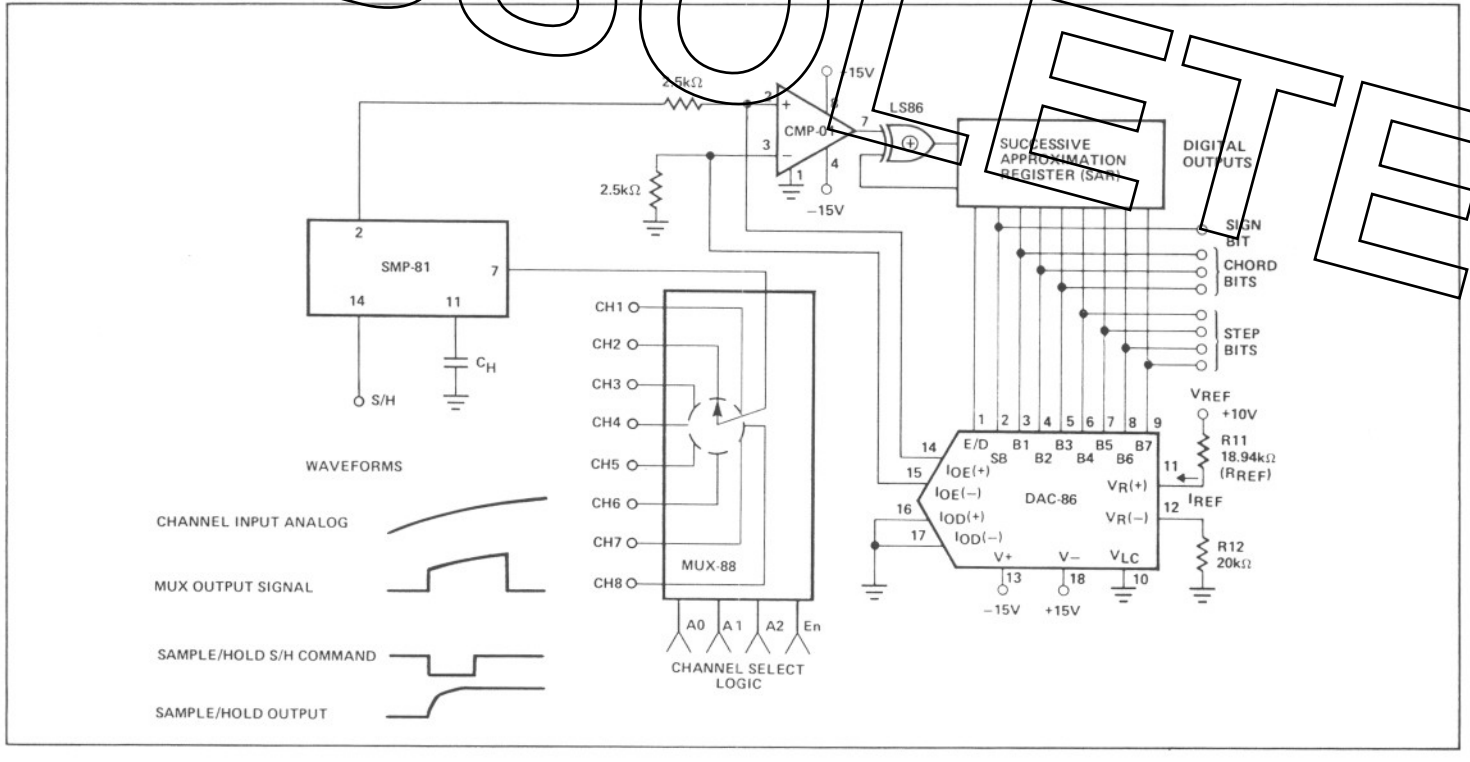
TYPICAL APPLICATION

EIGHT-CHANNEL SHARED CODEC PCM ENCODER



CROSSTALK IN PCM SYSTEMS

In PAM or PCM systems crosstalk specifications for components, such as multiplexers, are related to overall system crosstalk specifications in a complex manner. Component specification must, of necessity, refer to the operation of the multiplexer in a non-sampling mode of operation. When rapid sequential sampling takes place, such as would be the case with a typical shared-channel CODEC, crosstalk will be caused by the off isolation properties of the multiplexer as well as by storage elements on chip and PC card stray capacitance. For example, the capacitance has the effect of conferencing the channels and increasing crosstalk. Thus, system crosstalk in a shared-channel PCM CODEC is influenced by multiplexed characteristics as well as PC card layout and the timing relationship between the multiplexer and the sample-hold circuit.