

# DATA SHEET

**ELECTROSTATIC DISCHARGE  
PROTECTION DEVICES**

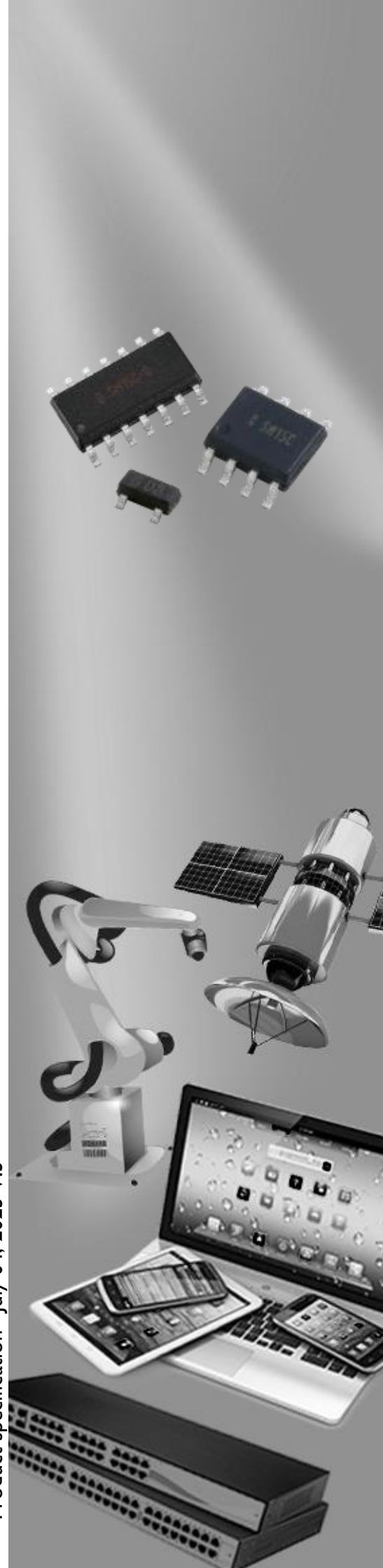
**INDUSTRIAL / CONSUMER**

UDS08A03L04

RoHS compliant & Halogen free



Product specification— July 04, 2023 V.3



## Electrostatic Discharged Protection Devices (ESD) Data Sheet

### Description

The UDS08A03L04 component is designed to protect low voltage state-of-the-art CMOS semiconductors from transients caused by electrostatic discharge (ESD), cable discharge events (CDE), lightning and other induced voltage surges. The device provides low stand-off voltages with significant reductions in leakage currents and capacitance over silicon avalanche diode processes.

The UDS08A03L04 features integrated low capacitance compensation diodes that reduce the typical capacitance 3pF per line.

This combined with low leakage current, means signal integrity preserved in high-speed applications such as 10/100/1000 Ethernet.

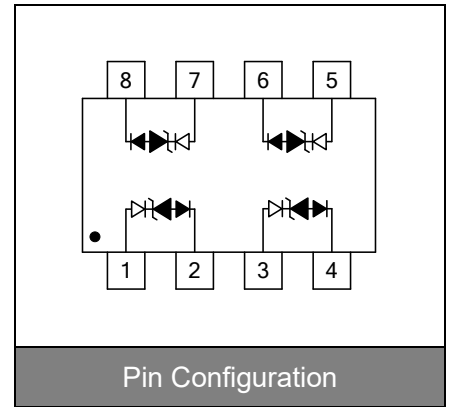


Contact : ±30kV  
Air : ±30kV



### Features

- IEC61000-4-2 ESD 30KV Air, 30KV contact compliance
- SOIC-08 surface mount package
- Protects four I/O lines
- Peak power dissipation of 400W under 8/20µs waveform
- Working voltage: 3.3V
- Low leakage current
- Low operating and clamping voltages
- Solid-state silicon avalanche technology
- Lead Free/RoHS compliant
- Solder reflow temperature: Pure Tin-Sn, 260~270°C
- Flammability rating UL 94V-0
- Meets MSL level 1, per J-STD-020
- Marking: B SLVU03-4



### Applications

- 10/100/1000 Ethernet
- WAN/LAN Equipment
- High current switching systems
- Desktops, Servers and Notebook
- Instrumentation
- Analog inputs
- Base stations

### Maximum Ratings

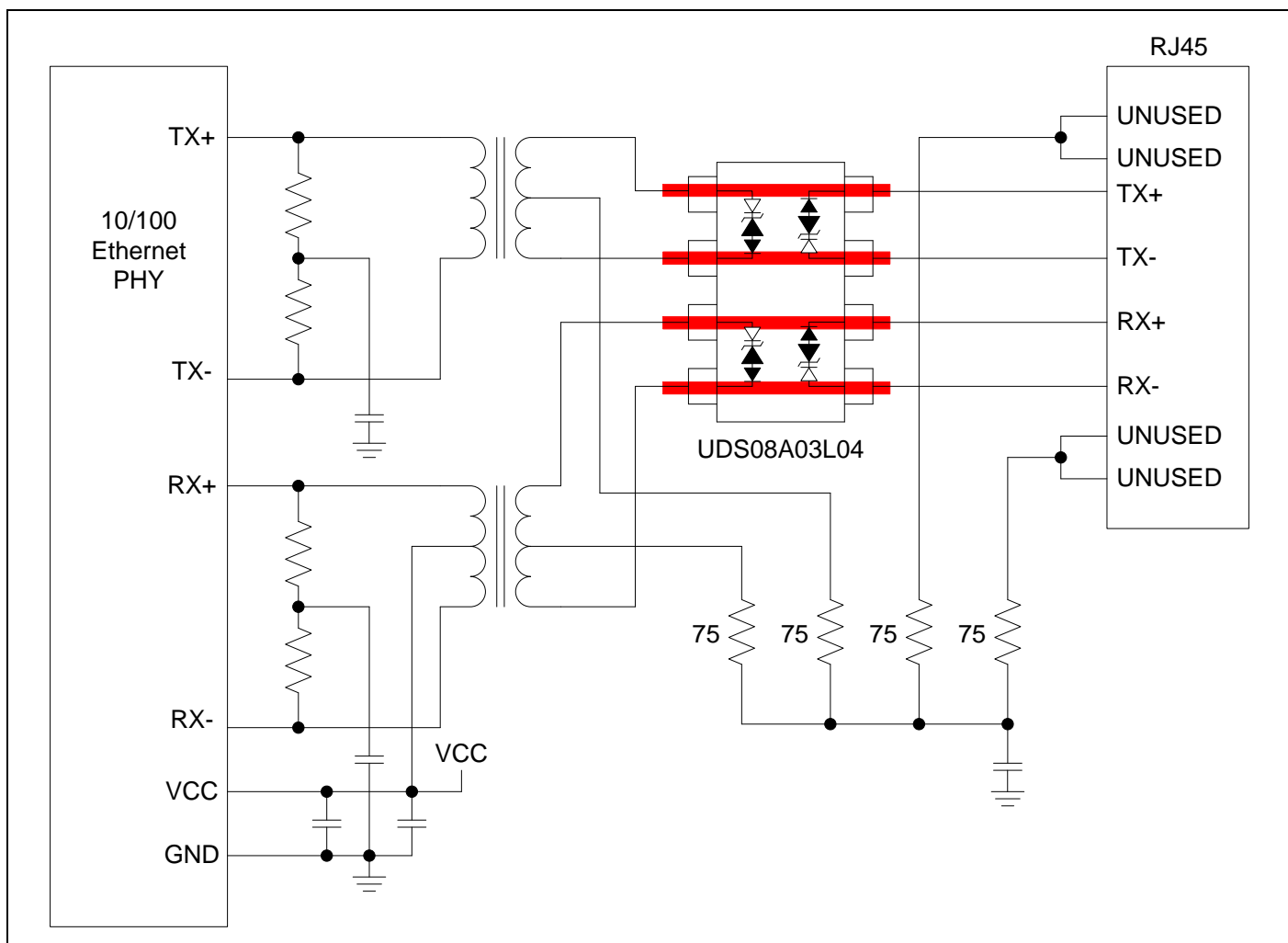
Rating	Symbol	Value	Unit
ESD voltage (Contact discharge)	V <sub>ESD</sub>	±30	kV
ESD voltage (Air discharge)		±30	
Storage & operating temperature range	T <sub>STG</sub> , T <sub>J</sub>	-55~+150	°C

**Electrical Characteristics (T<sub>J</sub>=25°C)**

Parameter	Symbol	Condition	Min.	Max.	Unit
Reverse stand-off voltage	V <sub>RWM</sub>			3.3	V
Reverse breakdown voltage	V <sub>BR</sub>	I <sub>BR</sub> =1mA	4.5		V
Reverse leakage current	I <sub>R</sub>	V <sub>R</sub> =3.3V Each I/O pin		0.1	uA
Clamping voltage (tp=8/20μs)	V <sub>C</sub>	I <sub>PP</sub> =5A		12.5	V
Peak pulse current (tp=8/20μs)	I <sub>PP</sub>			20	A
Off state junction capacitance	C <sub>J</sub>	0Vdc, f=1MHz Between I/O pins and GND		1.8	pF
		0Vdc, f=1MHz Line to Line, two I/O pins connected together on each line (Note)		3.6	pF

Note: Ratings with two pins connected together per the recommended configuration (ie pin 1 connected to pin 8, pin 2 connected to pin 7, pin 3 connected to pin 6, pin 4 connected to pin 5).

**Applications Information**



### Typical Characteristics Curves

Figure 1. Power Derating Curve

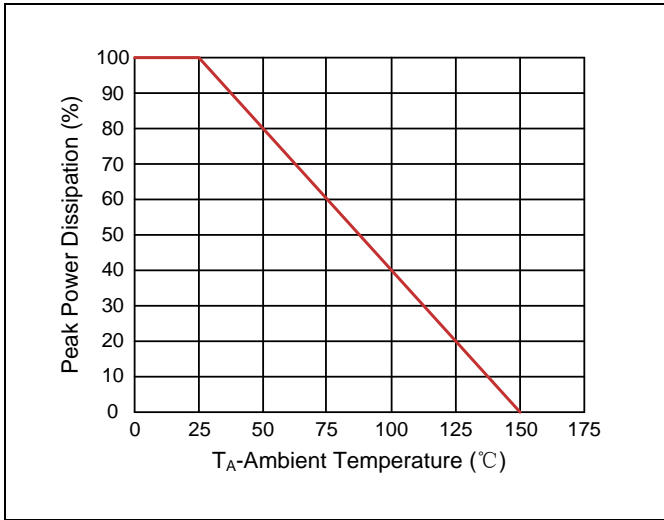


Figure 2. Pulse Waveforms

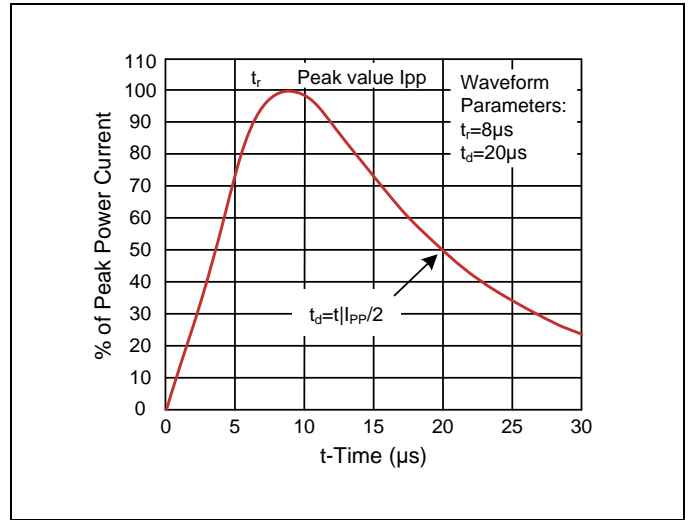


Figure 3. Non-Repetitive Peak Pulse vs. Pulse Time

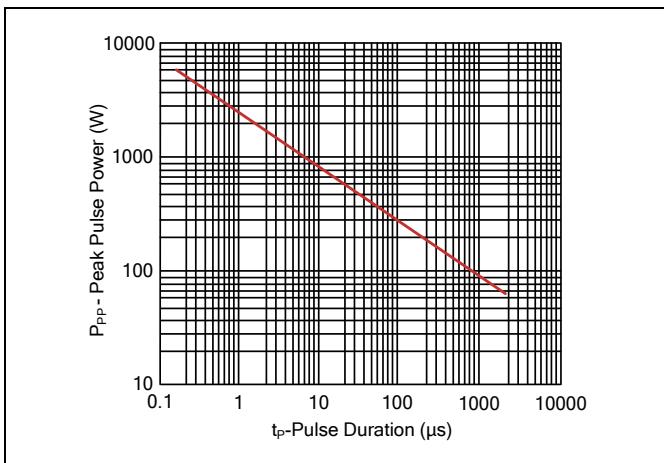


Figure 4. Capacitance vs. Reverse Voltage

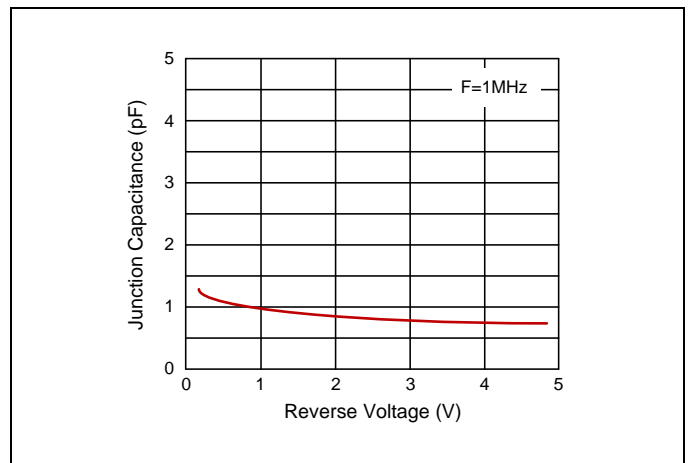
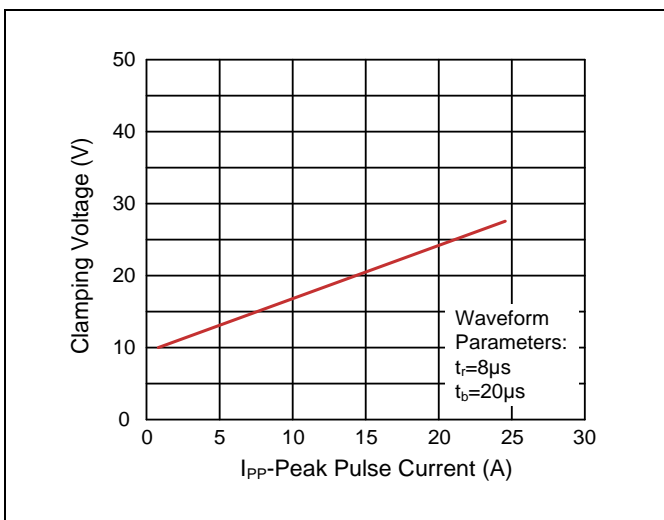
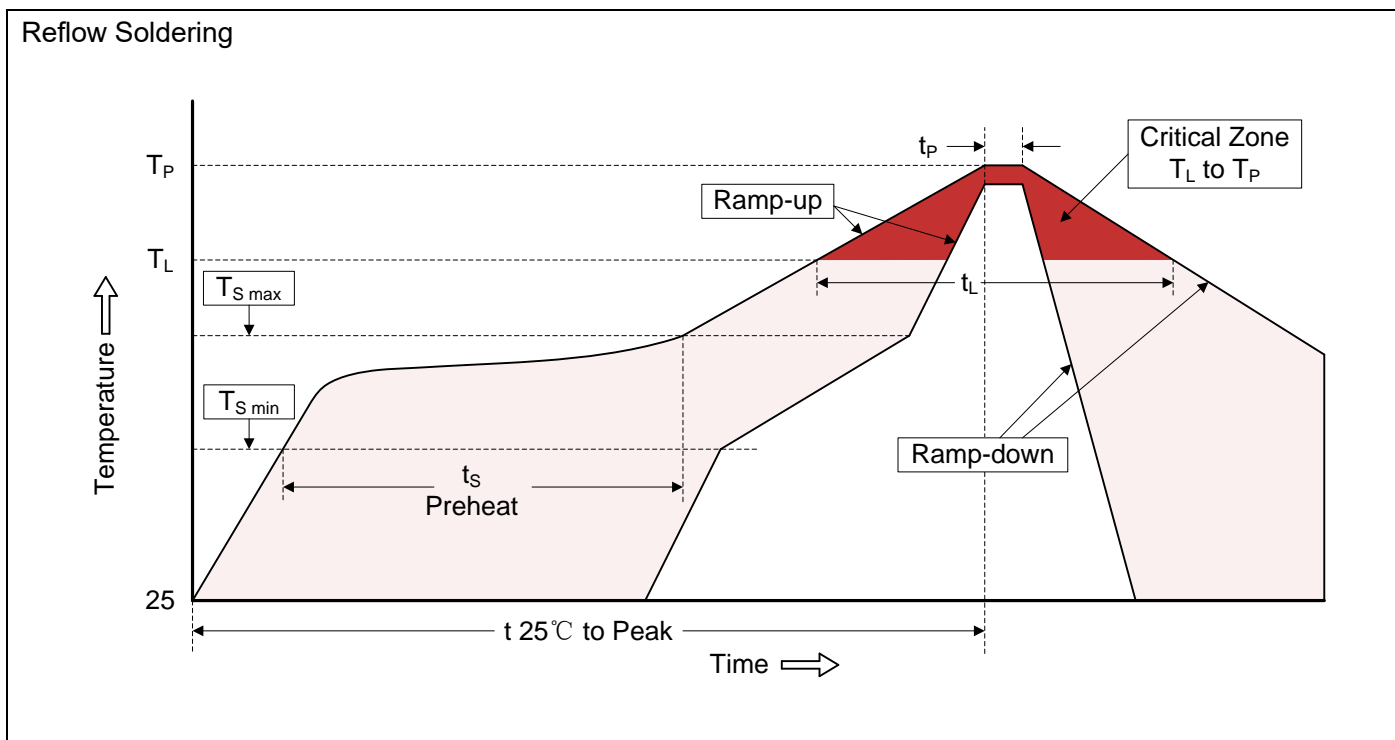


Figure 5. Clamping Voltage vs. Peak Pulse Current



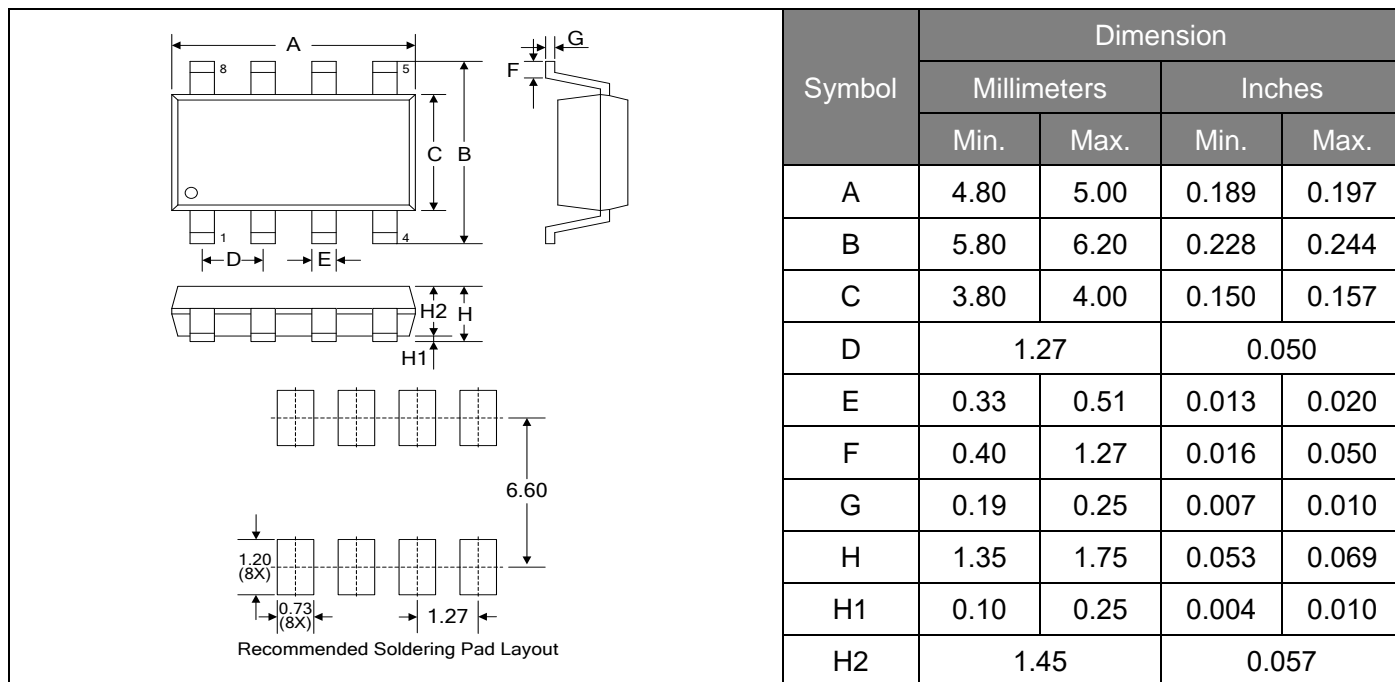
### Recommended Soldering Conditions



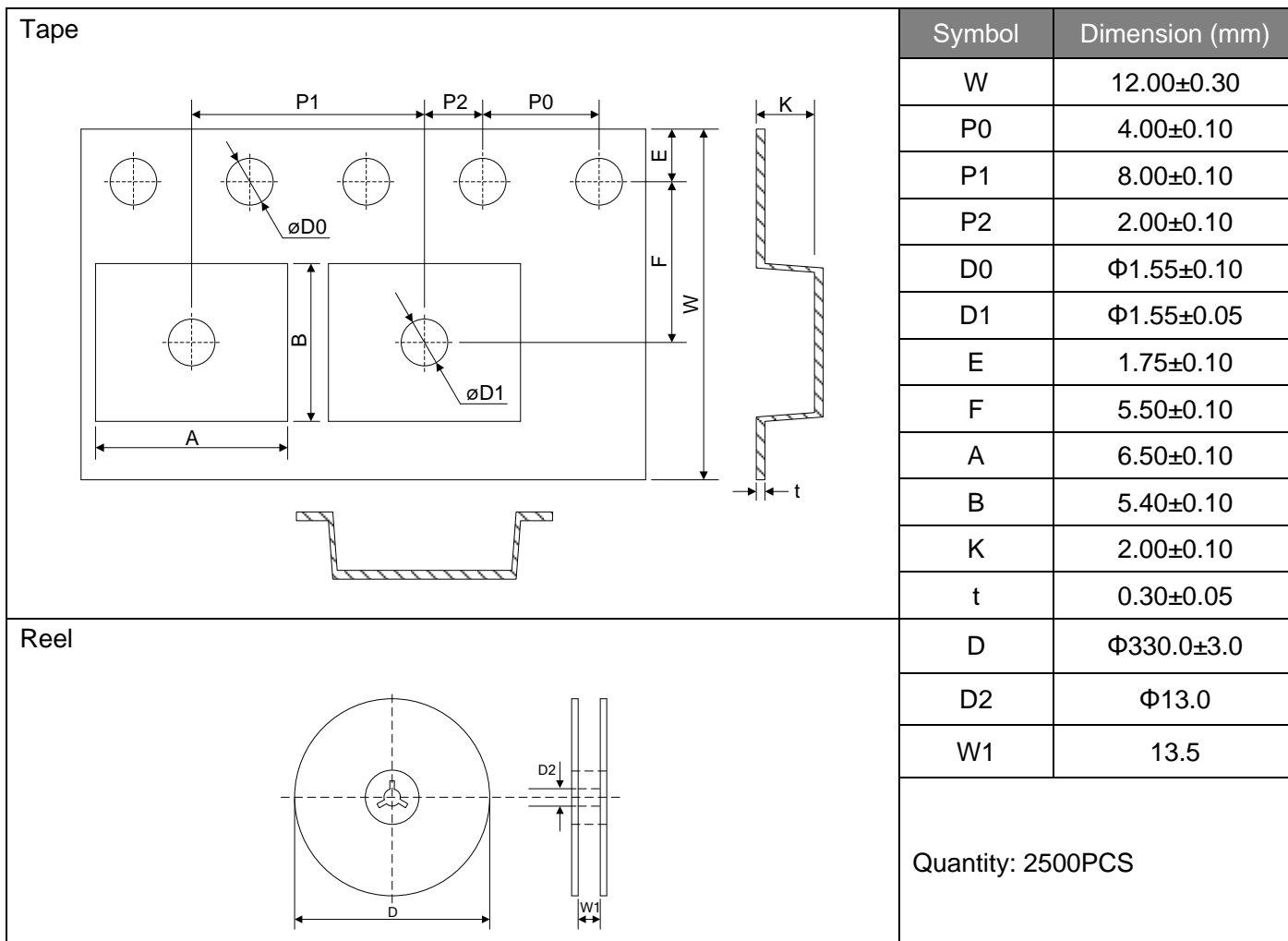
#### Recommended Conditions

Profile Feature	Pb-Free Assembly
Average ramp-up rate ( $T_L$ to $T_P$ )	3°C/second max.
Preheat -Temperature Min ( $T_{S\ min}$ ) -Temperature Max ( $T_{S\ max}$ ) -Time (min to max) ( $t_s$ )	150°C 200°C 60-180 seconds
$T_{S\ max}$ to $T_L$ -Ramp-up Rate	3°C/second max.
Time maintained above: -Temperature ( $T_L$ ) -Time ( $t_L$ )	217°C 60-150 seconds
Peak Temperature ( $T_P$ )	260°C
Time within 5°C of actual Peak Temperature ( $t_P$ )	20-40 seconds
Ramp-down Rate	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.

**Dimensions (SOIC-08)**



**Packaging**



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