

Features

- Supply Voltage: 4.5V to 36V
- Rail to Rail Output
- Bandwidth: 1 MHz
- Slew Rate: 0.7V/ μ s
- Excellent EMI Suppress Performance
- Offset Voltage: $\pm 150\mu$ V Maximum
- Offset Voltage Temperature Drift: 2 μ V/ $^{\circ}$ C
- Low Noise: 30 nV/ \sqrt Hz at 1kHz
- -40° C to 125° C Operation Temperature Range

Applications

- Instrumentation
- Active Filters, ASIC Input or Output Amplifier
- Sensor Interface
- Motor Control
- Industrial Control

Description

The TP07A is newest high supply voltage amplifiers with low offset, low power and stable high frequency response. It incorporates 3PEAK's proprietary and patented design techniques to achieve very good AC performance with 1MHz bandwidth, 0.7V/ μ s slew rate and low distortion while drawing only 900 μ A of quiescent current per amplifier. The input common-mode voltage range extends to V_{-} , and the outputs swing rail-to-rail. The TP07A can be used as plug-in replacements for many commercially available op-amps to reduce power and improve input/output range and performance.

The combination of features makes the TP07A ideal choices for industrial control, instrumentation.

Pin Configuration

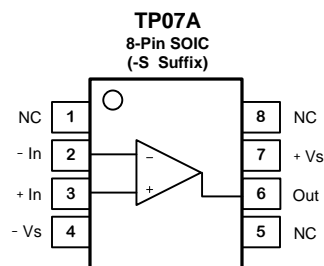


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Revision History

Date	Revision	Notes
2018/12/21	Rev.Pre	Pre-Release Version
2020/12/21	Rev.A.0	Release Version

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity
TP07A-SR	-40 to 125°C	8-Pin SOIC	TP07A	3	Tape and Reel, 4000

Absolute Maximum Ratings ^{Note 1}

Parameters	Rating
Supply Voltage, (+V _S)– (-V _S)	40 V
Input Voltage	(-V _S) – 0.3 to (+V _S) + 0.3
Differential Input Voltage	(+V _S) - (-V _S)
Input Current: +IN, –IN ^{Note 2}	±10mA
Output Short-Circuit Duration ^{Note 3}	Infinite
Maximum Junction Temperature	150°C
Operating Temperature Range	–40 to 125°C
Storage Temperature Range	–65 to 150°C
Lead Temperature (Soldering, 10 sec)	260°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 300mV beyond the power supply, the input current should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD Rating

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	MIL-STD-883H Method 3015.8	2	kV
CDM	Charged Device Model ESD	JEDEC-EIA/JESD22-C101E	1	kV

Thermal Information

Package Type	θ _{JA}	θ _{JC}	Unit
8-Pin SOIC	158	43	°C/W

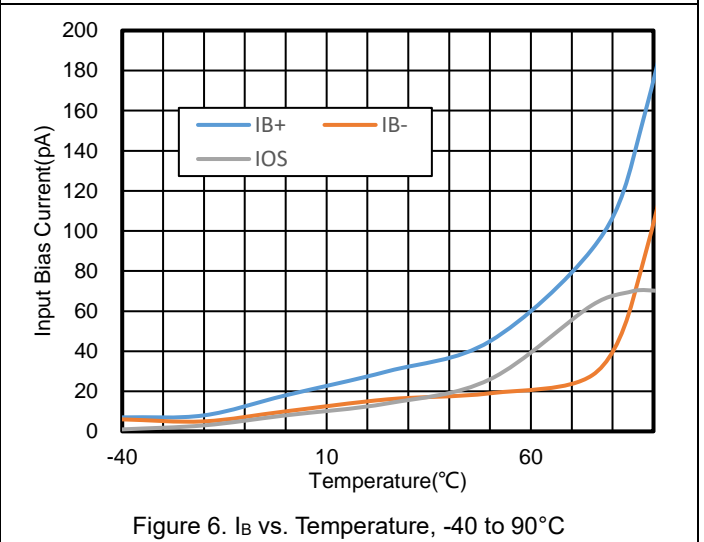
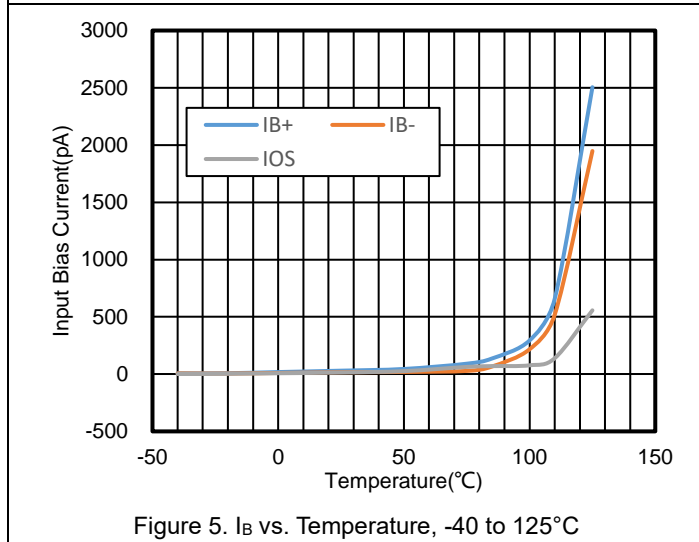
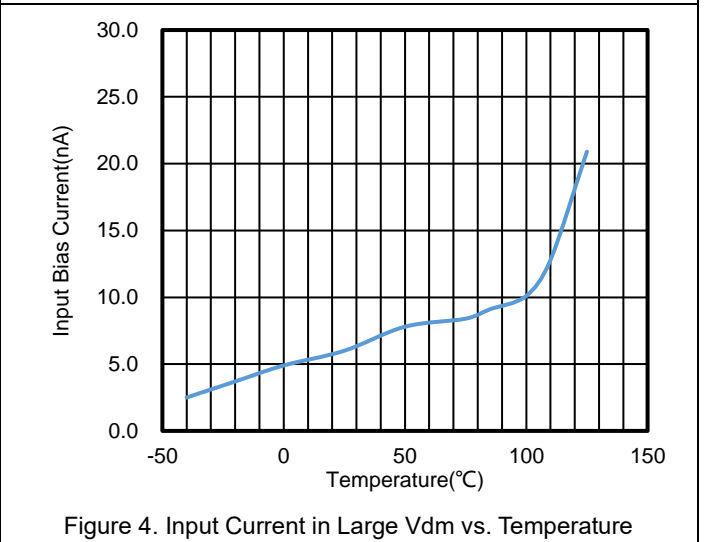
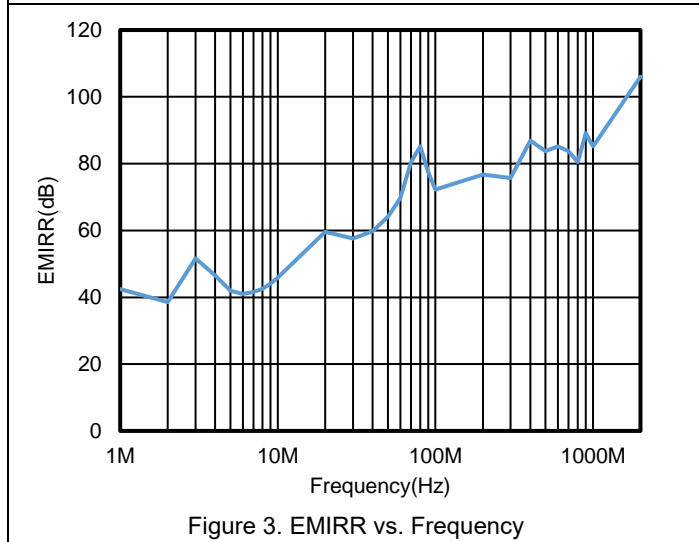
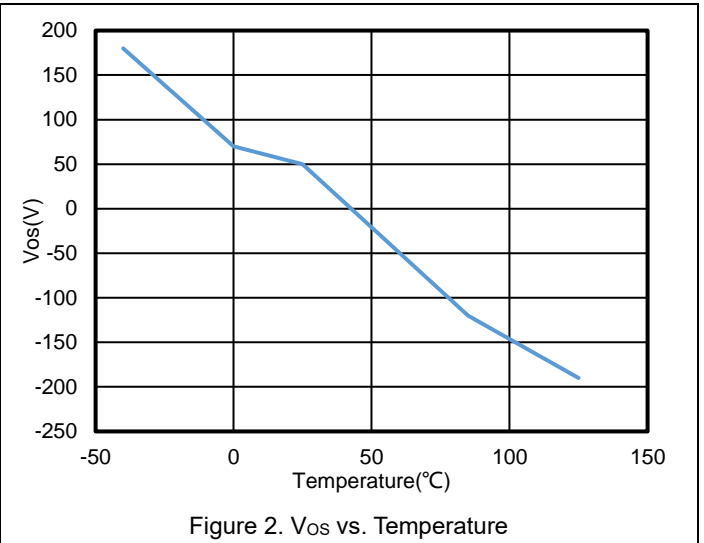
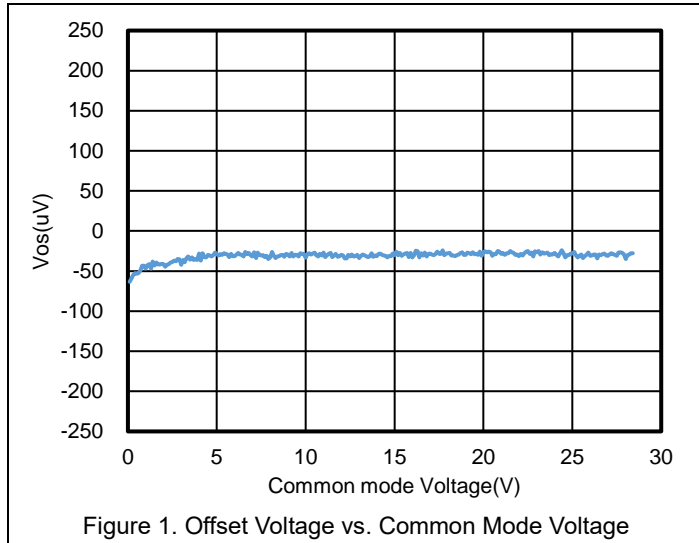
Electrical Characteristics

All test condition is $V_S = 30V$, $T_A = 25^\circ C$, $R_L = 10k\Omega$, unless otherwise noted.

Symbol	Parameter	Conditions	T_A	Min	Typ	Max	Unit
Power Supply							
V_S	Supply Voltage Range			4.5		36	V
I_Q	Quiescent Current per Amplifier	$V_S = 30V$			900	1600	μA
			-40°C to 125°C			1800	μA
PSRR	Power Supply Rejection Ratio	$V_S = 4.5V$ to 36V		100	120		dB
			-40°C to 125°C	95			dB
Input Characteristics							
V_{OS}	Input Offset Voltage	$V_S = 30V$, $V_{CM} = 15V$		-150	50	150	μV
			-40°C to 125°C	-650		650	μV
		$V_S = 25V$, $V_{CM} = 12.5V$		-150	50	150	μV
			-40°C to 125°C	-650		650	μV
$V_{OS\ TC}$	Input Offset Voltage Drift		-40°C to 125°C		2		μV/°C
I_B	Input Bias Current				25		pA
			-40°C to 85°C		80		pA
			-40°C to 125°C		1000		pA
I_{OS}	Input Offset Current				25		pA
I_{IN}	Differential Input Current	$V_S = 36V$, $V_{ID} = 36V$			10	200	nA
			-40°C to 125°C		100	300	nA
C_{IN}	Input Capacitance	Differential Mode			5		pF
		Common Mode			2.5		pF
A_V	Open-loop Voltage Gain	$V_S = 30V$, $V_{OUT} = 0.5V$ to 29.5V		100	120		dB
			-40°C to 125°C	90			dB
V_{CMR}	Common-mode Input Voltage Range			(V-)		(V+) - 1.5	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = 0.5V$ to 28.5V		100	120		dB
			-40°C to 125°C	95			dB
Output Characteristics							
V_{OH}	Output Swing from Positive Rail	$R_{LOAD} = 100k\Omega$ to $V_S/2$			15	30	mV
			-40°C to 125°C			50	mV
		$R_{LOAD} = 10k\Omega$ to $V_S/2$			60	90	mV
			-40°C to 125°C			140	mV
V_{OL}	Output Swing from Negative Rail	$R_{LOAD} = 100k\Omega$ to $V_S/2$			10	20	mV
			-40°C to 125°C			30	mV
		$R_{LOAD} = 10k\Omega$ to $V_S/2$			35	50	mV
			-40°C to 125°C			90	mV
I_{SC}	Output Short-Circuit Current			60		mA	

AC Specifications							
GBW	Gain-Bandwidth Product				1		MHz
SR	Slew Rate	G = 1		0.3	0.7		V/μs
			-40°C to 125°C	0.1			V/μs
t _{OR}	Overload Recovery				2		μs
t _S	Settling Time, 0.1%	G = -1, 10V step			15		μs
	Settling Time, 0.01%				20		μs
PM	Phase Margin	V _S = 36V, R _L =10K, C _L =100pF			50		°
GM	Gain Margin	V _S = 36V, R _L =10K, C _L =100pF			10		dB
Noise Performance							
E _N	Input Voltage Noise	f = 0.1Hz to 10Hz			2		μV _{RMS}
e _N	Input Voltage Noise Density	f = 1kHz			30		nV/√Hz
i _N	Input Current Noise	f = 1kHz			2		fA/√Hz
THD+N	Total Harmonic Distortion and Noise	f = 1kHz, G = 1, R _L = 10kΩ, V _{OUT} = 6V _{RMS}			0.002		%
Thermal Shutdown							
	Thermal Shutdown temperature				170		°C
	Recover Temperature				150		°C

Typical Performance Characteristics



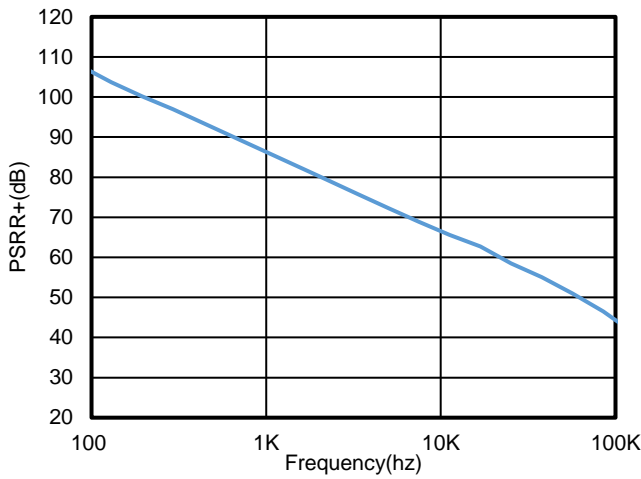


Figure 7. PSRR+ vs. Frequency

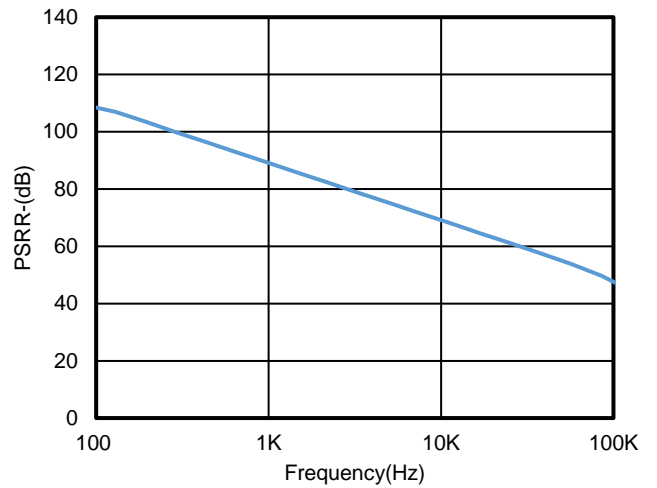


Figure 8. PSRR- vs. Frequency

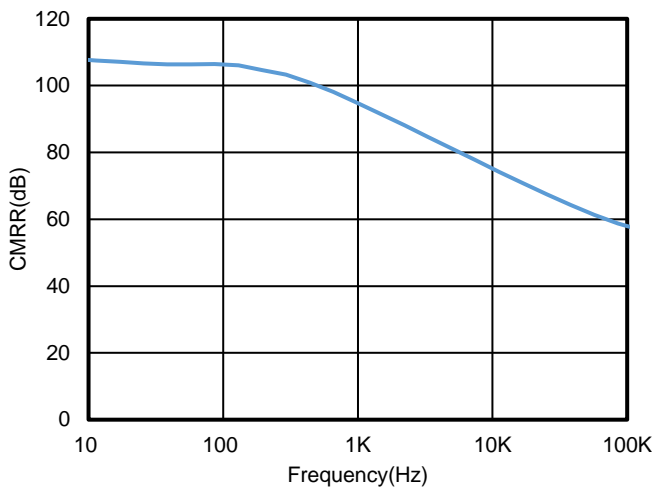


Figure 9. CMRR vs. Frequency

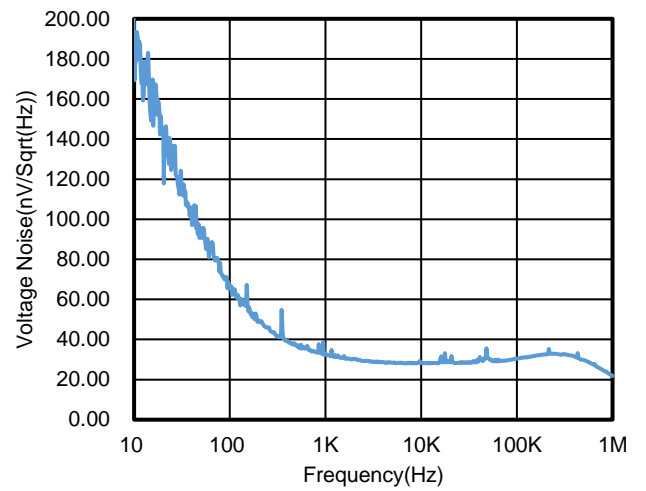


Figure 10. Voltage Noise Spectral Density vs. Frequency

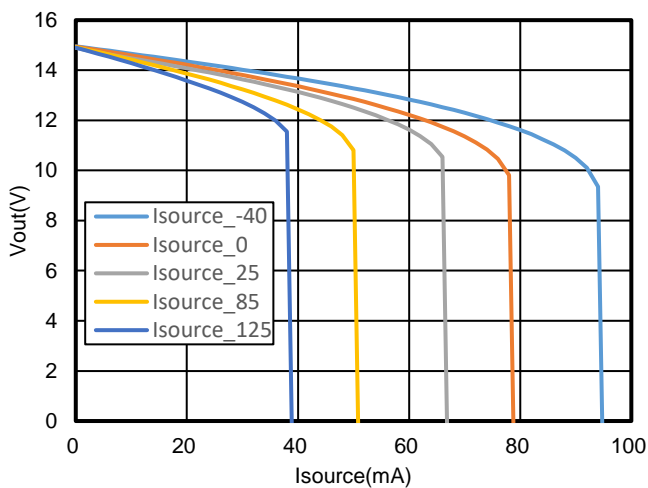


Figure 11. Positive Output Voltage vs. Output Current

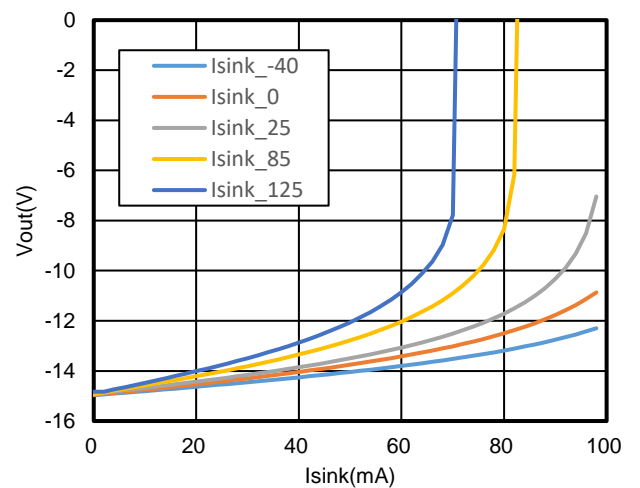


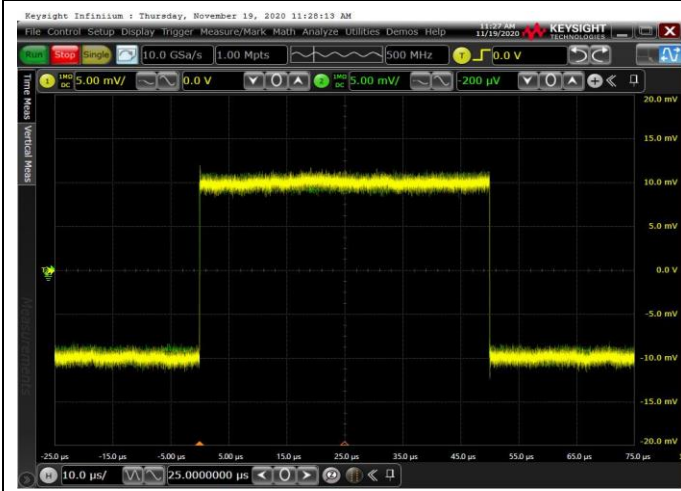
Figure 12. Negative Output Voltage vs. Output Current



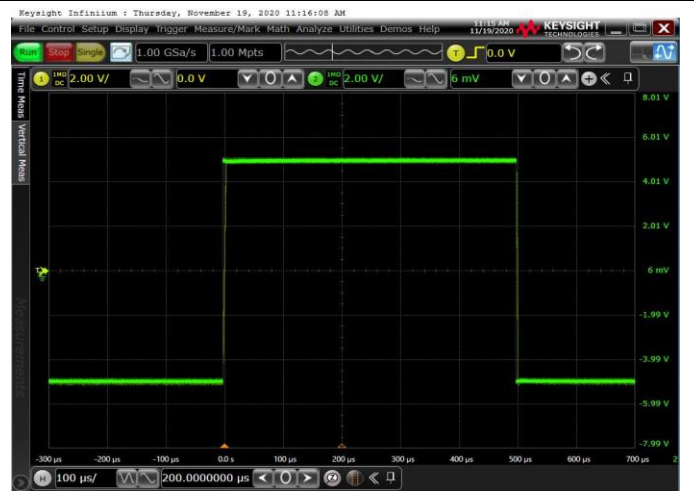
Voltage: 5V/div for Output, Time: 10 μ s/div
 $G=10$, $V_{REF} = GND$; $V_{IN}=5V_{PP}$
 Figure 13. Positive Overload Recovery



Voltage: 5V/div for Output, Time: 10 μ s/div
 $G=10$, $V_{REF} = GND$; $V_{IN}=5V_{PP}$
 Figure 14. Negative Overload Recovery

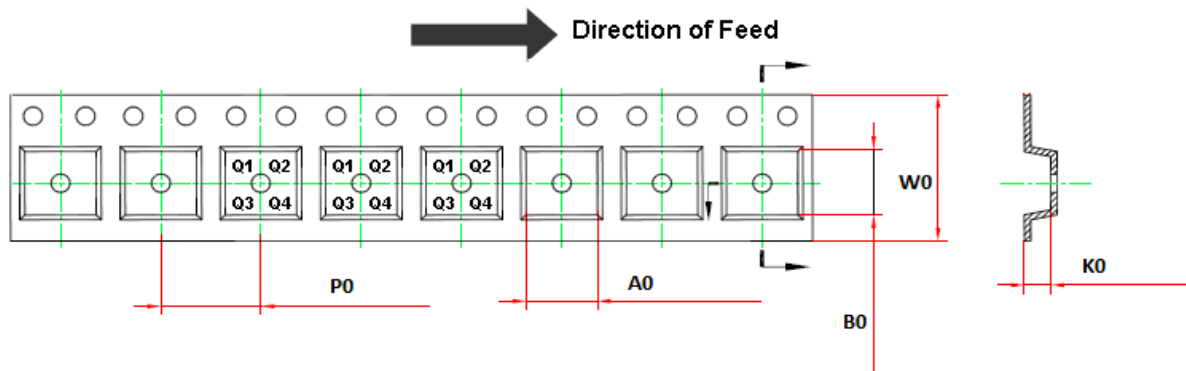
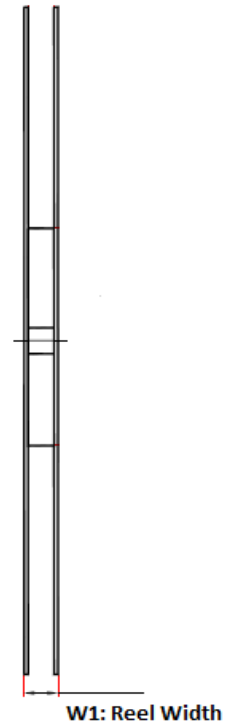
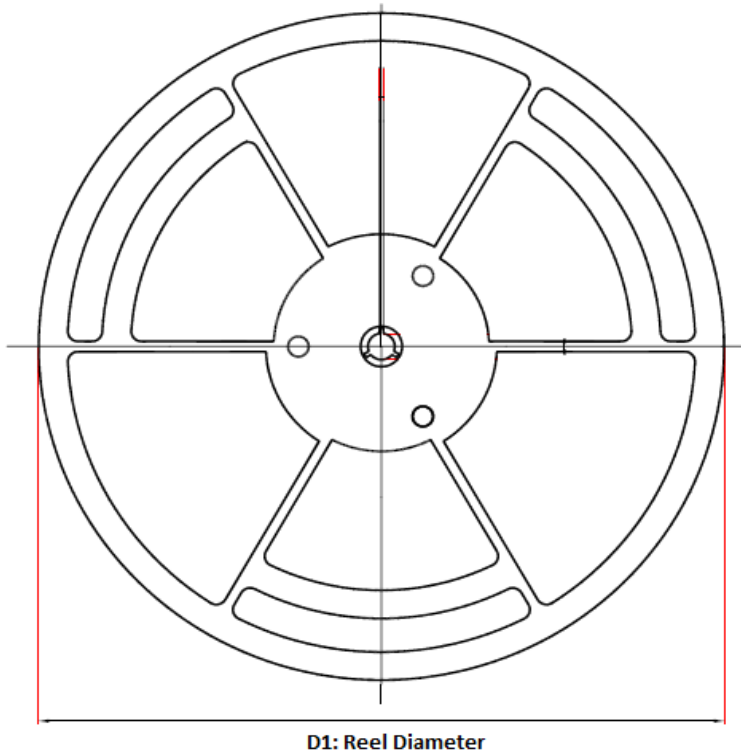


Voltage: 5mV/div, Time: 10 μ s/div
 $R_L=2K$, $C_L=100pF$, $G=1$
 Figure 15. 20mV Signal Step Response



Voltage: 5V/div, Time: 100 μ s/div
 $R_L=2K$, $C_L=100pF$, $G=1$
 Figure 16. 10V Signal Step Response

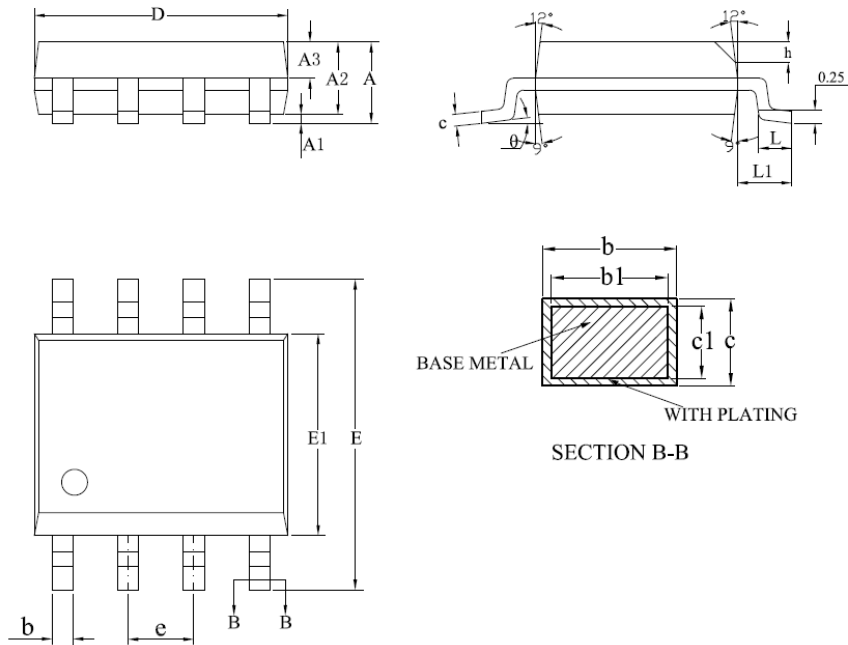
Tape and Reel Information



Order Number	Package	D1	W1	A0	B0	K0	P0	W0	Pin1 Quadrant
TP07A-SR	8-Pin SOIC	330.0	17.6	6.4	5.4	2.1	8.0	12.0	Q1

Package Outline Dimensions

SOIC-8



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

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