T-46-07-11

National Semiconductor

54FCT/74FCT374
Octal D Flip-Flop with TRI-STATE® Outputs

General Description

The 'FCT374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

FACT™ FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

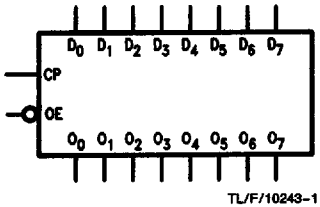
FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

- I_{CC} and I_{OZ} reduced to 40.0 μA and ±2.5 μA respectively
- NSC 54FCT/74FCT374 is pin and functionally equivalent to IDT 54FCT/74FCT374
- Controlled output edge rates and undershoot for improved noise immunity. Internal split ground for improved noise immunity
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA (commercial) and 32 mA (military)
- CMOS power levels
- ESD immunity ≥ 4kV typ
- Military product compliant to MIL-STD 883 and standard military drawing #5962-87628

Ordering Code: See Section 8

Logic Symbols



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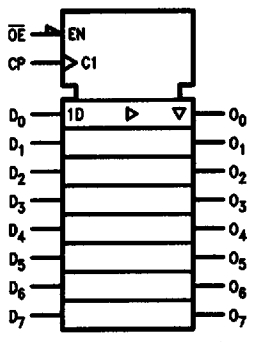
IEEE/IEC



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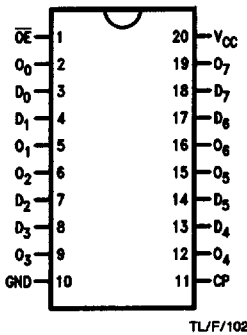
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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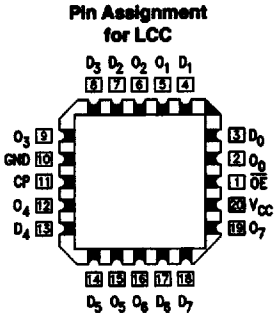
Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
O_0–O_7	TRI-STATE Outputs

Pin Assignment for LCC



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Functional Description

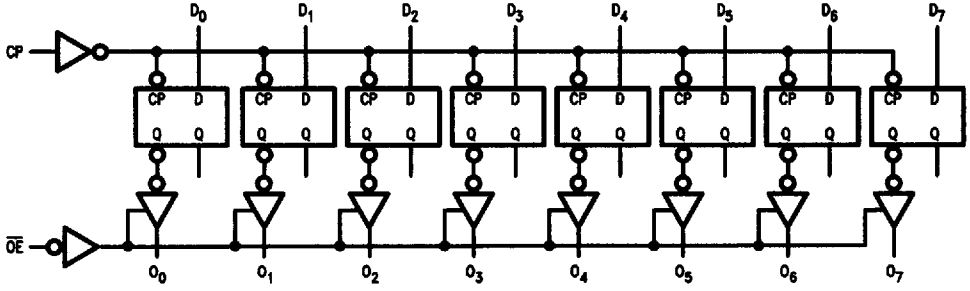
The 'FCT374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Truth Table

Inputs			Outputs
D_n	CP	$\overline{OE}$	O_n
H	↗	L	H
L	↗	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↗ = LOW-to-HIGH Transition

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})
- 54FCT: −0.5V to 7.0V
- 74FCT: −0.5V to 7.0V

Temperature under Bias (T_{BIAS})
- 74FCT: −55°C to +125°C
- 54FCT: −65°C to +135°C

Storage Temperature (T_{STG})
- 74FCT: −55°C to +125°C
- 54FCT: −65°C to +150°C

DC Output Current (I_{OUT}): 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 54FCT: 4.5V to 5.5V
- 74FCT: 4.75V to 5.25V

Input Voltage: 0V to V_{CC}

Output Voltage: 0V to V_{CC}

Operating Temperature (T_A)
- 54FCT: −55°C to +125°C
- 74FCT: 0°C to +70°C

Junction Temperature (T_J)
- CDIP: 175°C
- PDIP: 140°C

Note: All commercial mount packaging is not recommended for applications requiring greater than 2000 temperature cycles from −40°C to +125°C.

DC Characteristics for 'FCT Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, $V_{HC} = V_{CC} - 0.2V$.

Symbol	Parameter	54FCT/74FCT Min	Typ	Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0 5.0	μA	V_{CC} = Max	$V_I = V_{CC}$ V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0 −5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
I_{OZ}	Maximum TRI-STATE Current			2.5 2.5 −2.5 −2.5	μA	V_{CC} = Max	$V_O = V_{CC}$ V_O = 2.7V (Note 2) V_O = 0.5V (Note 2) V_O = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8	3.0		V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 μA	
		V_{HC} 2.4 2.4	V_{CC} 4.3 4.3			V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = −300 μA I_{OH} = −12 mA (Mil) I_{OH} = −15 mA (Com)
V_{OL}	Maximum Low Level Output Voltage		GND	0.2	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA	
			GND 0.3 0.3	0.2 0.50 0.50		V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 300 μA I_{OL} = 32 mA (Mil) I_{OL} = 48 mA (Com)
I_{CC}	Maximum Quiescent Supply Current		1.0	40.0	μA	V_{CC} = Max $V_{IN} \geq V_{HC}$, $V_{IN} \leq 0.2V$ f_I = 0	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	

DC Characteristics for 'FCT Family Devices (Continued)

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, $V_{HC} = V_{CC} - 0.2V$.

Symbol	Parameter	74FCT Min	74FCT Typ	74FCT Max	Units	Conditions	
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.15	0.25	mA/MHz	V_{CC} = Max Outputs Open One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
I_C	Total Power Supply Current (Note 6)		1.5	4.0	mA	V_{CC} = Max Outputs Open f_{CP} = 10 MHz $\overline{OE}$ = GND f_i = 5 MHz One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			1.8	6.0			V_{IN} = 3.4V V_{IN} = GND
			3.0	7.8		(Note 5) V_{CC} = Max Outputs Open f_{CP} = 10 MHz $\overline{OE}$ = GND f_i = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			5.0	16.8			V_{IN} = 3.4V V_{IN} = GND
V_H	Input Hysteresis to Clock Only		200		mV		

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

Note 7: For 54FCT, I_{CCD} = 0.40 mA/MHz.

Refer to applicable standard military drawing or NSC Table I for test conditions and I_C/I_{CC} limits.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	54FCT/74FCT $T_A = +25°C$ $V_{CC} = 5.0V$	74FCT $T_A, V_{CC} = Com$ $R_L = 500\Omega$ $C_L = 50\ pF$		54FCT $T_A, V_{CC} = Mil$ $R_L = 500\Omega$ $C_L = 50\ pF$		Units	Fig. No.
		Typ	Min (Note 1)	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay C_P to O_n	6.6	2.0	10.0	2.0	11.0	ns	2-8
t_{PZH} t_{PZL}	Output Enable Time	9.0	1.5	12.5	1.5	14.0	ns	2-11
t_{PHZ} t_{PLZ}	Output Disable Time	6.0	1.5	8.0	1.5	8.0	ns	2-11
t_{SU}	Set Up Time High or Low D_n to C_P	1.0	2.0		2.5		ns	2-10
t_H	Hold Time High or Low D_n to C_P	0.5	2.0		2.5		ns	2-10
t_w	C_P Pulse Width High or Low	4.0	7.0		7.0		ns	2-9
f_{max}	Maximum Clock Frequency				95		MHz	

Note 1: Minimum limits are guaranteed but not tested on propagation delays.

Capacitance $T_A = +25°C, f = 1.0$ MHz

Symbol	Parameter (Note 1)	Typ	Max	Unit	Condition
C_{IN}	Input Capacitance	6	10	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

Note 1: This parameter is measured at characterization but not tested.

C_{OUT} for 74FCT only.