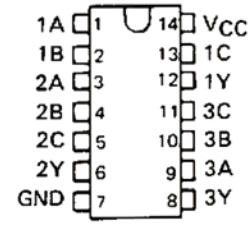
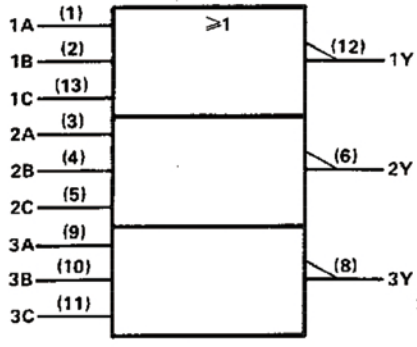
FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

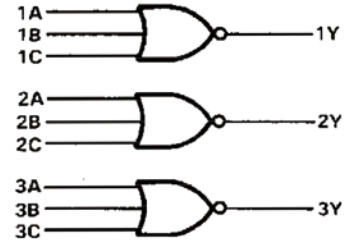
XD74LS27
(TOP VIEW)



logic symbol†



logic diagram

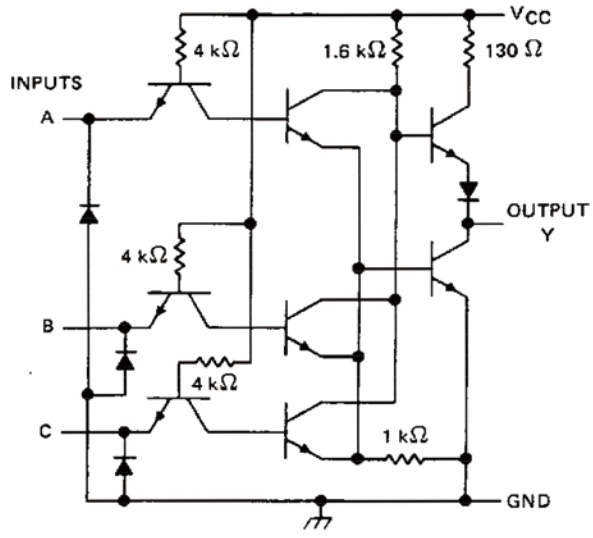


positive logic

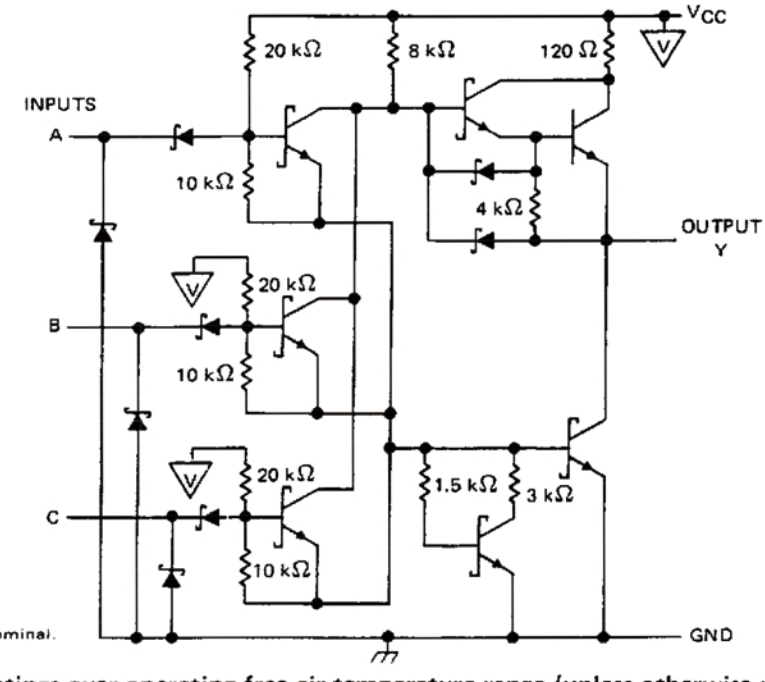
$$Y = \overline{A + B + C} \text{ or } Y = \overline{A} \cdot \overline{B} \cdot \overline{C}$$

schematics (each gate)

74LS27



74LS27



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: 74LS27 . . . . . 5.5 V
74LS27 . . . . . 7 V
Operating free-air temperature: 74LS27 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

	74LS27			UNIT
	MIN	NOM	MAX	
V_{CC} Supply voltage	4.75	5	5.25	V
V_{IH} High-level input voltage	2			V
V_{IL} Low-level input voltage			0.8	V
I_{OH} High-level output current			-0.4	mA
I_{OH} Low-level output current			8	mA
T_A Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

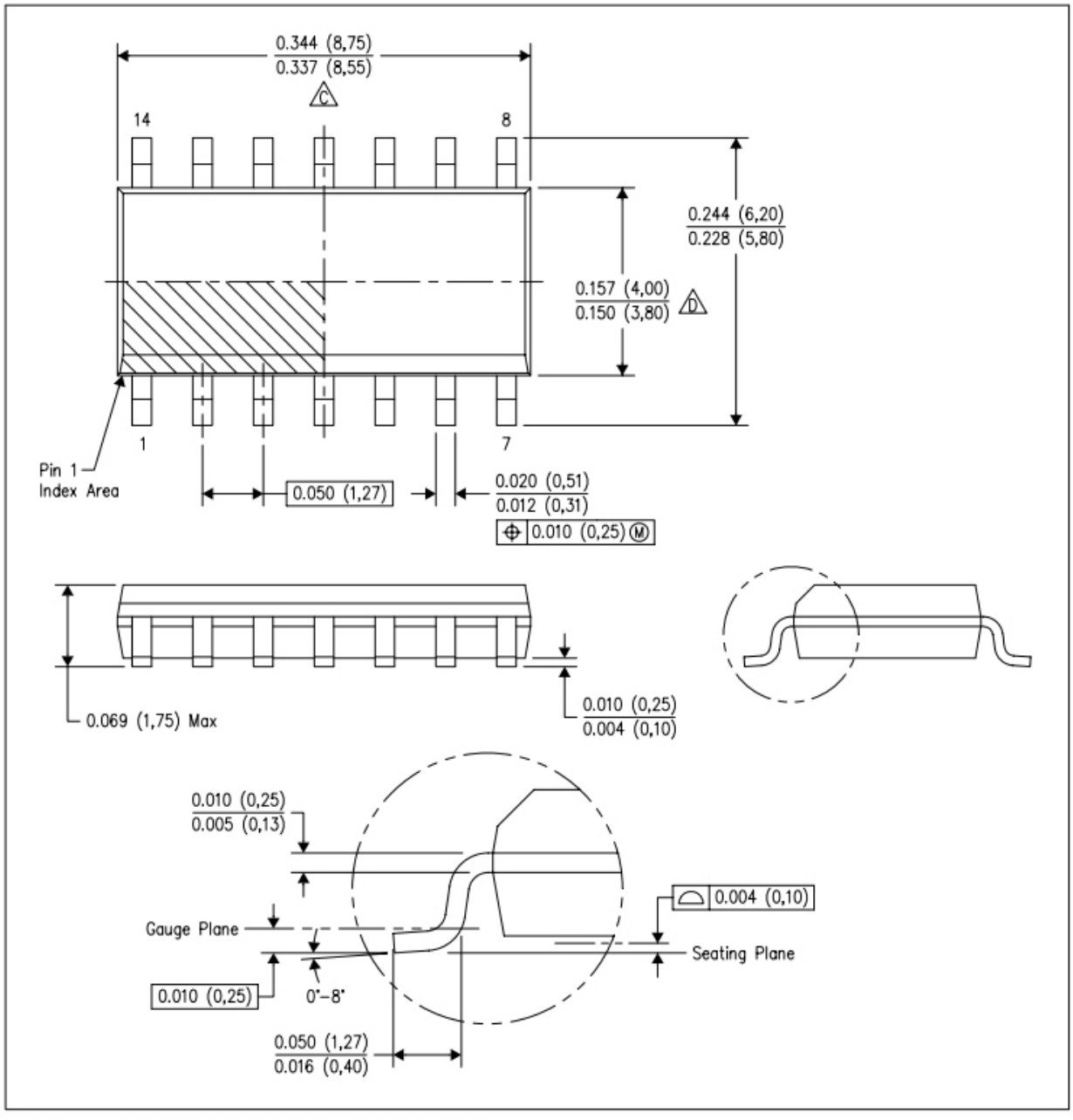
PARAMETER	TEST CONDITIONS†	74LS27			UNIT
		MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, V_{OH} - 18 mA			-1.5	V
V_{OH}	V_{CC} = MIN, V_{IL} =MAX, I_{OH} = -0.4mA	2.7	3.4		V
V_{OL}	V_{CC} = MIN, V_{IH} =2V, I_{OL} = 4mA		0.25	0.4	V
	V_{CC} = MIN, V_{IH} =2V, I_{OL} = 8mA		0.35	0.5	
I_I	V_{CC} = MIN, V_I =7V			0.1	mA
I_{IH}	V_{CC} = MIN, V_I =2.7V			20	μA
I_{IL}	V_{CC} = MIN, V_I =0.4V			-0.4	mA
I_{OS}§	V_{CC} = MIN,	-20		-100	mA
I_{CCH}	V_{CC} = MIN, V_I =0V		2	4	mA
I_{CCL}	V_{CC} = MIN, See Note 2		3.4	6.8	mA

switching characteristics, V_{CC} =5V, T_A =25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A,B or C	Y	R_L = 2 kΩ, C_L =15pF		10	15	ns
t_{PLH}					10	15	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE

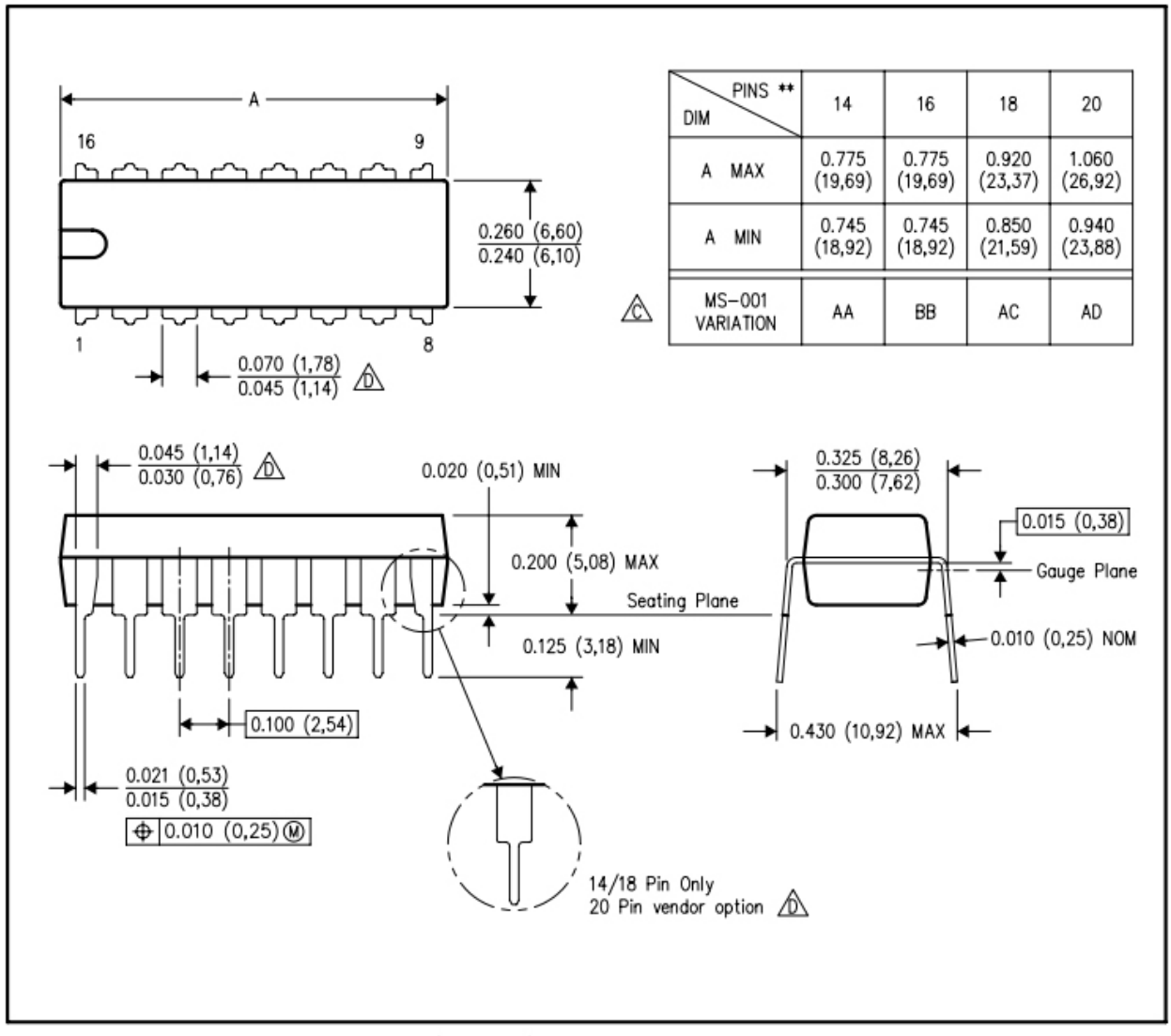


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C MS–001 VARIATION	AA	BB	AC	AD

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

以上信息仅供参考.如需帮助联系客服人员。谢谢 XINLUDA