

## P-Channel 100-V (D-S) MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)	$Q_g$ (Typ.)
- 100	0.200 at $V_{GS} = - 10$ V	- 3.0	13.2 nC
	0.230 at $V_{GS} = - 6$ V	- 2.4	

### FEATURES

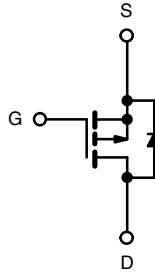
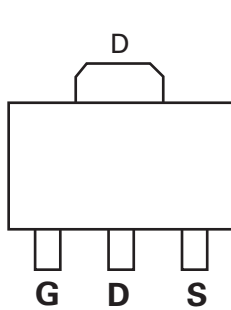
- TrenchFET® Power MOSFET
- 100%  $R_g$  and UIS Tested

### APPLICATIONS

- Active Clamp in Intermediate DC/DC Power Supplies
- H-Bridge High Side Switch for Lighting Application



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
Available



P-Channel MOSFET

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	- 100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 150$ °C)	$T_C = 25$ °C	- 3.0	A
	$T_C = 70$ °C	- 2.1	
	$T_A = 25$ °C	- 2 <sup>a, b</sup>	
	$T_A = 70$ °C	- 1.6 <sup>a, b</sup>	
Pulsed Drain Current	$I_{DM}$	- 12	A
Continuous Source-Drain Diode Current	$T_C = 25$ °C	- 4.9	
	$T_A = 25$ °C	- 2.5 <sup>a, b</sup>	
Avalanche Current	$I_{AS}$	- 15	
Single-Pulse Avalanche Energy	$E_{AS}$	11.25	mJ
Maximum Power Dissipation	$T_C = 25$ °C	6.5	W
	$T_C = 70$ °C	4.8	
	$T_A = 25$ °C	3.1 <sup>a, b</sup>	
	$T_A = 70$ °C	2 <sup>a, b</sup>	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150	°C

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b.  $t = 10$  s.

### THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a, b</sup>	$t \leq 10$ s	$R_{thJA}$	33	40	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	$R_{thJF}$	17	21	

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. Maximum under steady state conditions is 80 °C/W.

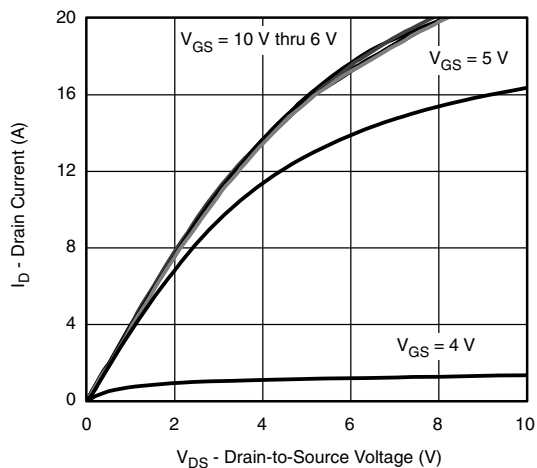
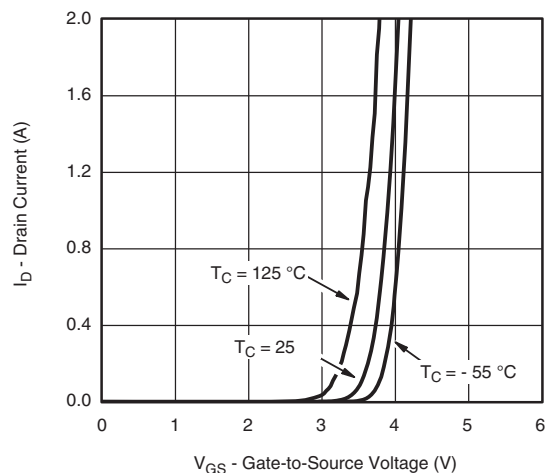
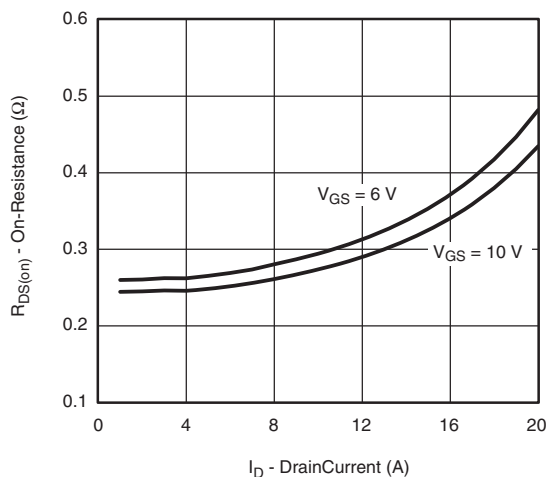
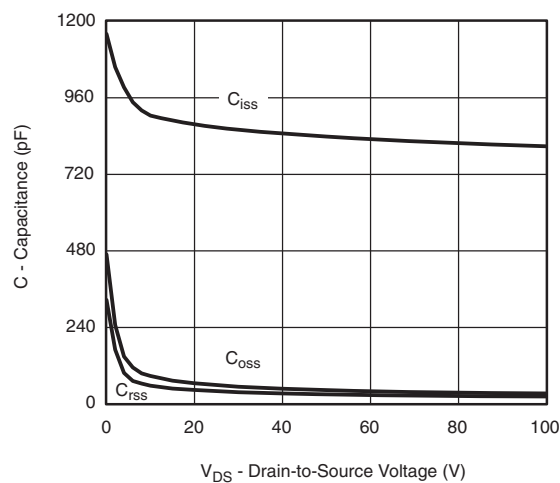
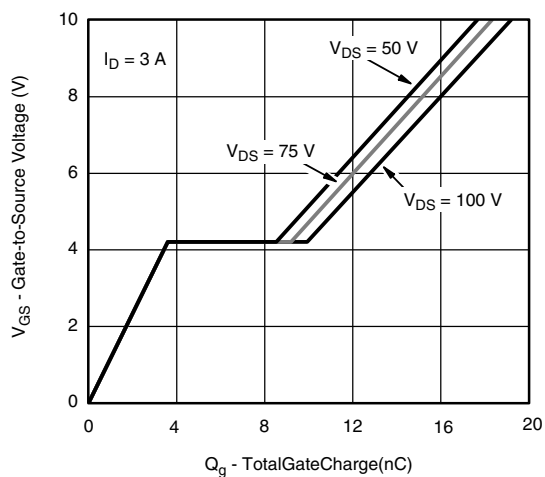
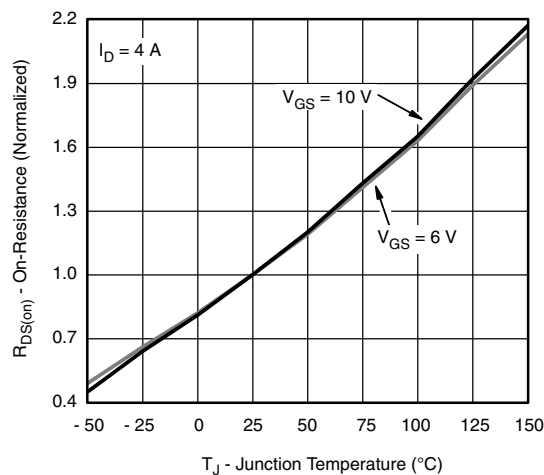
SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = - 250 μA	- 100			V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = - 250 μA		- 165		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>			- 6.6		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = - 250 μA	- 2		- 4	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = - 100 V, V <sub>GS</sub> = 0 V			- 1	μA
		V <sub>DS</sub> = - 100 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			- 10	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ - 5 V, V <sub>GS</sub> = - 10 V	- 8			A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 3 A		0.200		Ω
		V <sub>GS</sub> = - 6 V, I <sub>D</sub> = - 2 A		0.230		
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = - 15 V, I <sub>D</sub> = 3 A		12		S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = - 35 V, V <sub>GS</sub> = 0 V, f = 1 MHz		819		pF
Output Capacitance	C <sub>oss</sub>			51		
Reverse Transfer Capacitance	C <sub>rss</sub>			32		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = - 50 V, V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 3 A		17.5	32	nC
		V <sub>DS</sub> = - 50 V, V <sub>GS</sub> = - 6 V, I <sub>D</sub> = - 3 A		13.2	25	
Gate-Source Charge	Q <sub>gs</sub>			3.4		
Gate-Drain Charge	Q <sub>gd</sub>			6.4		
Gate Resistance	R <sub>g</sub>	f = 1 MHz		6.1	9.2	Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = - 50 V, R <sub>L</sub> = 25 Ω I <sub>D</sub> ≅ - 3 A, V <sub>GEN</sub> = - 6 V, R <sub>g</sub> = 1 Ω		10	20	ns
Rise Time	t <sub>r</sub>			55	95	
Turn-Off DelayTime	t <sub>d(off)</sub>			20	40	
Fall Time	t <sub>f</sub>			15	30	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = - 50 V, R <sub>L</sub> = 25 Ω I <sub>D</sub> ≅ - 3 A, V <sub>GEN</sub> = - 10 V, R <sub>g</sub> = 1 Ω		11	18	
Rise Time	t <sub>r</sub>			18	32	
Turn-Off DelayTime	t <sub>d(off)</sub>			32	58	
Fall Time	t <sub>f</sub>			20	35	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			- 13	A
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>				- 15	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = - 3 A		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = - 3 A, dI/dt = 100 A/μs, T <sub>J</sub> = 25 °C		65	90	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			180	270	nC
Reverse Recovery Fall Time	t <sub>a</sub>			45		ns
Reverse Recovery Rise Time	t <sub>b</sub>			20		

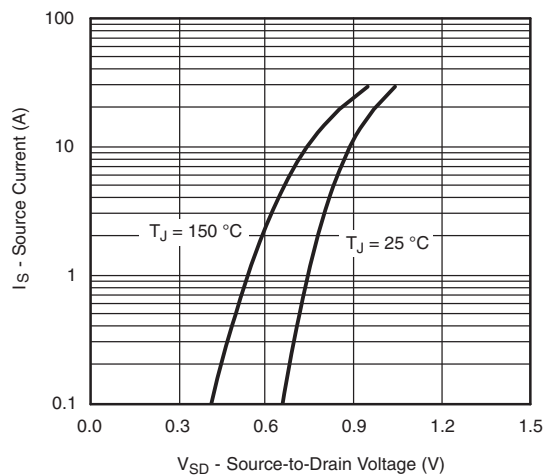
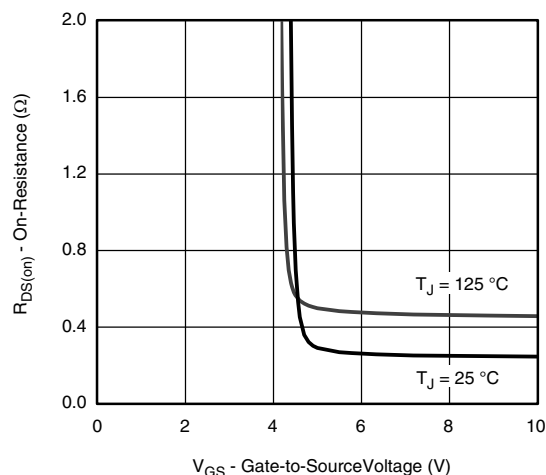
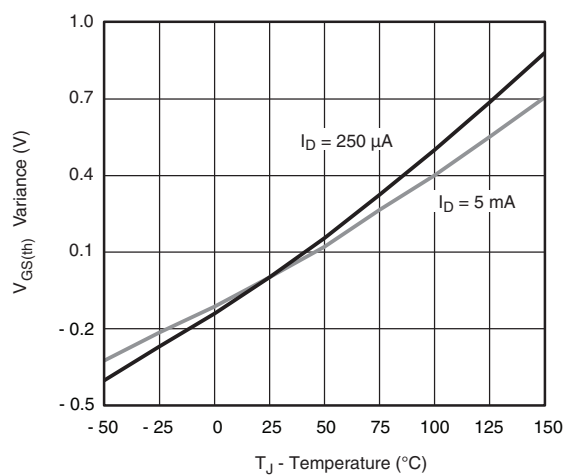
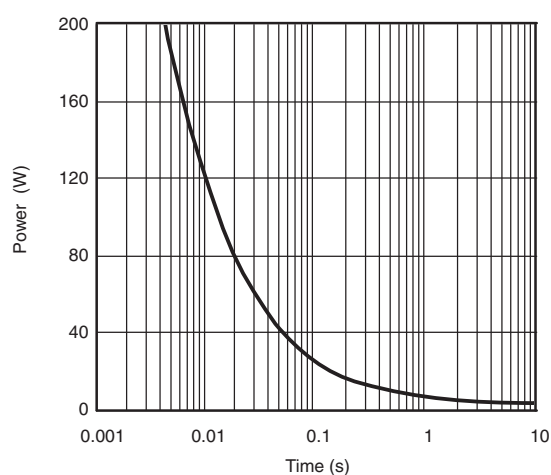
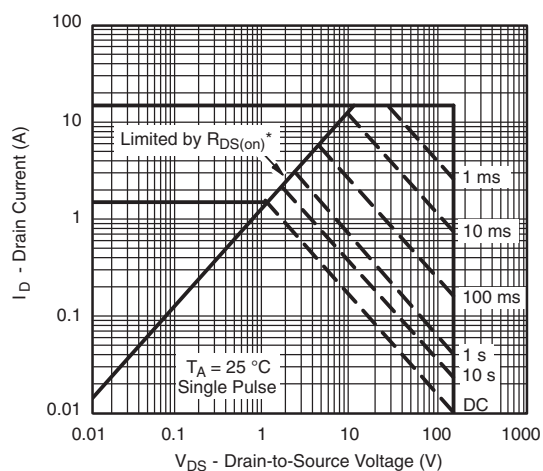
Notes:

a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

b. Guaranteed by design, not subject to production testing.

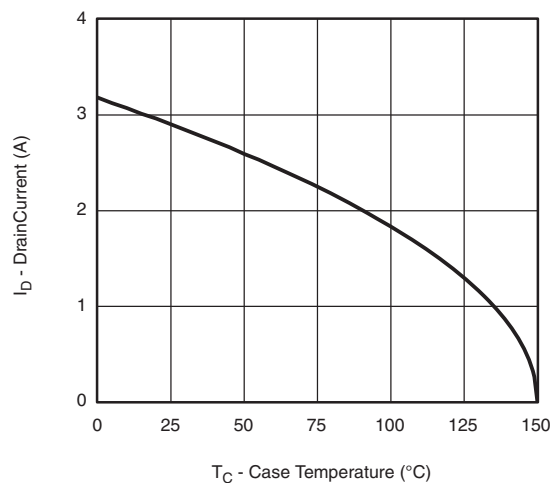
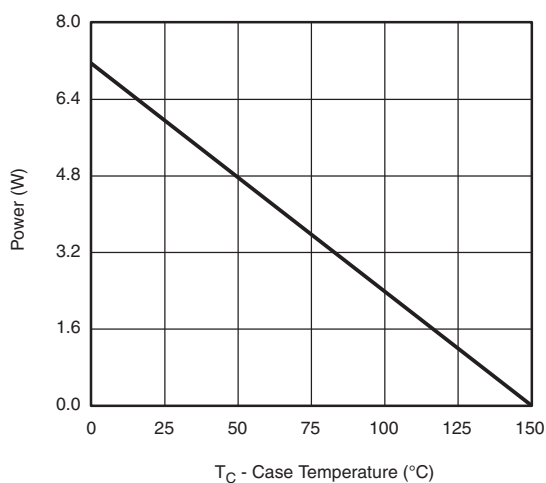
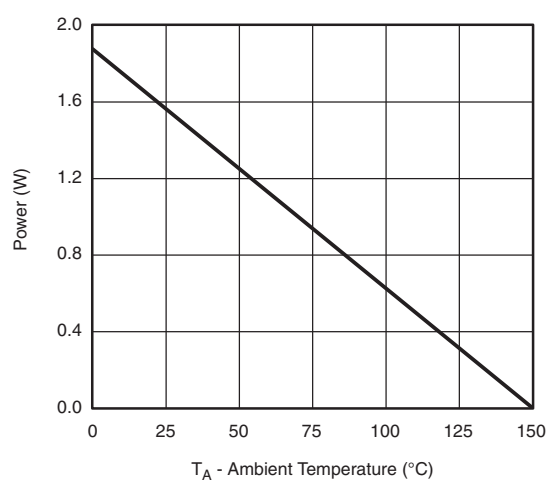
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Output Characteristics**

**Transfer Characteristics**

**On-Resistance vs. Drain Current and Gate Voltage**

**Capacitance**

**Gate Charge**

**On-Resistance vs. Junction Temperature**

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Source-Drain Diode Forward Voltage**

**On-Resistance vs. Gate-to-Source Voltage**

**Threshold Voltage**

**Single Pulse Power, Junction-to-Ambient**


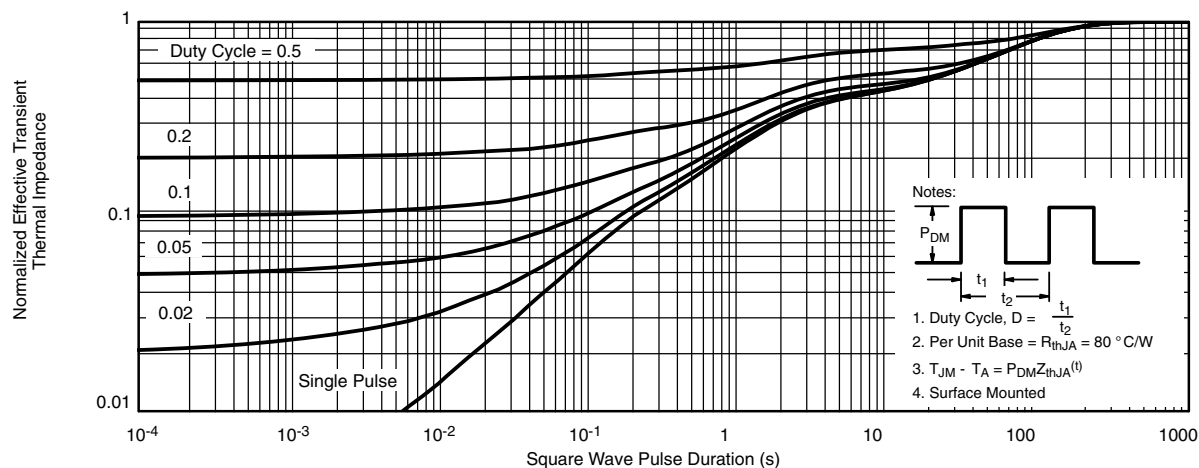
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

**Safe Operating Area, Junction-to-Ambient**

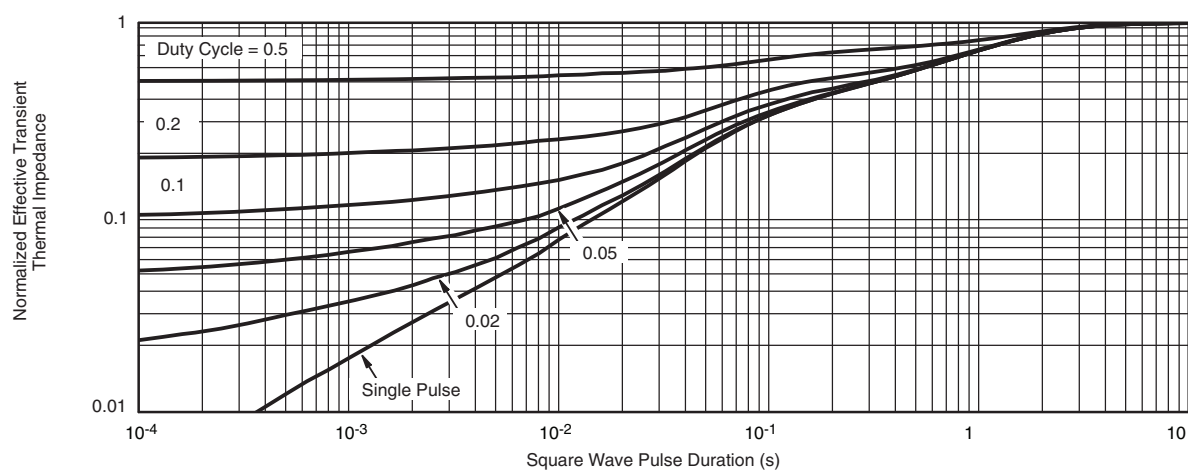
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Current Derating\***

**Power, Junction-to-Foot**

**Power, Junction-to-Ambient**

\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

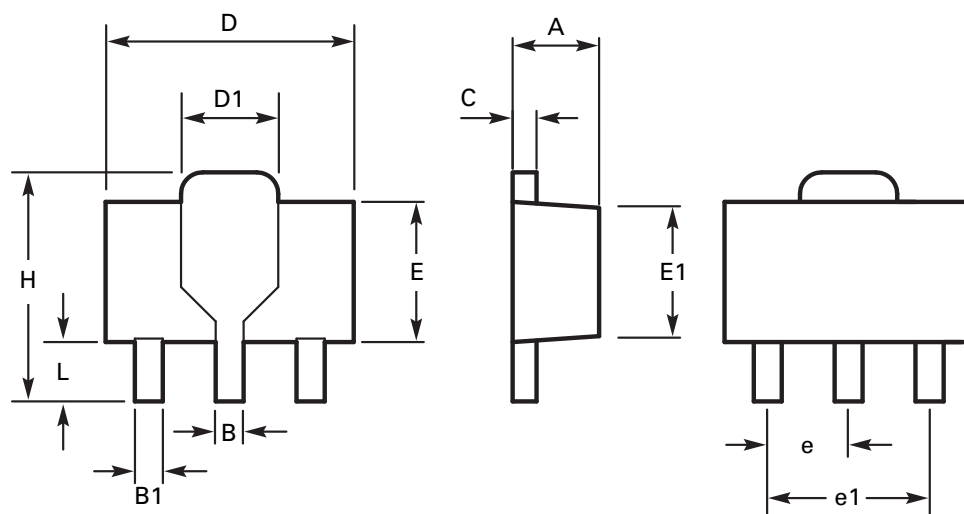


**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Foot**

### Package outline - SOT89



DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	1.40	1.60	0.550	0.630	E	2.29	2.60	0.090	0.102
B	0.44	0.56	0.017	0.022	E1	2.13	2.29	0.084	0.090
B1	0.36	0.48	0.014	0.019	e	1.50 BSC		0.059 BSC	
C	0.35	0.44	0.014	0.017	e1	3.00 BSC		0.118 BSC	
D	4.40	4.60	0.173	0.181	H	3.94	4.25	0.155	0.167
D1	1.62	1.83	0.064	0.072	L	0.89	1.20	0.035	0.047

**Note:** Controlling dimensions are in millimeters. Approximate dimensions are provided in inches

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