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Product Data Sheet

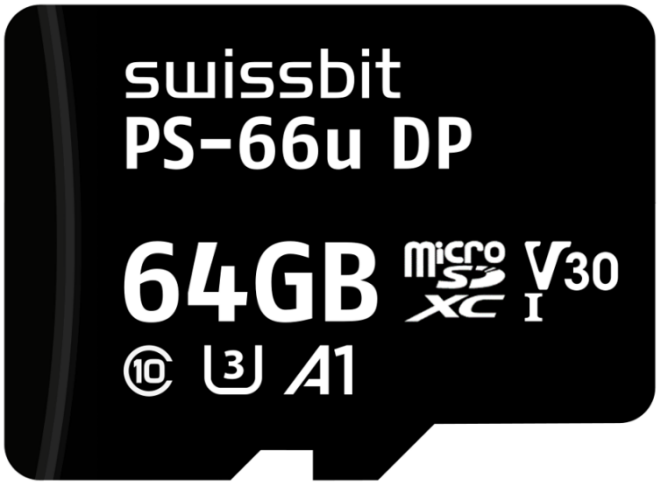
Secure Data Protection microSDHC / SDXC Memory Card

PS-66u DP Series

Data Protection, UHS-I Interface, pSLC

Industrial Temperature Grade

Date: March 21, 2024
Revision: 1.01



Made in Germany

Contents

PS-66u DP Series – Secure Data Protection microSDHC / SDXC Memory Card
16 GBytes up to 64 GBytes

1. Product Summary

- **Capacities:** 16 GBytes, 32 GBytes, 64 GBytes
- **Form Factor:** Standard microSD Memory card form factor – 15.0mm x 11.0mm x 0.7mm (1.0mm)
- **Compliance:** Fully compliant with SD Memory Card specification 6.10
  - SD/SDHC default/high speed mode and UHS supported
  - Speed class 10/U3/V30/A1 according SD6.10 specification
  - FAT32 or exFAT preformatted
- **Performance:**
  - SD Default speed
  - SD High speed
  - SD UHS-I
  - Read Performance: Sequential Read up to 90 MBytes/s, Random Read IOPS up to 1500
  - Write Performance: Sequential Write up to 75 MBytes/s, Random Write IOPS up to 1600
- **Operating Temperature Range**[1]**:**
  - Industrial: -40 °C to 85 °C
- **Storage Temperature Range:**
  - Industrial: -40 °C to 100 °C
- **Operating Voltage:** 2.7...3.6V normal operating voltage (Low-power CMOS technology)
- **Data Retention:** 10 Years @ Life Begin / 1 Year @ Life End
- **Humidity:** 85% RH @85°C 1000h
- **Electromagnetic Compatibility Test:** Radiated Emission; Radiated Immunity; Electrostatic Discharge
- **Officially tested and approved for Raspberry Pi**[2]
- **CmReady – Prepared for out-of-the-box use with Wibu-Systems CodeMeter (software protection & license management)**

[1] High Temperature storage without operation reduces the data retention, in operation the data will be refreshed, if data error issues were detected.

[2] Raspberry Pi Ltd has successfully tested and approved the PS-66u 16GB and 64GB (high endurance) microSD cards. The PS-66u (high endurance) 32GB microSD card uses identical controller and memory components and identical firmware & configuration.

2. Product Features

2.1 Security features

Table 1: Security Feature List PS-66u DP

	Access protection of data partition with configurable retry counter
	AES 256 bit flash memory encryption
	CD-ROM Emulation
	Private Partition
	Hidden Storage / OTP memory
	Fast crypto wipe option
	Implicit and replay safe secure authenticity and integrity check
	User PIN and administrator login
	Unique ID

2.2 Security use cases

Table 2: Use Cases List PS-66u DP

	Secure boot
	Counterfeit protection by authenticity and integrity check
	License control
	WORM functionality

2.3 Memory related features

Table 3: Memory related Features List PS-66u DP

	Description
	Wide Temperature Support
	ESD & EMI Safe
	Shock & Vibration
	Life Time Monitor
	Conformal Coating
	Power Loss Protected
	Wear Leveling
	Data Care Managed
	Read-Only Improved
	WAF Reduction

3. Ordering Information

Table 4: Available Part Numbers – Longevity

PS-66u DP (longevity)	
Capacity	**Part Number**
16 GBytes	SFSD016GN1PT1TB-I-5E-02P-SW4
32 GBytes	SFSD032GN1PT1TB-I-6F-02P-SW4
64 GBytes	SFSD064GN1PT1TB-I-7G-02P-SW4

Table 5: Available Part Numbers – High Endurance

PS-66u DP (high endurance)	
Capacity	**Part Number**
16 GBytes	SFSD016GN1PT1MT-I-5E-02P-SW4
32 GBytes	SFSD032GN1PT1MT-I-6F-02P-SW4
64 GBytes	SFSD064GN1PT1MT-I-7G-02P-SW4

4. Product Description

The microSD Memory Card is a small form factor non-volatile memory card which provides high capacity data storage. Its aim is to capture, retain and transport data, audio and images, facilitating the transfer of all types of digital information between a large variety of digital systems.
The card operates in two basic modes:

- SDHC/SDXC and UHS-I card modes
- SPI mode

The micro SD Memory Card also supports SD Default and High Speed mode with up to 50MHz clock frequency as well as UHS-I modes DDR50, SDR12/25/50 with up to 100MHz clock frequency.
The cards are compliant with

- SD Memory Card Specification Part 1, Physical layer Specification V6.10
- SD Memory card Specification Part 2, File System Specification V3.00
- MICRO SD Memory Card Addendum V4.20

The Card has an internal intelligent controller, which manages interface protocols, data storage and retrieval as well as hardware GCC Error Correction Code (ECC), defect handling, diagnostics and clock control.
The advanced wear leveling mechanism assures an equal usage of the Flash memory cells to extend the lifetime.
The controller performs control read operations and checks the consistency of the data. If an error of some bits is detected, the card refreshes all data in the flash cells to prevent data retention problems.

The card has a power-loss management feature to prevent data corruption after power-down.
The cards are RoHS compliant and lead-free.

Related Documentation

- Simplified specifications are available at (https://www.sdcard.org/)

If the data protection security features are activated, the erase command is blocked to prevent unexpected data loss. After deactivation of the data protection features the erase command is enabled again.

4.1 Performance Specifications

The PS-66u DP read/write sequential and random CDM performance benchmarks are detailed in Table 6 and Table 7.

Table 6: Read/Write Performance – Longevity

PS-66u DP (longevity)				
Capacity	**Sequential Read (MBPS)**	**Sequential Write (MBPS)**	**Random Read 4k (IOPS)**	**Random Write 4k (IOPS)**
16 GBytes	91,7	77,9	1540	1660
32 GBytes	91,6	78,1	1530	1660
64 GBytes	93,6	77,5	1430	1090

Table 7: Read/Write Performance – High Endurance

PS-66u DP (high endurance)				
Capacity	**Sequential Read (MBPS)**	**Sequential Write (MBPS)**	**Random Read 4k (IOPS)**	**Random Write 4k (IOPS)**
16 GBytes	47,6	46,3	1352	998
32 GBytes	47,6	46,3	1374	1000
64 GBytes	47,6	46,3	1562	1445

4.2 Environmental Specifications

4.2.1 Recommended Operating Conditions

The recommended operating conditions for the PS-66u DP are provided in Table 8.

Table 8: Recommended Operating Conditions

Parameter	Value
Industrial Operating Temperature	-40 °C to 85 °C

4.2.2 Recommended Storage Conditions

The recommended storage conditions are listed in Table 9.

Table 9: Recommended Storage Conditions

Parameter	Value
Industrial Storage Temperature	40 °C to 100 °C

4.2.3 Humidity & EMC

Table 10: Humidity and EMC

Parameter	Condition
Humidity (non-condensing)	85% RH @85°C 1000h
ESD	up to ±4 kV (contact discharge), according to IEC61000-4-2 and SDA, Human Body Model 150pF/ 330Ohm, on each contact pad, non-operating up to ±15 kV, (air discharge), according to IEC61000-4-2 and SDA, Human Body Model 150pF/ 330Ohm, isolated contact pad area, non-operating

4.2.4 Environmental conditions

Table 11: Environmental conditions

Parameter	Condition
UV light exposure	UV: 254nm, 15Ws/cm2 according to ISO7816-1
X-Ray	0.1 Gy 70keV to 140keV (ISO7816-1) according SDA
Durability	20,000 mating cycles
Drop Test	1.5m free fall
Bending / Torque	10N / 0.15Nm ±2.5° max
Mechanical Shock	1500G, 0.5ms, half sine wave ±xyz-axis, 4 pulses each
Vibration	50G, p-p, 20..2000Hz, sweep xyz-axis, 4 pulses each, non-operating, MIL-STD-883 M2007.3 Condition B

4.3 Regulatory Compliance

The PS-66u DP devices comply with the regulations / standards listed in Table 12.

Table 12: Regulatory Compliance

Abbreviation	Regulation/ Standard
EMC	CE – 2014/30/EU FCC – 47 CFR Part 15 UKCA – S.I. 2016 No. 1091 and S.I. 2012 No. 3032
RoHS	2011/65/EU with 2015/863/EU and 2017/2102/EU
REACh	1907/2006/EU and 207/2011/EU
WEEE	2012/19/EU

4.4 Physical dimensions

Table 13: Physical Dimensions

Physical Dimensions		Unit
Length	15.0±0.1	mm
Width	11.0±0.1	
Thickness (Max)	0.7±0.1	
Weight (Max Capacity)	0.4	g

4.5 Reliability

The Mean Time Between Failure (MTBF) is specified to exceed the value listed in Table 14. Data reliability with effective error tolerance and data retention at the beginning and end of life is also provided.

Table 14: Reliability

Parameter	Value
Data Retention at beginning @ 40°C	10 years
Data Retention at life end (max. endurance) @ 40°C	1 year
MTBF (at 25 °C)	> 3,000,000 hours

4.6 Endurance

Endurance represented as TeraBytes Written (TBW) is provided in the following tables.

Table 15: Endurance – Longevity variants [3, 4]

PS-66u DP (longevity)			
Capacity	TeraBytes Written (TBW) @ Seq. Write 128kB Operation	TeraBytes Written (TBW) @ Random Write 128kB Operation	TeraBytes Written (TBW) @ Random Write 4kB Operation
16 GBytes	483	266	67
32 GBytes	966	551	132
64 GBytes	1930	1110	257

[3] The specified TBW is valid, if the amount of data is spread evenly over at least 24 months. Higher daily data volume or frequent writing below 0°C reduces the specified TBW. The drive endurance limit, also called EOL or 0% remaining life, is defined as TBW or DWPD over the product's limited lifetime warranty period. TBW calculations refer to the JEDEC JESD218A and JESD219A standard for SSD device life and endurance measurement techniques if not otherwise specified.

[4] Sequential write 128kB simulates a continuous stream recording on a drive which has been preconditioned with a sequential write of the complete drive, Random Write 128KB or 4KB represent data logging applications with large or small block sizes.

Table 16: Endurance – High Endurance variants [5, 6]

PS-66u DP (high endurance)			
Capacity	**TeraBytes Written (TBW)** @ Seq. Write 128kB Operation	**TeraBytes Written (TBW)** @ Random Write 128kB Operation	**TeraBytes Written (TBW)** @ Random Write 4kB Operation
16 GBytes	1463	485	205
32 GBytes	2931	1048	414
64 GBytes	5871	2135	800

5. User density specification

Table 17: Capacity specification

Raw Capacity	Sectors	Total Addressable Bytes
16 GBytes	31,834,112	16,299,065,344
32 GBytes	62,333,952	31,914,983,424
64 GBytes	124,735,488	63,864,569,856

[5] The specified TBW is valid, if the amount of data is spread evenly over at least 24 months. Higher daily data volume or frequent writing below 0°C reduces the specified TBW. The drive endurance limit, also called EOL or 0% remaining life, is defined as TBW or DWPD over the product's limited lifetime warranty period. TBW calculations refer to the JEDEC JESD218A and JESD219A standard for SSD device life and endurance measurement techniques if not otherwise specified.

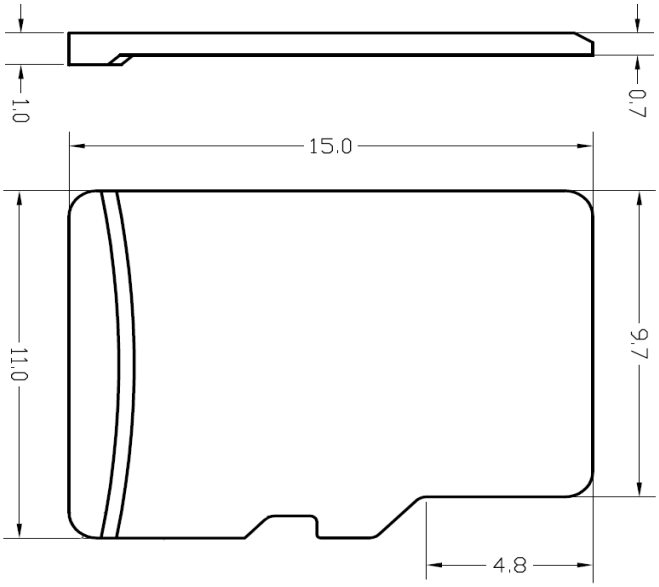
[6] Sequential write 128kB simulates a continuous stream recording on a drive which has been preconditioned with a sequential write of the complete drive, Random Write 128KB or 4KB represent data logging applications with large or small block sizes.

6. Card physical

6.1 Physical description

NOTE: The microSD Memory Card contains a single chip controller and Flash memory module(s). The controller interfaces with a host system allowing data to be written to and read from the Flash memory module(s).

Figure 1: Simplified mechanical dimensions



The dimensions and tolerances are according to the SD specification.

7. Electrical Interface

7.1 Electrical description

Figure 2: microSD Memory Card shape and interface (bottom view)

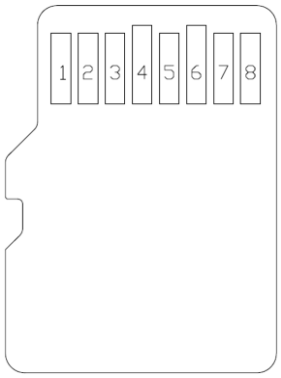


Table 18: Pad Assignment – SD Mode

Pin	Signal Name	Type[7]	Description
1	DAT2[8]	I/O/PP	Data Line [Bit 2]
2	CD/DAT3[9]	I/O/PP[10]	Card Detect/ Data Line [Bit 3]
3	CMD	PP	Command/Response
4	VDD	S	Supply voltage
5	CLK	I	Clock
6	VSS	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit 0]
8	DAT1[11]	I/O/PP	Data Line [Bit 1]

Table 19: Pad Assignment – SPI Mode

Pin	Signal Name	Type[7]	Description
1	RSV		
2	CS	I[10]	Chip Select (neg true)
3	DI	I	Data In
4	VDD	S	Supply voltage
5	SCLK	I	Clock
6	VSS	S	Supply voltage ground
7	DO	O/PP	Data Out
8	RSV		

[7] S: power supply; I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers
[8] DAT2 line may be used as Read Wait signal in SDIO mode (refer to "SDIO Card Specification" for further details).
[9] The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used.
[10] At power up this line has a 50k0hm pull up enabled in the card. This resistor serves two functions Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. The host should disconnect this pull-up during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command.
[11] DAT1 line may be used as Interrupt Output (from the Card) in SDIO mode during all the times that it is not in use for data transfer operations (refer to "SDIO Card Specification" for further details).

7.2 Power up / Power down behavior and reset

7.2.1 Power up

When the voltage is ramped up the controller is ready (internal reset pin released) if the voltage reaches 1.65V. The host can start with communication 1ms after 2.7V is reached according the SDA specification. That should perform 74 clock cycles and start with the sequence CMD0, CMD8, ACMD41 until card is ready as described in the SD specification 3.01.

7.2.2 Power down

When the power falls below 2.6V the controller stops the communication to the flash, but enables the flash to finish a started flash program operation (if voltage drop is not fast).

7.2.3 Power drop

If the voltage drops below 2.6V and rises again, the card preforms a reset. The card must be initialized like after a power on.

7.2.4 Operation below minimum voltage

If the card initialization is performed below the specified voltage of 2.7V, the card may be detected as 1MB card with no useful data. In this case the host should power off and on the card and start initialization above 2.7V.

7.3 DC characteristics

Measurements are not recommended operation conditions unless otherwise specified.

Table 20: DC characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I_{DD}	Operating Current Read (Longevity variants)		100	100	mA	@ 25°C
I_{DD}	Operating Current Write (Longevity variants)		95	100	mA	@ 25°C
I_{DD}	Operating Current Read (High Endurance variants)		80	85	mA	@ 25°C
I_{DD}	Operating Current Write (High Endurance variants)		80	90	mA	@ 25°C
I_{DD}	Pre-initialization Standby Current		5	15	mA	@ 25°C
I_{DD}	Post-initialization Standby Current[12]		10	12	mA	@ 25°C
I_{DD}	Post-initialization Standby Current[12]		10	12	mA	@ 85°C
I_{LI}	Input Leakage Current	-2		2	µA	without pull up R
I_{LO}	Output Leakage Current	-2		2	µA	without pull up R

Table 21: microSD Memory Card recommended operation conditions

Symbol	Parameter		Min	Typ	Max	Unit
V_{DD}	Supply voltage	Normal operating status	2.7	3.3	3.6	V
-	Power Up Time (from 0V to VDD min)				250	ms

7.4 Signal loading

According to SD specification

[12] Before auto read the idle current is larger than the typical idle current after auto read

7.5 AC characteristics

7.5.1 Default speed mode (0-25MHz)

According to SD specification

7.5.2 High speed mode (0-50MHz)

According to SD specification

7.5.3 UHS modes

UHS modes were driven with a signal level of 1.8V.
The cards support following UHS-I modes:

Table 22: Supported UHS-I modes

Host request	Card Modes (to select by host)	Max. Burst MB/s	Max. Clock frequency MHz
SDR12	SDR12	up to 12.5	up to 25
SDR25	SDR12, SDR25	up to 25	up to 50
SDR50	SDR12, SDR25, SDR50	up to 50	up to 100
DDR50	SDR12, SDR25, SDR50, DDR50	up to 50	50 (rising and falling edge)
SDR104	SDR12, SDR25, SDR50, SDR104[13], DDR50	up to 104[13]	up to 208[13]

According to the SD specification

[13] SDR104 / 104 MB/s / 208MHz supported on PS-66 DP (longevity) only. PS-66 DP (high endurance) supports up to SDR50 / 50 MB/s / 100MHz.

8. Host access specification

The following chapters summarize how the host accesses the card:

- Chapter 8.1 summarizes the SD and SPI buses.
- Chapter 8.2 summarizes the registers.

8.1 SD and SPI Bus Modes

The card supports SD and the SPI Bus modes. Application can chose either one of the modes. Mode selection is transparent to the host. The card automatically detects the mode of the reset command and will expect all further communication to be in the same communication mode. The SD mode uses a 4-bit high performance data transfer, and the SPI mode provides compatible interface to MMC host systems with little redesign, but with a lower performance.

8.1.1 SD Bus Mode Protocol

The SD Bus mode has a single master (host) and multiple slaves (cards) synchronous topology. Clock, power, and ground signals are common to all cards. After power up, the SD Bus mode uses DAT0 only; after initialization, the host can change the cards' bus width from 1 bit (DAT0) to 4 bits (DAT0-DAT3). In high speed mode, only one card can be connected to the bus.
Communication over the SD bus is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit.

- Command: a command is a token which starts an operation. A command is sent from the host either to a single card (addressed command) or to all connected cards (broadcast command). A command is transferred serially on the CMD line.
- Response: a response is a token which is sent from an addressed card, or (synchronously) from all connected cards, to the host as an answer to a previously received command. A response is transferred serially on the CMD line.
- Data: data can be transferred from the card to the host or vice versa. Data is transferred via the data lines.

8.1.2 SPI Bus Mode Protocol

The Serial Parallel Interface (SPI) Bus is a general purpose synchronous serial interface. The SPI mode consists of a secondary communication protocol. The interface is selected during the first reset command after power up (CMD0) and it cannot be changed once the card is powered on.
While the SD channel is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit, the SPI channel is byte oriented. Every command or data block is built of 8-bit bytes and is byte aligned to the CS signal.
The card identification and addressing methods are replaced by a hardware Chip Select (CS) signal. There are no broadcast commands. For every command, a card (slave) is selected by asserting (active low) the CS signal. The CS signal must be continuously active for the duration of the SPI transaction (command, response and data). The only exception occurs during card programming, when the host can de-assert the CS signal without affecting the programming process.
The bidirectional CMD and DAT lines are replaced by unidirectional dataIn and data0ut signals.

Table 23: SPI Bus signals

Signal	Description
/CS	Host to card chip select
CLK	Host to card clock signal
Data In	Host to card data signal
Data Out	Card to host data signal
Vdd, Vss	Power and ground

8.1.3 Mode Selection

The microSD Memory Card wakes up in the SD mode. It will enter SPI mode if the CS signal is asserted (negative) during the reception of the reset command (CMD0) and the card is in idle_state. If the card recognizes that the SD mode is required it will not respond to the command and remain in the SD mode.
If SPI mode is required the card will switch to SPI and respond with the SPI mode R1 response.
The only way to return to the SD mode is by entering the power cycle. In SPI mode the microSD Memory Card protocol state machine is not observed. All the SD Memory Card commands supported in SPI mode are always available.
During the initialization sequence, if the host gets Illegal Command indication for ACMD41 sent to the card, it may assume that the card is Multimedia Card. In that case it should restart the card as Multimedia Card using CMD0 and CMD1.

8.2 Card registers

The microSD Memory Card has the following registers.

Table 24: microSD Memory Card registers

Register name	Bit width	Description	Function
CID	128	Card Identification information	This register contains the card identification information used during the Card Identification phase.
OCR	32	Operation Conditions Registers	This register describes the operating voltage range and contains the status bit in the power supply.
CSD	128	Card specific information	This register provides information on how to access the card content. Some fields of this register are writeable by PROGRAM_CSD (CMD27).
SCR	64	SD Memory Card's Special features	This register provides information on special features.
RCA[14]	16	Relative Card Address	This register carries the card address is SD Card mode.
SSR	512	SD Status	information about the card proprietary features and vendor specific life time information

Table 25: CID register

Register name	Bit width	Description	Function
MID	8	Manufacture ID	0x5d
OID	16	OEM/Application ID	0x5053
PNM	40	Product Name	e.g." N1DP7"
PRV	8	Product Revision	0xgg
PSN	32	Product Serial Number	xxxxxxxx
–	4	Reserved	0x0
MDT	12	Manufacture Date	0xyym
CRC	7	Check sum of CID contents	chksum
–	1	Not used; always=1	1

[14] RCA register is not available in SPI mode

Table 26: OCR register

OCR bit positon	VDD voltage windows	Typ. value	OCR bit position	VDD voltage window	Typ. value
0-3	Reserved	0	15	2.7-2.8	1
4	1.6-1.7	0	16	2.8-2.9	1
5	1.7-1.8	0	17	2.9-3.0	1
6	1.8-1.9	0	18	3.0-3.1	1
7	1.9-2.0	0	19	3.1-3.2	1
8	2.0-2.1	0	20	3.2-3.3	1
9	2.1-2.2	0	21	3.3-3.4	1
10	2.2-2.3	0	22	3.4-3.5	1
11	2.3-2.4	0	23	3.5-3.6	1
12	2.4-2.5	0	24	Switching to 1.8V accepted	1
13	2.5-2.6	0	25-29	Reserved	
14	2.6-2.7	0	30	Card Capacity Status (CCS)	*[15]
			31	0=busy; 1=ready	*[16]

[15] This bit is valid only when the card power up status bit is set
[16] This bit is set to LOW if the card has not finished the power up routine

Table 27: CSD register

Register name	Bits	Bit width	Description	Typ. Value
CSD_STRUCTURE	127:126	2	CSD structure	01
–	125:120	6	Reserved	00000
TAAC	119:112	8	Data read access time 1	00001110
NSAC	111:104	8	Data read access time 2 (CLK cycle)	00000000
TRAN_SPEED	103:96	8	Data transfer rate	00110010 Default speed or other values
CCC	95:84	12	Card command classes	010110110101
READ_BL_LEN	83:80	4	Read data block length	1001
READ_BL_PARTIAL	79	1	Partial blocks for read allowed	0
WRITE_BLK_MISALIGN	78	1	Write block misalignment	0
READ_BLK_MISALIGN	77	1	Read block misalignment	0
DSR_IMP	76	1	DSR implemented	0
–	75:70	6	Reserved	000000
C_SIZE	69:48	22	Device_SIZE	xxx[17]
–	47	1	Reserved	0
ERASE_BLK_EN	46	1	Erase single block enable	1
SECTOR_SIZE	45:39	7	Erase sector size	1111111
WP_GRP_SIZE	38:32	7	Write protect group size	0000000
WP_GRP_ENABLE	31	1	Write protect group enable	0
–	30:29	2	Reserved	00
R2W_FACTOR	28:26	3	Write speed factor	010
WRITE_BL_LEN	25:22	4	Write data block length	1001
WRITE_BL_PARTIAL	21	1	Partial blocks for write allowed	0
–	20:16	5	Reserved	00000
FILE_FORMAT_GRP	15	1	File format group	0 W(1)
COPY	14	1	Copy flag	0 W(1)
PERM_WRITE_PROTECT	13	1	Permanent write protection	0 W(1)
TMP_WRITE_PROTECT	12	1	Temporary write protection	0 W
FILE_FORMAT	11:10	2	File format	00 W(1)
–	9:8	2	Reserved	00 W
CRC	7:1	7	Checksum of CSD contents	xxxxxxx W
–	0	1	Always=1	1

Memory capacity = (C_SIZE+1) * 512kByte

W value can be changed with CMD27 (PROGRAM_CSD)
W(1) value can be changed ONCE with CMD27 (PROGRAM_CSD)

[17] Drive size and block sizes vary with card capacity

Table 28: SCR register

Field	Bits	Bit width	Typ. value	Remark
SCR_STRUCTURE	63:60	4	0000	SCR 1.01...3.00
SD_SPEC	59:56	4	0010	SD 2.00 or higher
DATA_STAT_AFTER_ERASE	55	1	1	data are 0xFF after erase
SD_SECURITY	54:52	3	011 100	2.00 (SDHC) 3.xx (SDXC)
SD_BUS_WIDTHS	51:48	4	0101	1 or 4 bit
SD_SPEC3	47	1	1	yes→ SD3.0X
EX_SECURITY	46:43	4	0000	no extended security
SD_SPEC4	42:42	1	1	yes
SD_SPECX	41:38	4	1	Version 5.XX
Reserved	37:34	4	0	
CMD_SUPPORT	33:32	2	11	CMD23 and CMD20 supported
Reserved	31:0	32	0	0

Table 29: RCA register

Field	Bits	Bit width
RCA	16	0x0000[18]

Table 30: SSR register

Field	Bits	Bit width	Typ. value	Remark
Data bus width	511:510	2	0x2[19]	4 bit width
Secured mode	509:509	1	0x0	not secured
Reserved for security	508:502	7	0x00	-
Reserved	501:496	6	0x00	-
SD card type	495:480	16	0x0000	Regular SD
Size protected area	479:448	32	0x02000000 0x03000000 0x04000000 0x05000000 0x08000000	32MiB for 4GB card 48MiB for 8GB card 64MiB for 16GB card 80MiB for 32GB card 128MiB for 64GB card
Speed class	447:440	8	0x04	Class 10
Move performance	439:432	8	0x05	5 MB/s
Allocation unit size	431:428	4	0x9	4 MiB
Reserved	427:424	4	0x0	
Erase unit size	423:408	16	0x0001	1 AU
Erase unit timeout	407:402	6	0x01	1 second
Erase unit offset	401:400	2	0x1	1 second
UHS mode Speed Grade	399:396	4	0x3	UHS Grade3
Allocation unit size in UHS mode	395:392	4	0x9	4 MiB
Video Speed Class	391:384	8	0x1e	Video Speed Class 30
Reserved	383:378	6	0x0	
AU size for Video Speed Class	377:368	10	0x8	8 MiB
Suspension Address	367:346	22	0x0	
Reserved	345:340	6	0x0	
Application Performance Class	339:336	4	1	Class A1
Performance Enhancement	335:328	8	0x0	

[18] After initialization the card can change the RCA register
[19] Value change in operation

Field	Bits	Bit width	Typ. value	Remark
Reserved	327:314	14	0x0	
Discard support	313:313	1	0x0	Not supported
Full User Area Logical Erase Support	312:312	1	0x0	Not supported
Data structure version identifier, currently 1	311:304	8	0x01	version 1
Number of manufacturer marked defect blocks	303:288	16	0x0030 0x0060 0x00C0	48 initial BB (4GB to 16GB) 96 initial BB (32GB) 192 initial BB (64GB)
Number of initial spare blocks (worst chip)	287:272	16	0x0431 0x0357 0x01A2 0x037C 0x0709	1073 spare blocks (4GB) 855 spare blocks (8GB) 418 spare blocks (16GB) 892 spare blocks (32GB) 1801 spare blocks (64GB)
Number of initial spare blocks (sum over all chips)	271:256	16	0x0431 0x0357 0x01A2 0x037C 0x0709	1073 spare blocks (4GB) 855 spare blocks (8GB) 418 spare blocks (16GB) 892 spare blocks (32GB) 1801 spare blocks (64GB)
Percentage of remaining spare blocks (worst chip)	255:248	8	0x64[19]	100%
Percentage of remaining spare blocks (all chips)	247:240	8	0x64[19]	100%
Number of uncorrectable ECC errors (not including ECC errors during startup)	239:224	16	0x0000[19]	0 uncorrectable errors
Number of correctable ECC errors (not including ECC errors during startup)	223:192	32	0x0045074b[19]	4523851 correctable ECC errors
Lowest wear level class	191:176	16	0x0000[19]	0
Highest wear level class	175:160	16	0x0000[19]	0
Wear level threshold	159:144	16	0x01ff	511 block erases per WL class
Total number of block erases	143:96	48	0x00...1ff0[19]	8176 block erase commands
Number of flash blocks, in units of 256 blocks	95:80	16	0x0005 0x000A 0x0015	1028 flash blocks (4GB to 16GB) 2560 flash blocks (32GB) 5376 flash blocks (64GB)
Maximum flash block erase count target, in wear level class units	79:64	16	0x0075	Flash endurance 117 WL classes (59904 erases)
Power on count	63:32	32	0x00000003[19]	3x power on
Firmware version	31:0	32	0xYYMMDDXX	Firmware Version

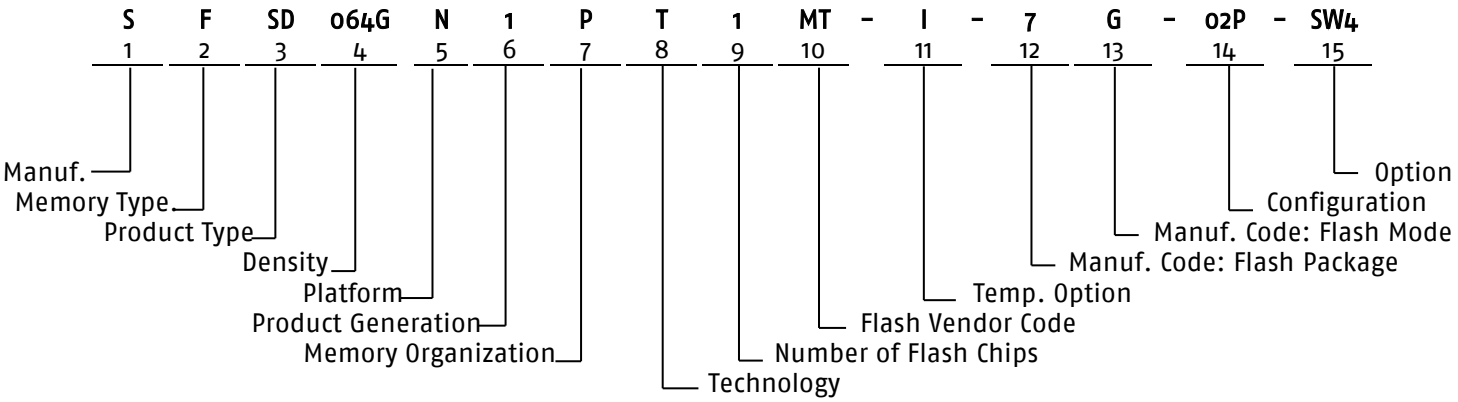
Bit 311:0 are vendor specific, example values in the table

9. Life Time Monitoring

The products support life time monitoring with a vendor specific SD command CMD56 with argument 0x53420001 (read transfer). CMD56 follows the SD protocol specification and returns 512 bytes of data.
All multi-byte values are in big endian order (most significant byte first).

Field	Bytes	Byte width	Remark
Unique ID	0:7	8	53 77 69 73 73 62 69 74 «Swissbit» in ASCII
Reserved	8:15	8	All 0x00
SD CID Register	16:31	16	See chapter 8.2
Firmware Revision	32:47	16	ASCII Null-Terminated
User Area Rated Cycles	48:51	4	
User Area Max. Cycle Count	52:55	4	
User Area Total Cycle Count	56:59	4	
User Area Average Cycle Count	60:63	4	
Reserved	64:67	4	All 0x00
System Area Max. Cycle Count	68:71	4	
System Area Total Cycle Count	72:75	4	
System Area Average Cycle Count	76:79	4	
Remaining Card Lifetime Percent (user area)	80:80	1	
Reserved	81:85	5	All 0x00
Current SD Card Speed Mode	86:86	1	0x00: Default Speed 0x01: High Speed 0x10: SDR12 0x11: SDR25 0x12: SDR50 0x14: DDR50 0x18: SDR104
Current SD Card Bus Width	87:87	1	0x00: 1 bit width 0x10: 4 bit width
Runtime Bad Blocks User Area	96:99	4	
Runtime Bad Blocks System Area	100:103	4	
Refresh Count User Area	104:107	4	
Refresh Count System Area	108:111	4	
Host Interface CRC count	112:115	4	
Power Cycle Counter	116:119	4	
Reserved	120:511	392	

10. Part Number Decoder



10.1 Manufacturer

Swissbit code	S

10.2 Memory Type

Flash	F

10.3 Product Type

SD Interface	SD

10.4 Density

16 GBytes	016G
32 GBytes	032G
64 GBytes	064G

10.5 Platform

microSD Memory Card	N

10.6 Product Generation

Generation	1

10.7 Memory Organization

Security Product x8	P

10.8 Technology

SD Memory Card controller (PS-6x platform)	T

10.9 Channels

1 Flash channel	1

10.10 Flash Code

Toshiba / Kioxia Gen3	T0
Toshiba / Kioxia Gen5	TB
Micron Technology	MT

10.11 Temperature Option

Industrial Temperature Range: -40 °C to 85 °C	I

10.12 Die Classification

3D TLC MONO (single die package)	5
3D TLC DDP (dual die package)	6
3D TLC QDP (quad die package)	7

10.13 Pin Mode

Single nCE and Single R/nB	E
Dual nCE and Dual R/nB	F
Quad nCE and Quad R/nB	G

10.14 Drive configuration XYZ

X = Smart Card Controller

Smart Card Controller	X
No Smart Card Controller	0

Y = Firmware Extension

FW Extension	Y
Data Protection mode	2

Z = Feature

Feature	Z
Standard	0
pSLC	P

10.15 Option

Swissbit/Data Protection	SW4
Customer specific	XXX

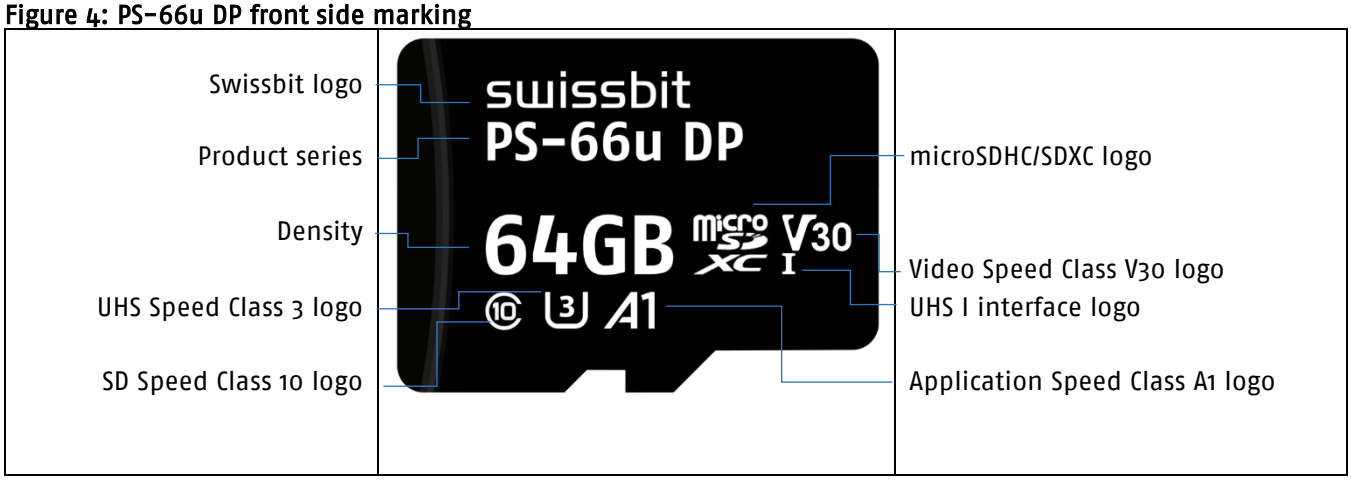
11. Marking Specification

11.1 Top View

Figure 3: PS-66u DP top view

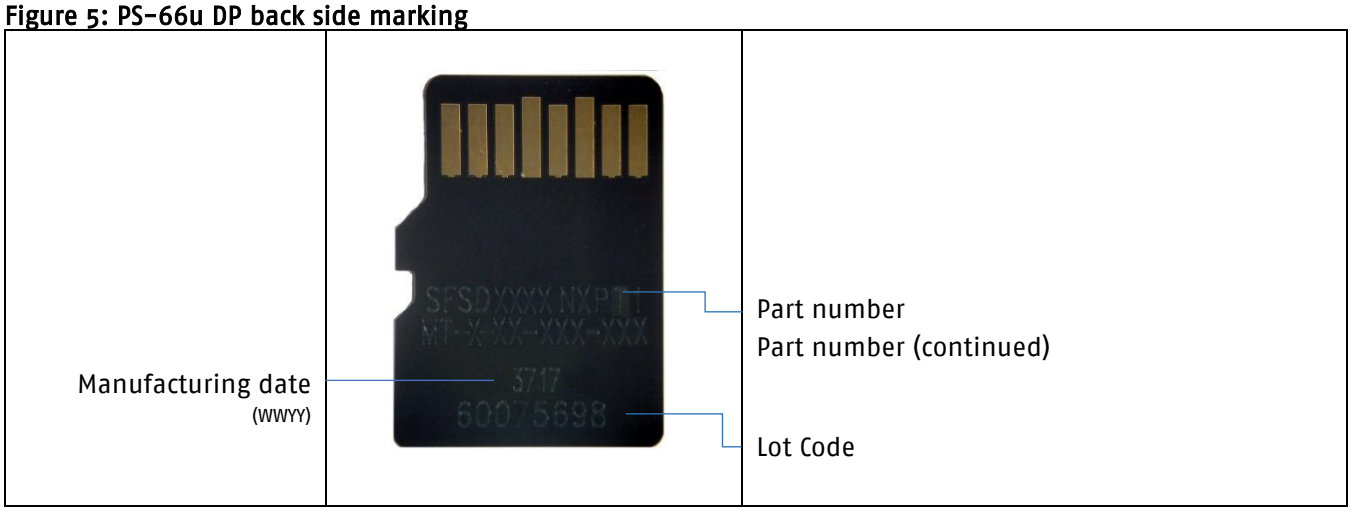
11.2 Front side marking

Figure 4: PS-66u DP front side marking



11.3 Back side marking

Figure 5: PS-66u DP back side marking



12. Revision History

Table 31: Document Revision History

Date	Revision	Description	Revision Details
14-Nov-2023	1.00	Initial release	Doc.req.no. 6692
21-Mar-2024	1.01	Added "Longevity" part numbers in ch. 3, ch. 4.1, ch. 4.6, ch. 7.3; updated table 14 (life end endurance). Added WIBU CmReady certification.	Doc.req.no. 6973