National Semiconductor

DS3890 BTL Octal Trapezoidal Driver
DS3892 BTL Octal TRI-STATE® Receiver

General Description

The DS3890 and DS3898 are designed specifically to overcome problems associated with driving densely populated backplanes. These products provide significant improvement in both speed and data integrity in comparison to conventional bus drivers and receivers. Their low output capacitance, low voltage swing and noise immunity features make them ideal for driving low impedance busses with minimum power dissipation.

The DS3890 features an open collector outputs that generate precise trapezoidal waveforms with typical rise and fall times of 6 ns which are relatively independent of capacitive loading conditions. These controlled output characteristics significantly reduce noise coupling to adjacent lines.

To minimize bus loading, the DS3890 also features a schottky diode in series with the open collector outputs that isolates the driver output capacitance in the disabled state. With this type of configuration the output low voltage is typically "1V". The output high level is intended to be 2 volts. This is achieved by terminating the bus with a pull up resistor. Both devices can drive an equivalent DC load of 18.5Ω (or greater) in the defined configuration.

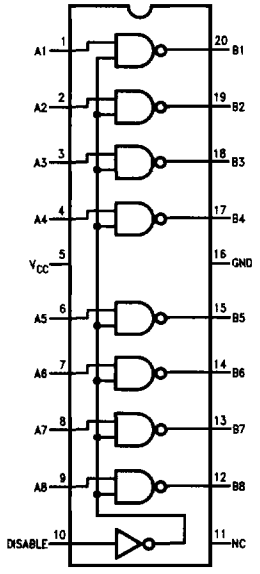
(General Description to be continued)

Features

- Driver output capacitance less than 5 pF
- 1 volt bus signal reduces power consumption
- Trapezoidal driver waveforms (t_r, t_f, typically 6 ns) reduces noise coupling to adjacent lines
- Precise receiver threshold track the bus logic high level to maximize noise immunity in both logic high ahd low states
- Open collector driver output allows wire-or connection
- Advanced low power schottky technology
- Glitch free power up/down protection
- TTL compatible driver and control inputs and receiver output
- BTL compatible

Logic and Connection Diagrams

DS3890 Octal Trapezoidal Driver



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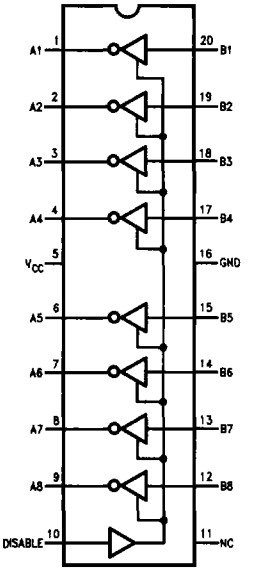
DS3892 Octal TRI-STATE Receiver



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Order Numbers DS3892M, DS3890N or DS3892N
See NS Package Number M20B or N20A

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	6V
Control Input Voltage	5.5V
Driver Input and Receiver Output	5.5V
Receiver Input and Driver Output	2.5V
Storage Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 4 sec.)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage	4.75	5.25	V
Temperature (T_A)	0	70	°C

DS3890 Electrical Characteristics (Notes 2 and 3)

DRIVER AND CONTROL INPUTS

Symbol	Conditions	Min	Typ	Max	Units
V_{IH}		2.0			V
V_{IL}				0.8	V
I_{IL} An	V_{CC} = Max V_{IN} = 0.4V		−1	−1.6	mA
I_{IL} Dis	V_{CC} = Max V_{IN} = 0.4V		−180	−400	μA
I_{IH}	V_{CC} = Max V_{IN} = 2.4V			40	μA
I_I	V_{CC} = Max V_{IN} = 5.25V			1	mA
V_{CL}	V_{CC} = Min I_{IN} = −12 mA		−0.9	−1.5	V
DRIVER OUTPUT					
V_{OL}	V_{CC} = Min R_L = 18.5Ω	0.75	1.0	1.2	V
I_{OH}	V_{CC} = Max V_{OUT} = 2V	−20	10	100	μA
I_O	V_{CC} = 0V V_{OUT} = 2V			100	μA
I_{IL}	V_{CC} = Max V_{OUT} = 0.75V		−100	−250	μA
I_{CC} Low	V_{CC} = Max		50	80	mA
I_{CC} High				100	mA

DS3892 Electrical Characteristics (Notes 2 and 3)

CONTROL INPUTS

Symbol	Conditions	Min	Typ	Max	Units
V_{IH}		2.0			V
V_{IL}				0.8	V
I_{IL}	V_{CC} = Max V_{IN} = 0.4V		−180	−400	μA
I_{IH}	V_{CC} = Max V_{IN} = 2.4V			40	μA
I_I	V_{CC} = Max V_{IN} = 5.25V			1	mA
V_{CL}	V_{CC} = Min I_{IN} = −12 mA		−0.9	−1.5	V
RECEIVER					
V_{OL}	V_{CC} = Min I_{OL} = 16 mA		0.35	0.5	V
V_{OH}	V_{CC} = Min I_{OH} = −400 μA	2.4	3.2		V
I_{OS}	V_{CC} = Max V_{OUT} = 0V	−20	−70	−100	mA
V_{TH} Rec	V_{CC} = 5V	1.47	1.55	1.62	V
I_{IH} Rec	V_{CC} = Max V_{IN} = 2V		10	100	μA
I_I Rec	V_{CC} = 0V V_{IN} = 2V			100	μA
I_{IL} Rec	V_{CC} = Max V_{IN} = 0.75V			100	μA
I_{CC} Low	V_{CC} = Max			80	mA
I_{CC} High				60	mA

DS3890 Switching Characteristics *(Figure 1)*

$0°C \leq T_A \leq 70°C$, $4.75V \leq V_{CC} \leq 5.25V$ unless otherwise specified

Symbol	Conditions	Min	Typ	Max	Units
T_{dLH}	An to Bn		9	15	ns
T_{dHL}			9	15	ns
T_{dLH}	Dis to Bn		10	18	ns
T_{dHL}			12	20	ns
T_r & T_f	Bn rise and fall time	3	6	10	ns

DS3892 Switching Characteristics (*Figures 2, 3* and *4*)

Symbol	Conditions	Min	Typ	Max	Units
T_{dLH}	Bn to An		12	18	ns
T_{pHL}			10	18	ns
T_{dLZ}	Dis to An		10	18	ns
T_{dZL}			8	15	ns
T_{dHZ}			4	8	ns
T_{dZH}			7	12	ns
TNR	Receiver noise rejection	3	6		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The Table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive values; all currents out of the device are shown as negative; all voltages are referenced to ground unless otherwise specified. All values shown as max or min are classified on absolute value basis and apply to the full operating temperature and V_{CC} range.

Note 3: All typical values are $V_{CC} = 5V$, $T_A = 25°C$.

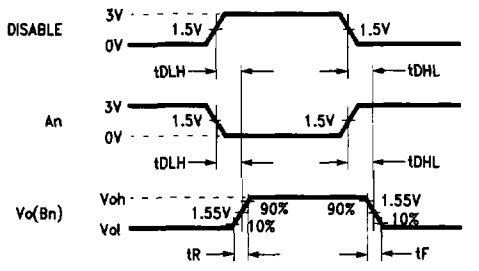
General Descriptions (Continued)

The DS3892 receiver inputs incorporate a low pass filter in conjunction with high speed comparator to further enhance the noise immunity. Both devices provide equal rejection to both positive and negative noise pulses (typically 6 ns) on the bus.

The DS3890 features TTL compatible inputs while the DS3892 inputs are BTL compatible. The control inputs on all devices are TTL compatible.

BTL "Backplane Transceiver Logic" is a new logic signaling method developed by IEEE P896 Future Bus Standards Committee. This standard was adopted to enhance the performance of Backplane Busses. BTL compatible bus interface circuits feature low capacitance drivers to minimize bus loading, a 1V nominal signal swing for reduced power consumption and receivers with precision thresholds for maximum noise immunity. This new standard overcomes some of the fundamental limitations of TTL bus transceivers in heavily loaded backplane bus applications. Devices designed to this standard provide significant improvements in switching speed and data integrity.

AC Switching Waveforms



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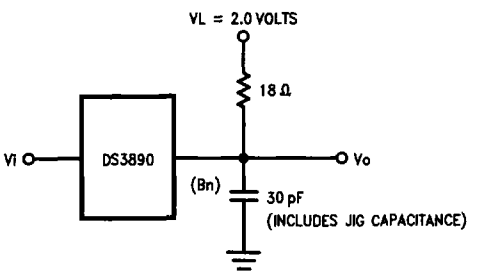

Note: $t_R = t_F < 10$ ns from 10% to 90%

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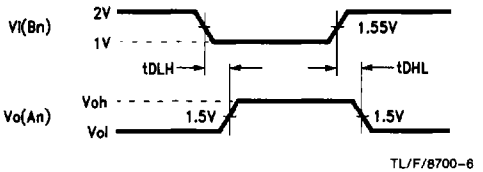
FIGURE 1
Driver Propagation Delays

AC Switching Waveforms (Continued)



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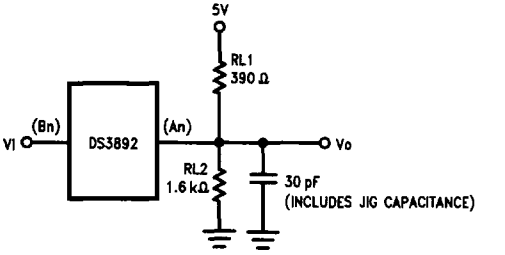

Note: $t_R = t_F < 10$ ns from 10% to 90%

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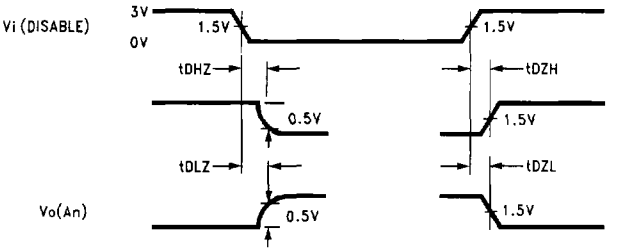
FIGURE 2. Receiver Propagation Delays



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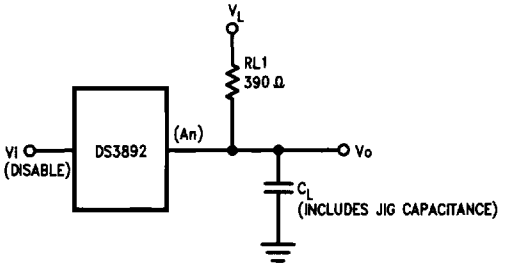
t_{DLZ}



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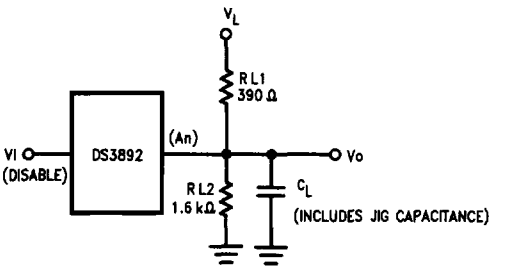
t_{DZL}



Note: $t_R = t_F < 5$ ns from 10% to 90%

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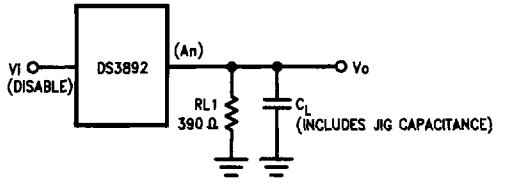
t_{DHZ}



Note: $t_R = t_F < 5$ ns from 10% to 90%

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t_{DZH}

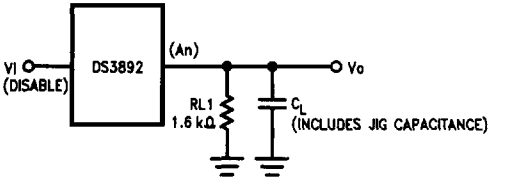

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FIGURE 3. Propagation Delay from Disable Pin to An

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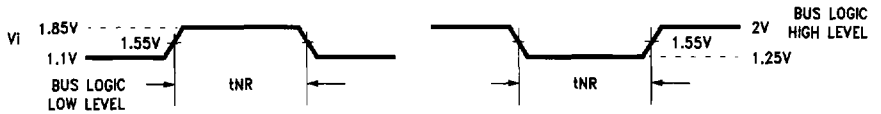
AC Switching Waveforms (Continued)



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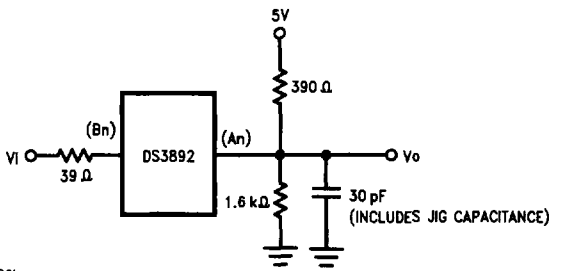
High **Low**



Note: $t_R = t_F < 2$ ns from 10% to 90%

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FIGURE 4

Receiver Noise Immunity:
"No Response at Output" Input Waveforms