GENERAL DESCRIPTION

The ft2815 is a charge-pump boosted Class-G/D/AB audio power amplifier with automatic level control (ALC) for portable audio applications. It integrates a Class-D/AB audio power amplifier with a Class-G charge pump regulator. With a supply voltage at 5V, it can deliver an output power of 5W with 10% THD+N, or 4.2W with 1% THD+N, into a 4Ω speaker load. Housed in a small package of QFN3x3-16L, the ft2815 delivers highest density of output power in its kind.

In ft2815, the power supply rail of the audio amplifier's output stage can be adaptively boosted and regulated by a Class-G charge pump regulator, allowing higher audio loudness than a stand-alone one directly connected to the battery. The adaptive nature of the Class-G charge pump regulator's output voltage, varying dynamically in response to the level of the audio outputs, improves power efficiency and extends battery life in playing audio. Its higher output power and greater power efficiency make ft2815 an ideal audio solution for portable applications based upon single-cell Lithium batteries.

To facilitate various applications, the charge pump regulator in ft2815 can be configured in either Adaptive Boost or Bypass mode.

Furthermore, the ft2815 provides with three types of audio amplifier outputs, i.e., Class-G, D, AB. For typical applications, Class-G/D outputs are preferred for high efficiency. Class-AB outputs are specifically to alleviate design complexities for applications where minimum FM radio interference is required.

A simple one-wire pulse control is employed in ft2815 to configure the device in various operating modes.

The ft2815 features ALC that constantly monitors and safeguards the audio outputs against the amplifier's supply voltage, preventing output clipping distortion, excessive power dissipation, or speaker over-load. Once an over-level condition is detected, the ALC lowers the amplifier's voltage gain proportionally to eliminate output clipping.

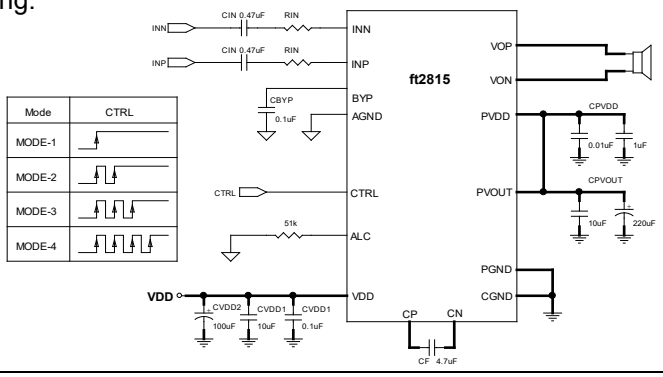
FEATURES

- Wide range of supply voltages from 3V to 5.5V
- Filterless Class- D/AB audio amplifier integrated with Class-G charge pump regulator
- Automatic level control to eliminate output clipping
- Maximum output power (Non-ALC Mode)
  - 5.0W (R_L=4Ω+33μH, THD+N=10%, V_{DD}=5V)
  - 4.2W (R_L=4Ω+33μH, THD+N=1%, V_{DD}=5V)
  - 3.8W (R_L=4Ω+33μH, THD+N=1%, V_{DD}=4.2V)
  - 3.4W (R_L=4Ω+33μH, THD+N=1%, V_{DD}=3.7V)
  - 2.3W (R_L=8Ω+33μH, THD+N=1%, V_{DD}=5V)
  - 2.2W (R_L=8Ω+33μH, THD+N=1%, V_{DD}=3.7V)
- Constant output power (ALC Mode, V_{IN}=0.4V_{RMS})
  - 3.8W (R_L=4Ω+33μH, THD+N<1%, V_{DD}=5V)
  - 3.6W (R_L=4Ω+33μH, THD+N<1%, V_{DD}=4.2V)
  - 3.3W (R_L=4Ω+33μH, THD+N<1%, V_{DD}=3.7V)
  - 2.2W (R_L=8Ω+33μH, THD+N<1%, V_{DD}=5V)
  - 2.2W (R_L=8Ω+33μH, THD+N<1% V_{DD}=3.7V)
- Highest density of output power in its kind
- One-wire pulse control to set operating mode
- Charge pump configuration: Adaptive Boost or Bypass
- Audio output configuration: Class-G/D/AB
- Low quiescent current: 3.2mA @ V_{DD}=3.7V
- Maximum voltage gain: 26dB
- Three ALC dynamic characteristics (sound effects)
- High SNR: 88dB (V_{DD}=3.7V, R_L=4Ω+33μH, P_O=1W)
- High efficiency: 70% (V_{DD}=3.7V, R_L=4Ω+33μH, P_O=1W)
- Low THD+N: 0.06% (V_{DD}=3.7V, R_L=4Ω+33μH, P_O=1W)
- Wide ALC dynamic range: 10dB
- Auto-recovering over-current and thermal-overload protection
- Available in QFN3x3-16L package

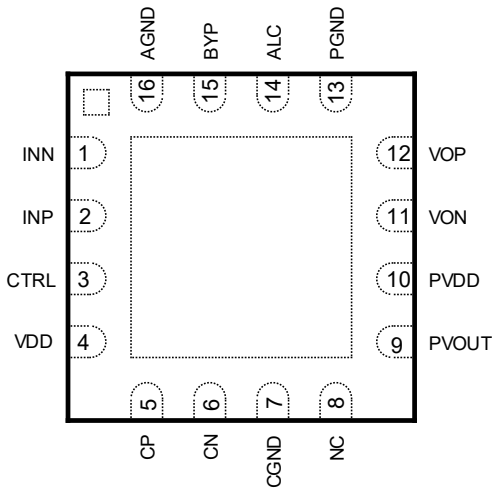
APPLICATIONS

- Blue Tooth Speakers
- Smart Speakers
- Portable Consumer Electronic Devices

TYPICAL APPLICATION CIRCUIT



PIN ASSIGNMENT AND DESCRIPTION



ft2815Q (TOP VIEW)

NAME	PIN #	TYPE	DESCRIPTION
INN	1	AI	Inverting audio input.
INP	2	AI	Non-inverting audio input.
CTRL	3	DI	**Operating Mode Control** with an internal 300kΩ pulldown resistor to ground. A string of VDD-compliant digital pulses sets the operating mode and the voltage gain of the audio amplifier. When held low for more than 5 milliseconds, the device enters into shutdown mode.
VDD	4	P	Power supply input. Place the supply decoupling capacitors of 10μF//0.1μF close to the pin.
CP	5	AO	Positive connection to the flying capacitor C_F of the charge pump regulator.
CN	6	AO	Negative connection to the flying capacitor C_F of the charge pump regulator.
CGND	7	G	Power ground for the charge pump regulator. Connect to the system ground plane GND.
NC	8	-	No internal connection.
PVOUT	9	AO	Boosted voltage output of the charge pump regulator. Place an output capacitor of 10μF close to the pin. Short the pin directly to PVDD on the system board.
PVDD	10	P	Power supply input for the audio amplifier's output stage. Place the supply decoupling capacitors of 1μF//0.01μF close to the pin. Short the pin directly to PVOUT on the system board.
VON	11	AO	Inverting BTL audio output.
VOP	12	AO	Non-inverting BTL audio output.
PGND	13	G	Power ground for the audio amplifier's output stage. Connect to the system ground plane GND.
ALC	14	AI	**ALC Mode Select** to set the ALC dynamic characteristic in the operating modes of Mode-1, 2, or 3. In the operating mode of Mode-4, the ALC function is disabled and this pin has no effect.
BYP	15	AO	Common-mode voltage bias for the audio inputs. Place a decoupling capacitor of 0.1μF close to the pin.
AGND	16	G	Analog ground. Connect to the system ground plane GND.
GND	17	G	Thermal pad ground. Connect to the system ground plane GND.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKING OPTION	PACKAGE
ft2815Q	-40°C to +85°C	Tape and Reel, 5000	QFN3X3-16L

REVISION HISTORY

Initial Release (February 2019)

Changed from Initial 1.0 (February 2019) to Revision 1.1 (January 2020)

1. Changed the operation of Mode-3 from Class-G (with Charge Pump Regulator enabled) to Class-D (with Charge Pump Regulator disabled) and the ALC characteristic is set by the ALC pin.
2. Added electrical characteristics for Mode-3 (Class-D) on Page 9.
3. Lowered the specification of the audio output offset voltage from ±30mV to ±10mV.
4. Changed the BYP voltage and the INN/INP input common voltage from 1.85V to 1.67V for Class-AB operation and revised the output power rating in Mode-4 accordingly.
5. Adjusted ALC dynamic characteristics of ALC-1 mode.
6. Changed the recommended audio input capacitance from 0.33μF to 0.47μF.

Changed from Revision 1.1 (January 2020) to Revision 1.2 (September 2022)

1. Added PACKING OPTION.

ABSOLUTE MAXIMUM RATINGS (Note 1)

PARAMETER	VALUE
Supply Voltage, VDD	-0.3V to 6V
PVOUT, PVDD, VOP, VON, CP, CN	-0.3V to 7V
All Other Pins	-0.3V to VDD+0.3V
CGND to AGND, PGND to AGND	-0.3V to 0.3V
ESD Ratings - Human Body Model (HBM)	2000V
Operating Junction Temperature	-40°C to +150°C
Storage Temperature	-40°C to +125°C
Maximum Soldering Temperature (@10 sec. duration)	260°C

Note 1: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

POWER DISSIPATION RATINGS (Note 2, 3)

PACKAGE	TA ≤ +25°C	TA = +70°C	TA = +85°C	Θ_{JA}
QFN3x3-16L	3.1W	2.0W	1.6W	40°C/W

Note 2: The thermal pad of the package must be directly soldered onto a grounded metal island as a thermal sink on the system board.
Note 3: The power dissipation ratings are for a two-side, two-plane printed circuit board (PCB).

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Supply Voltage	V_{DD}	VDD (Note 4)		3		5.5	V
Operating Ambient Temperature	T_A			-40		85	°C
Minimum Load Resistance	R_L	Across VOP and VON		3.2	4		Ω
Digital High Input Voltage	V_{HI}	@ CTRL		1.2			V
Digital Low Input Voltage	V_{LO}	@ CTRL				0.4	V
Audio Input Resistor	R_{IN}	@ INP, INN (Note 5)		0	10	22	kΩ
Audio Input Capacitor	C_{IN}	@ INP, INN (Note 5)			0.33	1.0	μF
Bypass Capacitor	C_{BYP}	@ BYP			0.1	1.0	μF
Supply Decoupling Capacitor	C_{VDD}	Ceramic			10	22	μF
		Electrolytic or Tantalum (Note 6)			100	220	μF
Boosted Supply Decoupling Cap.	C_{PVDD}	@ PVDD			1.0		μF
Charge Pump Flying Capacitor	C_F	Ceramic	4Ω Speaker		4.7	10	μF
			8Ω Speaker		2.2	4.7	μF
Charge Pump Output Capacitor	C_{POUT}	Ceramic			10	44	μF
		Electrolytic or Tantalum (Note 6)	4Ω Speaker		220	470	μF
			8Ω Speaker		100	220	μF
ALC Mode Select Resistor (Mode-1 & Mode-2)	R_{ALC}	Non-ALC Mode		10kΩ to VDD			
		ALC-3 Mode		Unconnected			
		ALC-2 Mode		51kΩ to GND			
		ALC-1 Mode		Short to GND			

Note 4: The maximum supply voltage will be also affected by the thermal dissipation capabilities of the package and the layout of the system board. Since the power efficiency of the charge pump regulator is inversely proportional to the supply voltage, an occasional thermal shutdown may occur for applications where the supply voltage is 4.5V or higher with speaker loads of 4Ω or less.

Note 5: The impedance seen at two audio inputs, INP and INN, shall be limited to an $R_{IN}C_{IN}$ time constant less than 5 milliseconds, allowing the input capacitors C_{IN} to be fully charged during the startup time of 40 milliseconds. If the input capacitors C_{IN} are not fully charged during the startup time, mismatch in resistance or capacitance between two audio inputs may cause pop noise.

Note 6: Input/output bulk electrolytic or tantalum capacitors are not required for a proper operation of the charge pump regulator. However, additional bulk capacitors in tandem with ceramic capacitors are needed to facilitate higher output current capability and higher voltage margin for higher output power, particularly in applications where speaker load impedances are 4Ω or less.

IMPORTANT APPLICATION NOTES

1. It is crucial to place the ft2815 in close proximity to the flying capacitor and input/output capacitors of the charge pump regulator on the system board, minimizing parasitic impedance of high current traces. Furthermore, place these capacitors on the same layer with ft2815. High-current traces are connected with short and wide metal lines and with no vias. Failure to do a proper layout of the system board can result in significant degradation of maximum output power, efficiency, and EMI performance.
2. The ft2815 is a high performance audio amplifier with an exposed thermal pad underneath the package. The thermal pad must be directly soldered onto a grounded metal island as a thermal sink on the system board for proper power dissipation. Failure to do so might result in the device entering into thermal shutdown prematurely.
3. The ft2815 requires adequate power supply decoupling to ensure its optimal performance in output power, efficiency, THD+N, and EMI emission. Place each decoupling capacitor as individually close as possible to VDD, BYP, and PVDD pins.
4. Place the charge pump flying capacitor C_F close to CP and CN pins and the output capacitors C_{PVOUT1} and C_{PVOUT2} close to the PVOUT pin.
5. It is recommended to employ a ground plane GND on the system board for ft2815. The CGND and PGND pins must be directly shorted to the ground plane GND, which serves as a central “star” ground for ft2815. Use a single point of connection between the analog ground AGND and the ground plane to minimize the coupling of high-current switching noise onto audio signals.
6. For best noise performance, use differential inputs from the audio source. In single-ended input applications, the unused audio input pin should be AC-grounded to the ground at the audio source.
7. Pay close attention to match the impedances seen at two differential inputs, INP and INN.
8. Apply a ferrite bead filter comprising a ferrite bead and a capacitor to audio outputs VOP and VON, as depicted in Figure 35, for further EMI suppression. Choose a ferrite bead with low DC resistance (DCR) and high impedance (100Ω ~ 470Ω) at high frequencies (>100MHz). Ensure that its rated current is no less than 3A for applications where the speaker load is 4Ω or less. Place each ferrite beard filter tightly together and individually close to VOP and VON pins.
9. For applications where speaker load resistances are 4Ω or less with long speaker wires, add an RC snubber circuit across two audio outputs, VOP and VON, as depicted in Figure 36, to prevent the device from accelerated deterioration or abrupt destruction due to excessive inductive flybacks that are induced on fast output switching or by an over-current condition.
10. Do not connect audio output VOP or VON directly to GND, VDD, PVDD, or PVOUT as this might damage the device permanently.

FUNCTIONAL BLOCK DIAGRAM

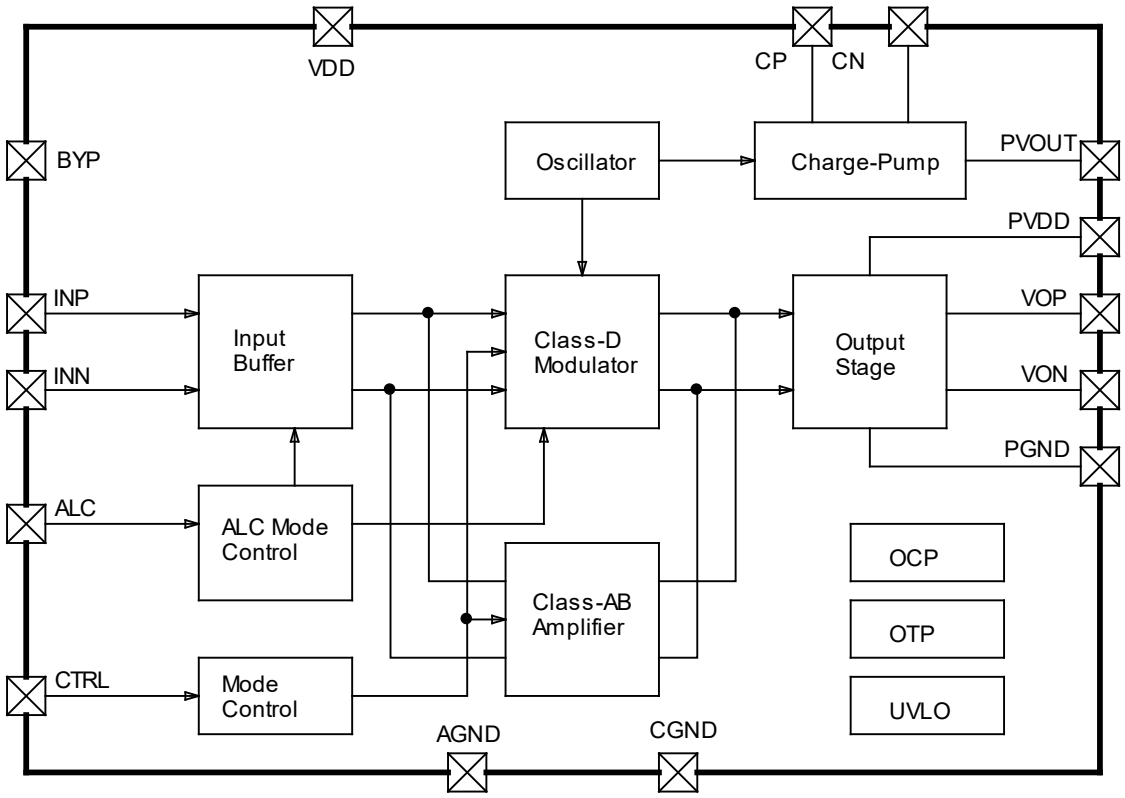


Figure 1: Simplified Functional Block Diagram of ft2815

TEST SETUP FOR ELECTRICAL & PERFORMANCE CHARACTERISTICS

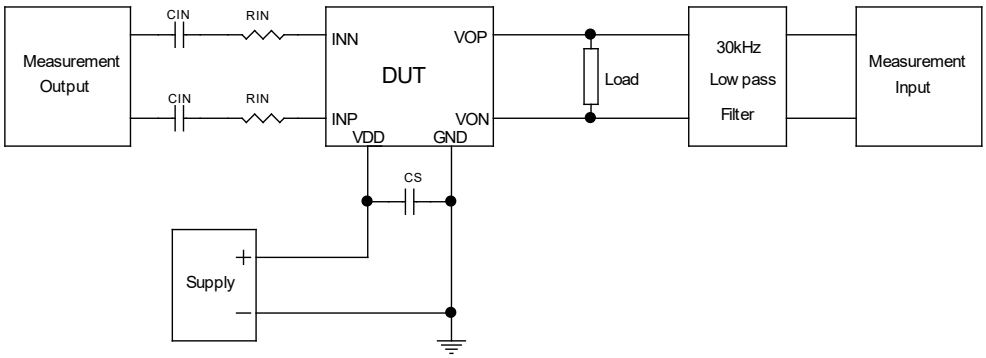


Figure 2: Test Setup Diagram for ft2815

All parameters specified in Electrical and Typical Performance Characteristics sections are measured according to the conditions:

1. The two differential inputs are shorted for common-mode input voltage measurement. All other parameters are taken with input resistors R_{IN}=10kΩ and input capacitors C_{IN}=0.33μF, unless otherwise specified.
2. The VDD supply decoupling capacitors C_{VDD1}=10μF//0.1μF are placed close to the VDD pin. Also, a bulk electrolytic or tantalum capacitor C_{VDD2}=100μF is added close to the device.
3. The PVDD supply decoupling capacitors C_{PVDD}=1μF/0.01μF are placed close to the PVDD pin.
4. The PVOUT output capacitor C_{PVOUT1}=10μF is placed close to the PVOUT pin. Also, a bulk electrolytic or tantalum capacitor C_{PVOUT2}=220μF is added close to the device.
5. An output inductor of 33μH inductor is placed in series with the load resistor to emulate a speaker load for all AC and dynamic parameters.
6. The 33kHz lowpass filter is added even if the analyzer has an internal lowpass filter. An RC lowpass filter (1kΩ, 4.7nF) is used on each output for the datasheet graphs.

ELECTRICAL CHARACTERISTICS

V_{DD}=3.7V, MODE-1, Load=4Ω+33μH, C_{IN}=0.47μF, R_{IN}=10kΩ, C_{VDD}=10μF//0.1μF//100μF, C_{PVDD}=1μF//0.01μF, C_{PVOUT}=10μF//220μF, C_F=4.7μF, C_{BYP}=0.1μF, f=1kHz, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DD}	Supply Voltage	VDD		3		5.25	V
V_{UVLOUP}	Power-On Threshold Voltage	VDD from Low to High			2.2		V
V_{UVLODN}	Power-Off Threshold Voltage	VDD from High to Low			2.0		V
I_{DDQ}	Supply Quiescent Current Inputs AC-Grounded, No Load	V_{DD}=3.7V	Mode-1 (Class-G)	2.4	3.2	4.2	mA
			Mode-4 (Class-AB)	18	24	32	mA
		V_{DD}=5.0V	Mode-1 (Class-G)	2.8	3.7	4.8	mA
			Mode-4 (Class-AB)	20	32	50	mA
I_{SD}	Shutdown Current	CTRL=Low			0.1	1	μA
V_{BYP}	Bypass Voltage	No Load, V_{DD}=3.7V		1.55	1.67	1.80	V
V_{HI}	Digital High Input Voltage	@ CTRL		1.2			V
V_{LO}	Digital Low Input Voltage	@ CTRL				0.4	V
V_{ALC}	ALC Mode Select Voltage	10kΩ to VDD (Non-ALC)		V_{DD}-0.5		V_{DD}	V
		R_{ALC}=Open (ALC-3)		1.5	1.7	1.9	V
		R_{ALC}=51kΩ to GND (ALC-2)		0.70	1.0	1.3	V
		R_{ALC}=0Ω to GND (ALC-1)				0.30	V
T_{OTSD}	Over-Temperature Threshold				160		°C
T_{HYS}	Over-Temperature Hysteresis				20		°C
CLASS-G CHARGE PUMP REGULATOR							
PVOUT	Charge Pump Output Voltage	I_{OUT}=0mA		6.1	6.3	6.5	V
f_{CP}	Charge Pump Frequency			800	1000	1200	kHz
CLASS-G AUDIO POWER AMPLIFIER (MODE-1, MODE-2)							
$P_{O, MAX}$	Maximum Output Power Load=4Ω+33μH Non-ALC	V_{DD}=5.0V	THD+N=10%		5.0		W
			THD+N=1%		4.2		W
		V_{DD}=4.2V	THD+N=10%		4.6		W
			THD+N=1%		3.8		W
		V_{DD}=3.7V	THD+N=10%		3.8		W
			THD+N=1%		3.4		W
	Maximum Output Power Load=8Ω+33μH Non-ALC	V_{DD}=5.0V	THD+N=10%		2.8		W
			THD+N=1%		2.3		W
		V_{DD}=4.2V	THD+N=10%		2.8		W
			THD+N=1%		2.3		W
		V_{DD}=3.7V	THD+N=10%		2.7		W
			THD+N=1%		2.2		W
$P_{O, ALC}$	Constant Output Power V_{IN}=0.40V_{RMS} ALC-3	Load=4Ω+33μH	V_{DD}=5.0V		3.8		W
			V_{DD}=4.2V		3.6		W
			V_{DD}=3.7V		3.3		W
		Load=8Ω+33μH	V_{DD}=5.0V		2.2		W
			V_{DD}=4.2V		2.2		W
			V_{DD}=3.7V		2.2		W

ELECTRICAL CHARACTERISTICS

V_{DD}=3.7V, MODE-1, Load=4Ω+33μH, C_{IN}=0.47μF, R_{IN}=10kΩ, C_{VDD}=10μF//0.1μF//100μF, C_{PVDD}=1μF//0.01μF, C_{PVOUT}=10μF//220μF, C_F=4.7μF, C_{BYP}=0.1μF, f=1kHz, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
CLASS-G AUDIO POWER AMPLIFIER (Cont'd)							
THD+N	Total Harmonic Distortion + Noise	Load=4Ω+33μH	P_O=1.0W		0.06		%
			V_{IN}=0.40V_{RMS} ALC-3		0.8		%
		Load=8Ω+33μH	P_O=0.50W		0.03		%
			V_{IN}=0.40V_{RMS} ALC-3		0.6		%
η	Power Efficiency	Load=4Ω+33μH	P_O=0.50W		80		%
			P_O=1.0W		70		%
			V_{IN}=0.40V_{RMS} ALC-3		68		%
		Load=8Ω+33μH	P_O=0.25W		81		%
			P_O=0.50W		71		%
			V_{IN}=0.40V_{RMS} ALC-3		76		%
A_V	Voltage Gain	R_{IN}=10kΩ	Mode-1		23		dB
			Mode-2		20		dB
A_{MAX}	Maximum ALC Attenuation				10		dB
V_{COMM}	Input Common-Mode Bias	@ INP, INN			1.7		V
R_{IN}	Input Resistance	@ INP, INN			20		kΩ
R_O	Output Resistance in Shutdown	CTRL=Low @ VOP, VON			3		kΩ
V_{OS}	Output Offset Voltage	Inputs AC-Grounded, No Load			±10		mV
V_N	Output Voltage Noise	Inputs AC-Grounded A_V=20dB A-Weighted	Mode-1 R_{IN}=22kΩ		80		μV_{RMS}
			Mode-2 R_{IN}=10kΩ		80		μV_{RMS}
SNR	Signal-To-Noise Ratio	A_V=20dB A-Weighted	P_O=3W		93		dB
			P_O=1W		88		dB
PSRR	Power Supply Rejection Ratio	±100mV Ripple, f=1kHz, R_{IN}=0Ω			70		dB
CMRR	Common Mode Rejection Ratio	V_{IN}=0.20V_{RMS}, R_{IN}=0Ω			70		dB
f_{PWM}	PWM Switching Frequency			400	500	600	kHz
T_{STUP}	Startup Time				40		ms
T_{SD}	Shutdown Settling Time				5		ms
ONE-WIRE PULSE INTERFACE							
T_{LOW}	CTRL Pulse Low Duration			1		80	μs
T_{HIGH}	CTRL Pulse High Duration			1		80	μs
T_{SETUP}	Mode Setup Duration					500	μs
T_{SHDN}	Low Duration for Shutdown			400			μs

ELECTRICAL CHARACTERISTICS

V_{DD}=3.7V, MODE-3, Load=4Ω+33μH, C_{IN}=0.47μF, R_{IN}=10kΩ, C_{VDD}=10μF//0.1μF//100μF, C_{PVDD}=1μF//0.01μF, C_{PVOUT}=10μF//220μF, C_F=4.7μF, C_{BYP}=0.1μF, f=1kHz, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
CLASS-D AUDIO AMPLIFIER (MODE-3)							
V_{DD}	Supply Voltage	VDD		3		5.5	V
$P_{O, MAX}$	Maximum Output Power Load=4Ω+33μH	V_{DD}=5.0V	THD+N=10%		2.8		W
			THD+N=1%		2.3		W
		V_{DD}=4.2V	THD+N=10%		2.0		W
			THD+N=1%		1.6		W
		V_{DD}=3.7V	THD+N=10%		1.5		W
			THD+N=1%		1.2		W
	Maximum Output Power Load=8Ω+33μH	V_{DD}=5.0V	THD+N=10%		1.7		W
			THD+N=1%		1.4		W
		V_{DD}=4.2V	THD+N=10%		1.1		W
			THD+N=1%		0.95		W
		V_{DD}=3.7V	THD+N=10%		0.90		W
			THD+N=1%		0.74		W
$P_{O, ALC}$	Constant Output Power V_{IN}=0.40V_{RMS} ALC-3	Load=4Ω+33μH	V_{DD}=5.0V		2.2		W
			V_{DD}=4.2V		1.5		W
			V_{DD}=3.7V		1.2		W
		Load=8Ω+33μH	V_{DD}=5.0V		1.3		W
			V_{DD}=4.2V		0.90		W
			V_{DD}=3.7V		0.70		W
THD+N	Total Harmonic Distortion + Noise	Load=4Ω+33μH	P_O=1.0W		0.02		%
			V_{IN}=0.40V_{RMS} ALC-3		0.7		%
		Load=8Ω+33μH	P_O=0.50W		0.01		%
			V_{IN}=0.40V_{RMS} ALC-3		0.8		%
η	Power Efficiency	Load=4Ω+33μH	P_O=1.0W		81		%
			V_{IN}=0.40V_{RMS} ALC-3		81		%
		Load=8Ω+33μH	P_O=0.50W		87		%
			V_{IN}=0.40V_{RMS} ALC-3		88		%
A_V	Voltage Gain	R_{IN}=10kΩ			20		dB
V_{COMM}	Input Common-Mode Bias	@ INP, INN			1.7		V
V_N	Output Voltage Noise	Inputs AC-Grounded A_V=20dB, A-Weighted			80		μV_{RMS}
SNR	Signal-To-Noise Ratio	P_O=1.0W, A_V=20dB, A-Weighted			88		dB
PSRR	Power Supply Rejection Ratio	±100mV Ripple, f=1kHz, R_{IN}=0Ω			70		dB
CMRR	Common Mode Rejection Ratio	V_{IN}=0.20V_{RMS}, R_{IN}=0Ω			70		dB

ELECTRICAL CHARACTERISTICS

V_{DD}=3.7V, MODE-4, Load=4Ω+33μH, C_{IN}=0.47μF, R_{IN}=10kΩ, C_{VDD}=10μF//0.1μF//100μF, C_{PVDD}=1μF//0.01μF, C_{PVOUT}=10μF//220μF, C_F=4.7μF, C_{BYP}=0.1μF, f=1kHz, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
CLASS-AB AUDIO AMPLIFIER (MODE-4)							
V_{DD}	Supply Voltage	VDD		3		5.5	V
$P_{O, MAX}$	Maximum Output Power Load=4Ω+33μH	V_{DD}=5.0V	THD+N=10%		2.8		W
			THD+N=1%		2.3		W
		V_{DD}=4.2V	THD+N=10%		2.0		W
			THD+N=1%		1.6		W
		V_{DD}=3.7V	THD+N=10%		1.5		W
			THD+N=1%		1.2		W
	Maximum Output Power Load=8Ω+33μH	V_{DD}=5.0V	THD+N=10%		1.6		W
			THD+N=1%		1.2		W
		V_{DD}=4.2V	THD+N=10%		1.1		W
			THD+N=1%		0.88		W
		V_{DD}=3.7V	THD+N=10%		0.90		W
			THD+N=1%		0.67		W
THD+N	Total Harmonic Distortion + Noise	Load=4Ω+33μH, P_O=1.0W			0.10		%
		Load=8Ω+33μH, P_O=0.50W			0.08		%
η	Power Efficiency	Load=4Ω+33μH, P_O=1.0W			59		%
		Load=8Ω+33μH, P_O=0.50W			59		%
A_V	Voltage Gain	R_{IN}=10kΩ			20		dB
V_{COMM}	Input Common-Mode Bias	@ INP, INN, V_{DD}=3.7V			1.67		V
V_N	Output Voltage Noise	Inputs AC-Grounded A_V=20dB, A-Weighted			80		μV_{RMS}
SNR	Signal-To-Noise Ratio	P_O=1.0W, A_V=20dB, A-Weighted			88		dB
PSRR	Power Supply Rejection Ratio	±100mV Ripple, f=1kHz, R_{IN}=0Ω			70		dB
CMRR	Common Mode Rejection Ratio	V_{IN}=0.20V_{RMS}, R_{IN}=0Ω			70		dB

TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD}=3.7V, MODE-1, Load=4Ω+33μH, C_{IN}=0.47μF, R_{IN}=10kΩ, C_{VDD}=10μF//0.1μF//100μF, C_{PVDD}=1μF//0.01μF, C_{PVOUT}=10μF//220μF, C_F=4.7μF, C_{BYP}=0.1μF, f=1kHz, unless otherwise specified.

List of Performance Characteristic Plots

DESCRIPTION	CONDITIONS		FIGURE #
Output Power vs. Supply Voltage	Mode-1 Class-G	R_L=4Ω+33μH, THD+N=1%, 10%, ALC (V_{IN}=0.40V_{RMS})	3
		R_L=8Ω+33μH, THD+N=1%, 10%, ALC (V_{IN}=0.40V_{RMS})	4
	Mode-4 Class-AB	R_L=4Ω+33μH, THD+N=1%, 10%	5
		R_L=8Ω+33μH, THD+N=1%, 10%	6
Output Power vs. Input Voltage	V_{DD}=3.7V, R_L=4Ω+33μH, Mode-1 & 2, ALC		7
	V_{DD}=3.7V, R_L=4Ω+33μH, Mode-3 (ALC), Mode-4		8
	V_{DD}=4.2V, R_L=4Ω+33μH, Mode-1 & 2, ALC		9
	V_{DD}=4.2V, R_L=4Ω+33μH, Mode-3 (ALC), Mode-4		10
	V_{DD}=3.7V, R_L=8Ω+33μH, Mode-1 & 2, ALC		11
	V_{DD}=3.7V, R_L=8Ω+33μH, Mode-3 (ALC), Mode-4		12
	V_{DD}=4.2V, R_L=8Ω+33μH, Mode-1 & 2, ALC		13
	V_{DD}=4.2V, R_L=8Ω+33μH, Mode-3 (ALC), Mode-4		14
Efficiency vs. Output Power	R_L=4Ω+33μH, Mode-1, V_{DD}=3.7V, 4.2V		15
	R_L=8Ω+33μH, Mode-1, V_{DD}=3.7V, 4.2V, 5.0V		16
THD+N vs. Output Power	R_L=4Ω+33μH, Mode-1, V_{DD}=3.7V, 4.2V		17
	R_L=4Ω+33μH, Mode-4, V_{DD}=3.7V, 4.2V		18
	R_L=8Ω+33μH, Mode-1, V_{DD}=3.7V, 4.2V, 5.0V		19
	R_L=8Ω+33μH, Mode-4, V_{DD}=3.7V, 4.2V, 5.0V		20
THD+N vs. Input Voltage	R_L=4Ω+33μH, Mode-1, V_{DD}=3.7V, 4.2V		21
	R_L=4Ω+33μH, Mode-4, V_{DD}=3.7V, 4.2V		22
	R_L=8Ω+33μH, Mode-1, V_{DD}=3.7V, 4.2V, 5.0V		23
	R_L=8Ω+33μH, Mode-4, V_{DD}=3.7V, 4.2V, 5.0V		24
THD+N vs. Input Frequency	R_L=4Ω+33μH, Mode-1, P_O=1.0W		25
	R_L=4Ω+33μH, Mode-4, P_O=1.0W		
PSRR vs. Input Frequency	R_L=4Ω+33μH, Mode-1, Input AC-Grounded		26
	R_L=4Ω+33μH, Mode-4, Input AC-Grounded		
Quiescent Current vs. Supply Voltage	Input AC-Grounded, No Load, Mode-1		27
	Input AC-Grounded, No Load, Mode-4		
Output Power vs. Input Frequency	R_L=4Ω+33μH, P_O=1W, 3W, f=20Hz ~ 20kHz		28
Output Waveforms on ALC Attack	(VOP-VON) with 33kHz RC Lowpass Filter, V_{IN}=0.25V_{RMS} →		29
Output Waveforms on ALC Release	(VOP-VON) with 33kHz RC Lowpass Filter, V_{IN}=0.70V_{RMS} →		30
Output Waveforms during Startup	(VOP-VON) with 33kHz RC Lowpass Filter, V_{IN}=0.10V_{RMS}		31
Output Waveforms during Shutdown	(VOP-VON) with 33kHz RC Lowpass Filter, V_{IN}=0.10V_{RMS}		32

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

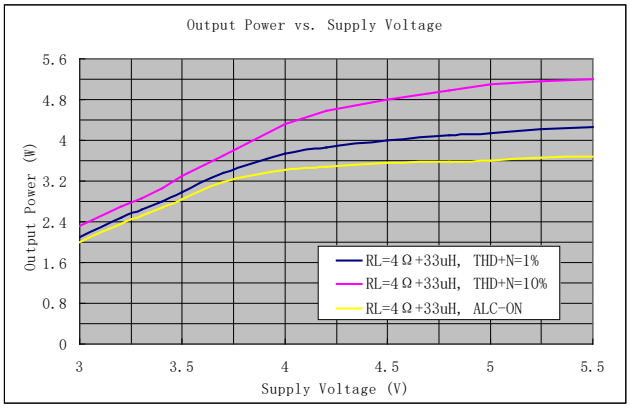


Figure 3: Output Power (Class-G) vs. Supply Voltage

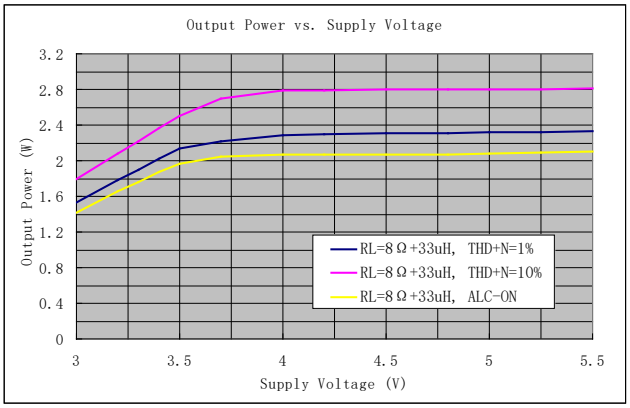


Figure 4: Output Power (Class-G) vs. Supply Voltage

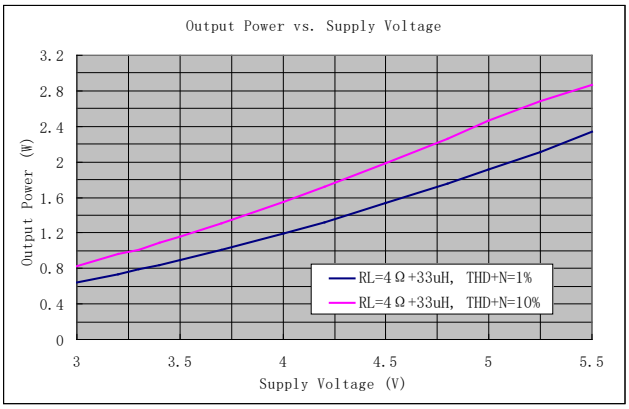


Figure 5: Output Power (Class-AB) vs. Supply Voltage

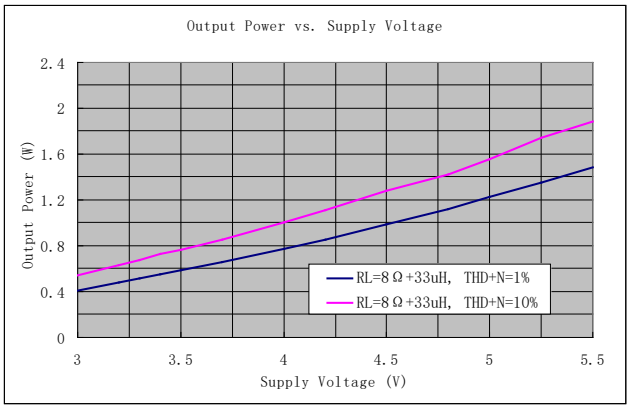


Figure 6: Output Power (Class-AB) vs. Supply Voltage

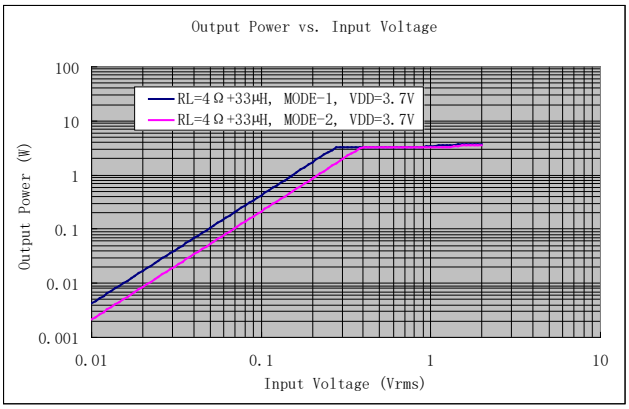


Figure 7: Output Power vs. Input Voltage

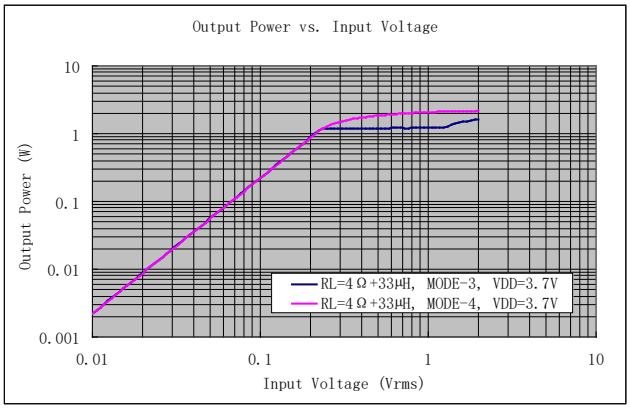


Figure 8: Output Power vs. Input Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

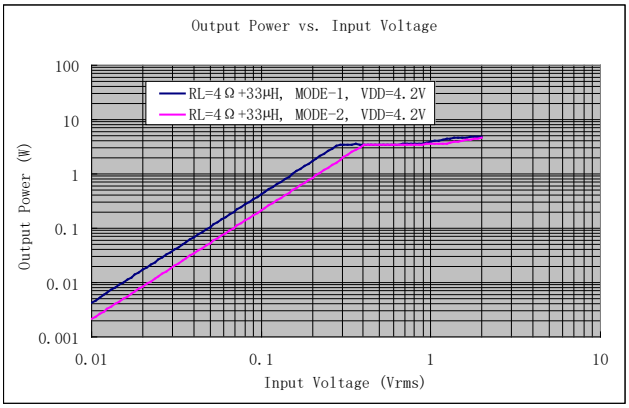


Figure 9: Output Power vs. Input Voltage

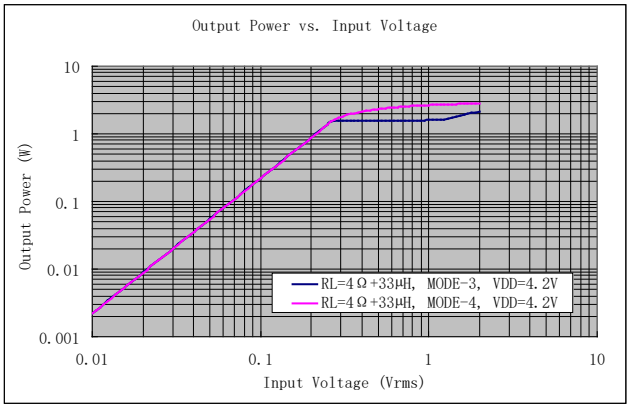


Figure 10: Output Power vs. Input Voltage

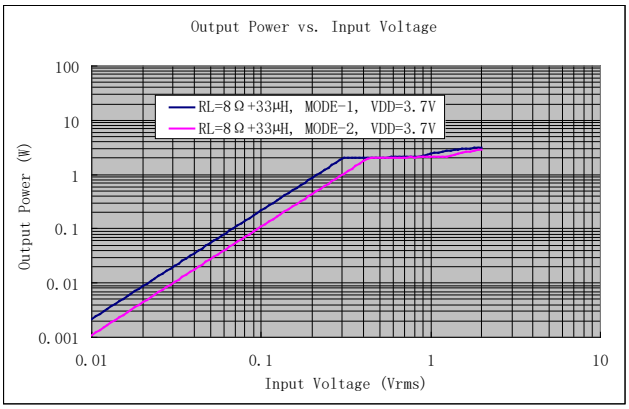


Figure 11: Output Power vs. Input Voltage

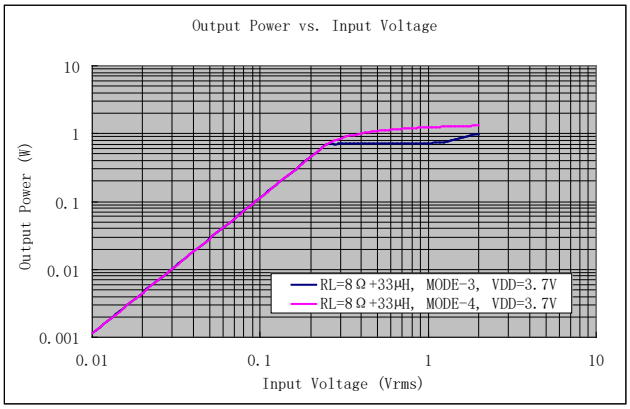


Figure 12: Output Power vs. Input Voltage

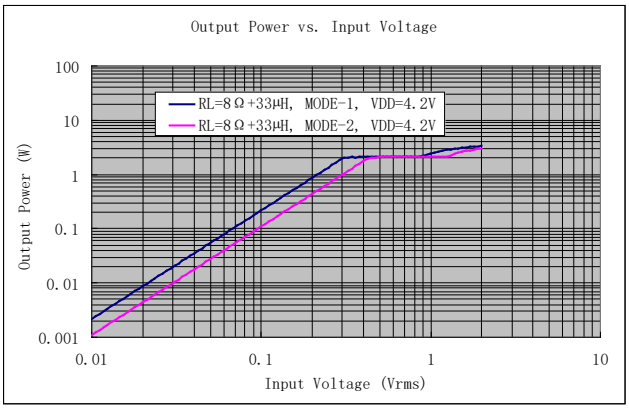


Figure 13: Output Power vs. Input Voltage

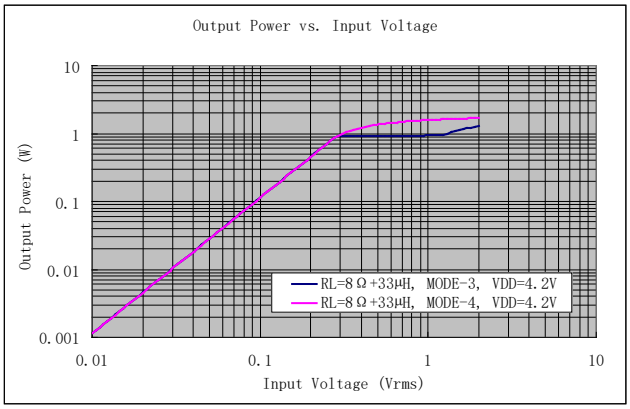


Figure 14: Output Power vs. Input Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

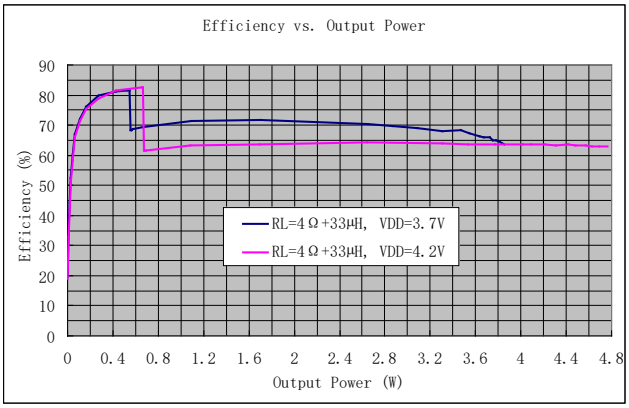


Figure 15: Efficiency vs. Output Power

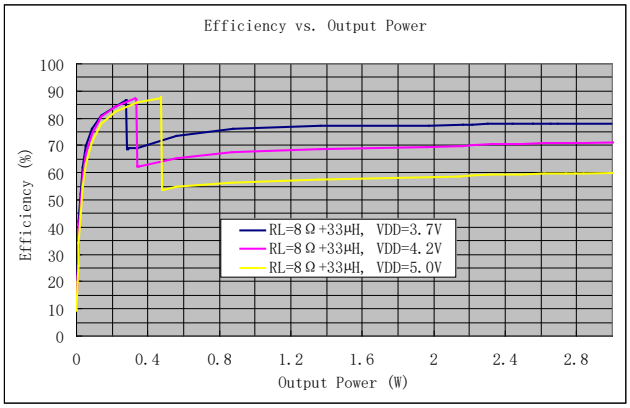


Figure 16: Efficiency vs. Output Power

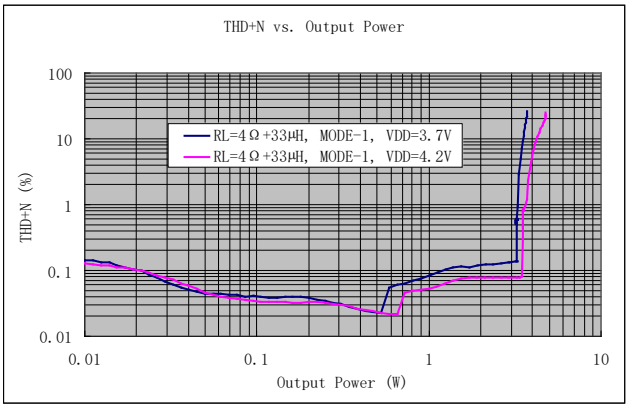


Figure 17: THD+N vs. Output Power (Class-G)

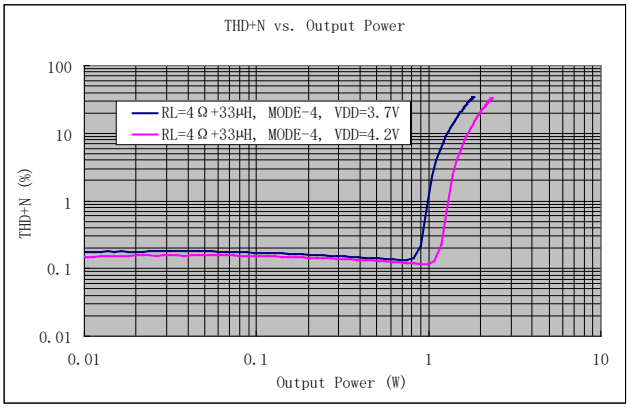


Figure 18: THD+N vs. Output Power (Class-AB)

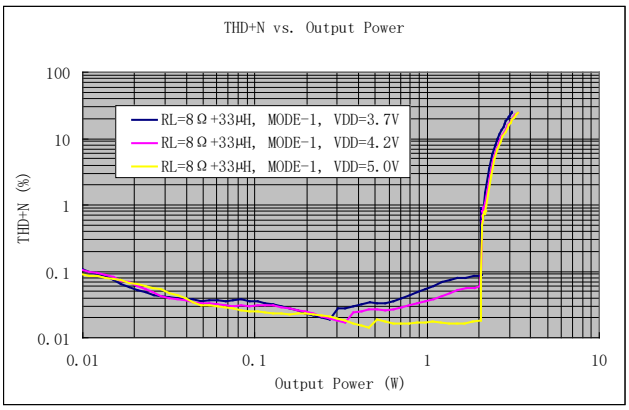


Figure 19: THD+N vs. Output Power (Class-G)

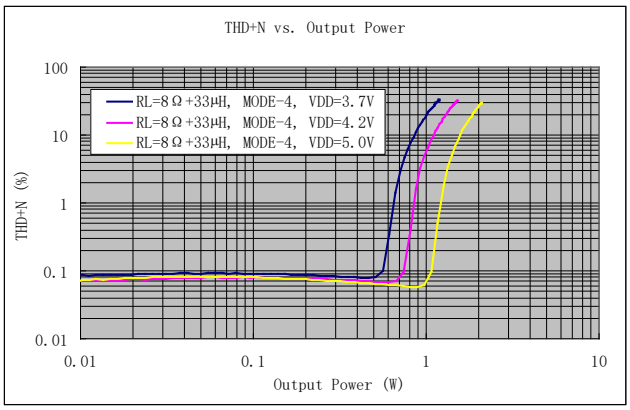


Figure 20: THD+N vs. Output Power (Class-AB)

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

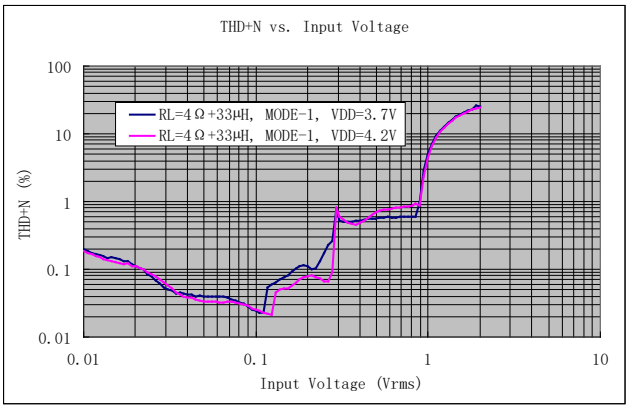


Figure 21: THD+N vs. Input Voltage (Class-G)

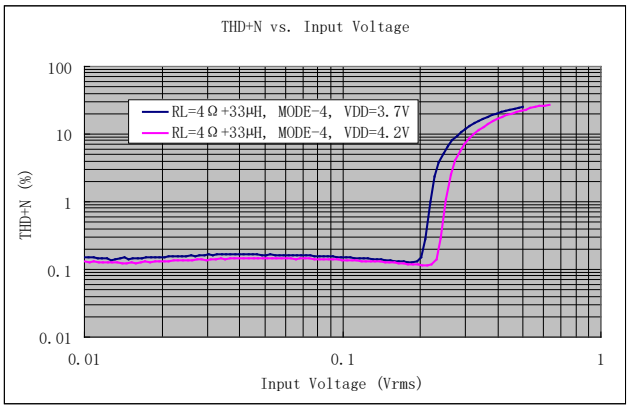


Figure 22: THD+N vs. Input Voltage (Class-AB)

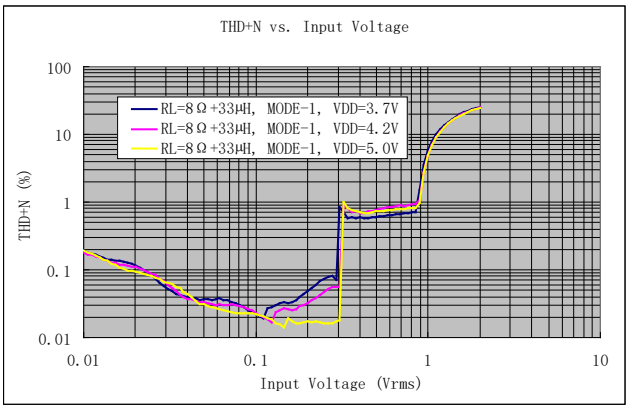


Figure 23: THD+N vs. Input Voltage (Class-G)

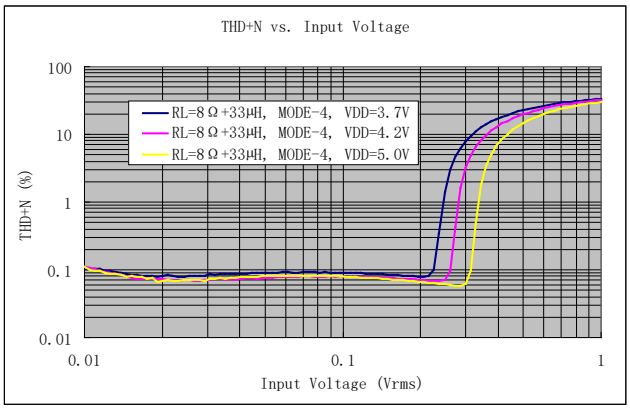


Figure 24: THD+N vs. Input Voltage (Class-AB)

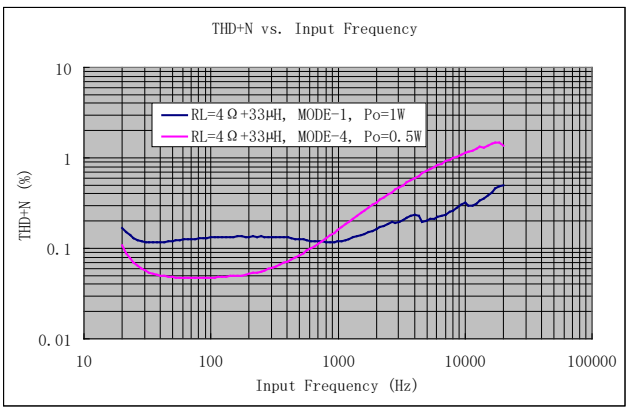


Figure 25: THD+N vs. Input Frequency

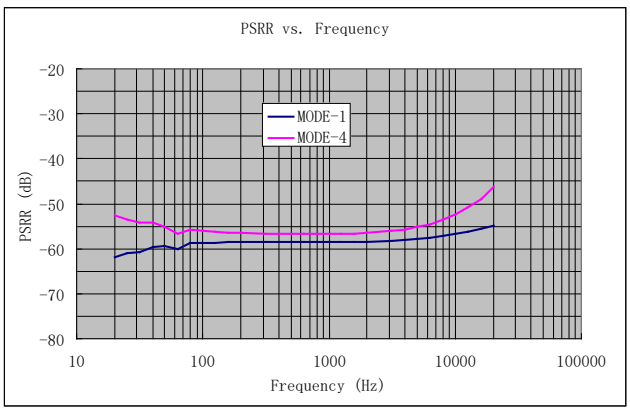


Figure 26: PSRR vs. Input Frequency

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

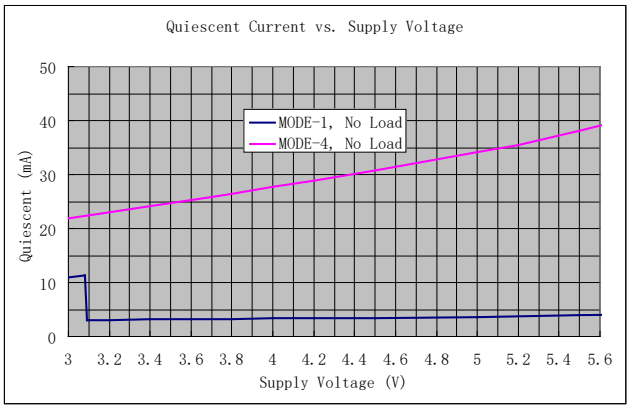


Figure 27: Quiescent Current vs. Supply Voltage

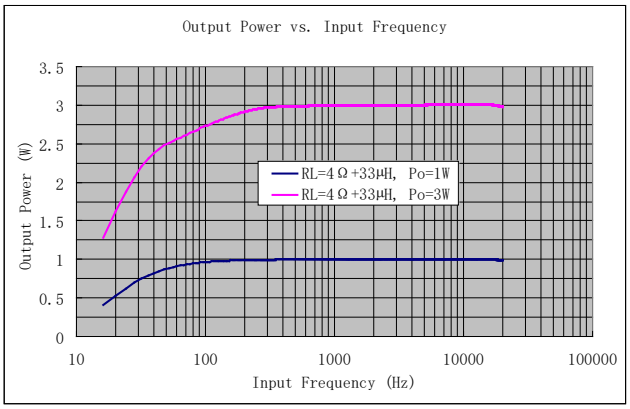


Figure 28: Output Power vs. Input Frequency

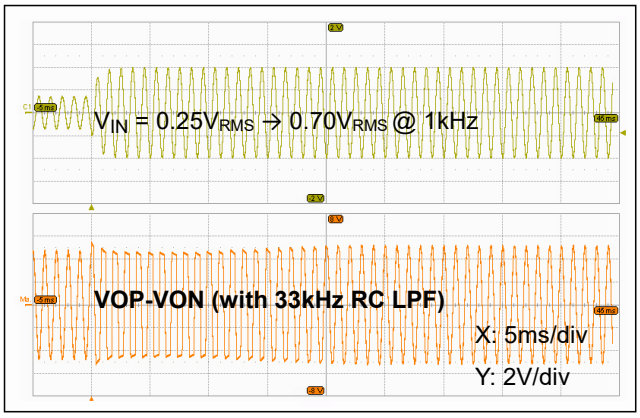


Figure 29: Output Waveforms on ALC Attack

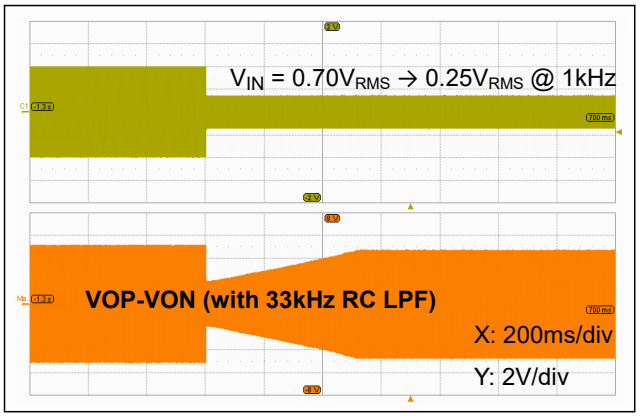


Figure 30: Output Waveforms on ALC Release

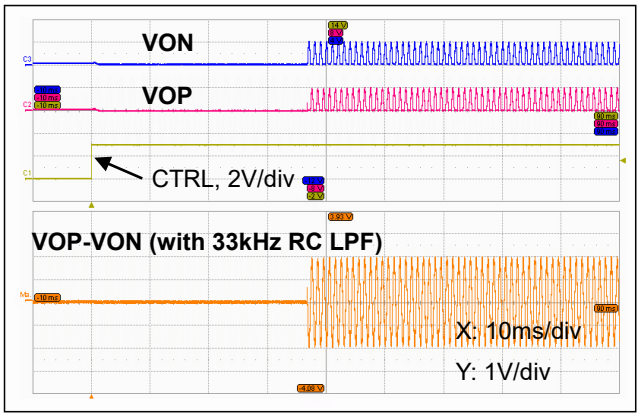


Figure 31: Output Waveforms during Startup

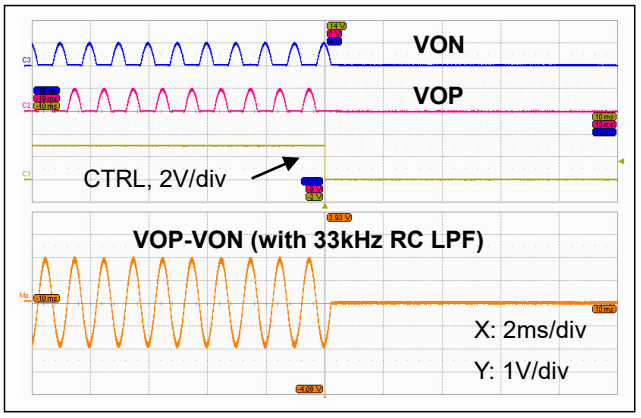


Figure 32: Output Waveforms during Shutdown

APPLICATION INFORMATION

The ft2815 is a charge-pump boosted Class-G/D/AB audio power amplifier with automatic level control (ALC) for portable audio applications. It integrates a Class-D/AB audio power amplifier with a Class-G charge pump regulator. It operates from a wide range of supply voltages from 3 V to 5.5V. With a supply voltage at 5V, it can deliver an output power of 5W with 10% THD+N, or 4.2W with 1% THD+N, into a 4Ω speaker load. With a supply voltage at 4.2V, it can deliver an output power of 4.6W with 10% THD+N, or 3.8W with 1% THD+N, into a 4Ω speaker load. Housed in a small package of QFN3x3-16L, the ft2815 delivers highest density of output power in its kind.

In ft2815, the power supply rail of the audio amplifier's output stage can be adaptively boosted and regulated by a Class-G charge pump regulator, allowing higher audio loudness than a stand-alone one directly connected to the battery. The adaptive nature of the Class-G charge pump regulator's output voltage, varying dynamically in response to the level of the audio outputs, improves power efficiency and extends battery life in playing audio. Its higher output power and greater power efficiency make ft2815 an ideal audio solution for portable applications based upon single-cell Lithium batteries.

To facilitate various applications, the charge pump regulator in ft2815 can be configured in either Adaptive Boost or Bypass mode.

Furthermore, the ft2815 provides with three types of audio amplifier outputs, i.e., Class-G, D, and AB. For most applications, Class-G/D outputs are preferred for high power efficiency. Class-AB outputs are chosen specifically to alleviate design complexities for applications where minimum FM radio interference is required.

A simple one-wire pulse control is employed in ft2815 to configure the device in various operating modes.

The ft2815 features ALC that constantly monitors and safeguards the audio outputs against the amplifier's supply voltage, preventing output clipping distortion, excessive power dissipation, or speaker over-load. Once an over-level condition is detected, the ALC lowers the amplifier's voltage gain proportionally to eliminate output clipping while maintaining a maximum dynamic range of the audio outputs allowed with the amplifier's supply voltage. With a 4.2V supply voltage, the ft2815 can deliver an ALC output power of 3.6W with THD+N<1%, into a 4Ω speaker load.

As specifically designed for portable device applications, the ft2815 incorporates shutdown mode to minimize the power consumption by holding the CTRL pin to ground. It also includes comprehensive protection modes against various operating faults such as over-current, short-circuit, over-temperature, and under-voltage for safe and reliable operation.

ADAPTIVE CHARGE PUMP REGULATOR

To allow for higher audio loudness, an on-chip Class-G charge pump regulator is employed to boost PVDD, the power supply rail of the audio amplifier's output stage, from the supply voltage VDD to a higher value. Whenever the audio outputs are higher than a prescribed level for an extended period of time, the charge pump regulator is activated to boost and regulate PVDD at 6.3V. In this manner, the charge pump regulator operates in the regulation mode.

On the other hand, when the audio outputs are less than a prescribed level for an extended period of time, the charge pump regulator is de-biased and forced into the bypass mode. In the bypass mode, the amplifier output stage is powered directly from the battery voltage through VDD. The adaptive nature of the charge pump regulator can greatly improve the power efficiency of ft2815 in playing audio and extends battery life.

CHARGE PUMP REGULATOR

In order to maximize the output power, the ft2815 employs an on-chip charge pump regulator to boost the supply voltage PVDD of the audio power amplifier to a higher value. To limit the battery inrush current to an acceptable value when the supply voltage is first applied to the device, the charge pump regulator features soft-start during activation.

DESIGN GUIDELINES OF CHARGE PUMP REGULATOR

Selection of Flying Capacitor (C_F)

For 4Ω speaker loads, a low-ESR ceramic capacitor (such as X7R or X5R) of 4.7μF, 10V is recommended for the flying capacitor C_F of the charge pump. Higher values can be used to improve its dynamic response to load transients. For 8Ω speaker loads, a low-ESR ceramic capacitor of 2.2μF, 16V is recommended.

Selection of Output Capacitor (C_{PVOUT})

The output capacitor of the charge pump is required to keep output voltage ripples small and ensure maximum output power capability. A low-ESR ceramic capacitor of 10μF, 16V is recommended for the output capacitor C_{PVOUT1} of the charge pump.

It is noted that maximum output power of the audio amplifier at low frequencies will be largely affected by the output capacitance of the charge pump, particularly for low-impedance (4Ω or less) speakers. Thus, it is often necessary to add a bulk electrolytic or tantalum capacitor C_{PVOUT2} in tandem with ceramic capacitors for the output capacitance. The value of the bulk capacitor is application-specific. For 4Ω speaker loads, a bulk electrolytic capacitor of 220μF should be sufficient. For 8Ω speaker loads, a bulk electrolytic capacitor of 100μF can be used.

Table 4 lists recommended flying and output capacitances of the charge pump regulator for 4Ω and 8Ω speaker loads. It is highly recommended to add a small low-ESR ceramic capacitor of 0.1μF, 16V in close proximity to the PVDD pin for high-frequency decoupling.

Speaker Load Impedance	Input Supply Voltage	C_F (Ceramic)	C_{PVOUT1} (Ceramic)	C_{PVOUT2} (Electrolytic or Tantalum)
4Ω	3.6V ~ 4.2V	4.7μF	10μF//0.1μF	220μF ~ 470μF
	4.5V ~ 5.25V	2.2μF	10μF//0.1μF	100μF ~ 220μF
8Ω	3.6V ~ 4.2V	2.2μF	10μF//0.1μF	100μF ~ 220μF
	4.5V ~ 5.25V	1.0μF	10μF//0.1μF	47μF ~ 100μF

Table 1: Recommended Flying & Output Capacitors of Charge Pump Regulator

Selection of Supply Decoupling Capacitor (C_{VDD})

For best power supply coupling, place a low-ESR ceramic capacitor, 10μF or greater, close to the VDD pin. It is important to place the decoupling capacitor C_{VDD} close to ft2815 since any parasitic resistances between ft2815 and C_{VDD} cause efficiency loss. The decoupling capacitor serves as a charge reservoir for the input current that flows onto the flying capacitor C_F, thus reducing the amount of voltage ripples seen at the VDD pin.

The decoupling capacitor C_{VDD} must have an RMS current rating greater than 3A. Also the rated voltage of the input capacitor must be higher than the supply input voltage with sufficient voltage margin to minimize the effect of dc bias. For most applications, a low-ESR ceramic capacitor of 10μF, 10V can be used. Also, add a small low-ESR ceramic capacitor of 0.1μF to the VDD pin for high-frequency decoupling.

For applications where additional input capacitance is required to meet the requirement of the input current ripple or transient response, place a bulk electrolytic or tantalum capacitor in close proximity to ft2815. The bulk capacitor acts as a charge reservoir for the flying capacitor current, providing energy faster than the system power supply, mitigating current surges and/or voltage droops of the supply voltage. A bulk electrolytic capacitor of 100μF should be sufficient for ft2815.

OPERATING MODE CONTROL

To support for a wide range of applications, the ft2815 incorporates one-wire pulse control to configure the device in one of four operating modes. By applying a string of VDD-compliant digital pulses to the CTRL pin, the operating mode is set by the number of low-to-high transitions of digital pulses received at the CTRL pin.

After an initial application of the power supply, the first low-to-high transition at the CTRL pin forces the device

into Mode-1, where the audio amplifier is configured in Class-G operation with maximum voltage gain at 26dB. The second low-to-high transition advances the device into Mode-2, where the audio amplifier is also configured in Class-G operation with maximum voltage gain at 23dB. The third low-to-high transition advances the device into Mode-3, where the charge pump regulator is disabled and the input supply voltage VDD is directly applied to the supply rail of the audio amplifier. In Mode-3, the audio amplifier is configured in Class-D operation. Lastly, the fourth low-to-high transition advances the device into Mode-4, where the charge pump regulator is also disabled and the input supply voltage VDD is directly applied to the supply rail of the audio amplifier. In Mode-4, the audio amplifier is configured in Class-AB operation. The detailed timing diagram of the one-wire pulse control to select the operating mode is shown in Figure 33.

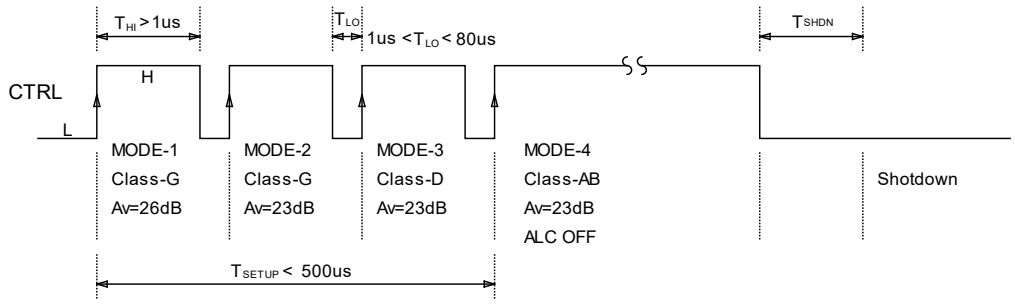


Figure 33: Timing Diagram of Operating Mode Control

Each individual pulse must be longer than a minimum of 1μs to be recognized. Any pulses shorter than 1μs may be ignored. Also, no more than four low-to-high transitions are recognized. Redundant low-to-high transitions after the fourth one will not alter the operating mode and the device remain in the final state, Mode-4. Also, all the digital pulses required for configuring the device in a specific mode must be received within 500 μs to be valid.

Whenever the CTRL pin is held low for more than 5ms, the device enters into shutdown mode, where all the internal circuitry is de-biased. Once the device is forced into shutdown mode, one or multiple digital pulses are required to return the device to the original mode of operation.

Mode	# of Pulses	Maximum Voltage Gain	Audio Amplifier Configuration	Charge Pump Regulator	ALC Functionality
Mode-1	1	26dB (21X)	Class-G	Enable	Set by ALC Pin
Mode-2	2	23dB (15X)	Class-G	Enable	Set by ALC Pin
Mode-3	3	23dB (15X)	Class-D	Disable	Set by ALC Pin
Mode-4	4	23dB (15X)	Class-AB	Disable	Disable

Table 2: Operating Mode Table

VOLTAGE GAIN SETTING

To accommodate for various levels of audio inputs, two voltage gain settings are available for the audio amplifier in ft2815. The voltage gain is selected via one-wire pulse control at the CTRL pin, as described in Table 2. It can also be fine-adjusted by inserting an external input resistor R_{IN} in series with an input capacitor C_{IN} to both differential inputs, INN and INP, individually. Equation 1 described the voltage gain for Mode-1 operation and Equation 2 for Mode-2, 3, 4 operations. In both equations, A_V is the voltage gain of the audio amplifier and R_{IN} is the external input resistor and expressed in kΩ. Table 3 shows example resistor values of R_{IN} for specific voltage gains in three operating modes.

$$A_V = \frac{425}{R_{IN}+20}, \quad \text{for Mode-1} \qquad (1)$$

$$A_V = \frac{300}{R_{IN}+20}, \quad \text{for Mode-2, 3, 4} \qquad (2)$$

Operating Mode	R_{IN} (kΩ)	0	3.3	6.8	10	14	18	22
Mode-1	A_V (V/V)	21	18	16	14	12.5	11	10
	A_V (dB)	26	25	24	23	22	21	20
Mode-2, 3, 4	A_V (V/V)	15	13	11	10	9	8	7
	A_V (dB)	23	22	21	20	19	18	17

Table 3: Example Resistor Values of R_{IN} for Specific Voltage Gains

The choice of the voltage gain will highly influence the loudness and quality of audio sounds. In general, the higher the voltage gain is, the louder the sound is perceived. However an excessive voltage gain may cause the audio outputs to be severely compressed or clipped for high-level (loud) audio sounds. On the other hand, an unusually low gain may cause relatively low-level (quiet) sounds soft or inaudible. Thus it is crucial to choose a proper voltage gain for high audio quality.

The voltage gain is chosen based upon various system-level considerations including the boosted supply voltage, maximum input level of the audio source, output power rating, and desired sound effect. As an example, Table 4 shows the voltage gains for various audio input levels. In the table, R_{IN} is the external input resistor in series with the input capacitor. Typically, the voltage gain of audio amplifiers is set between 26dB (21X) and 17dB (7X), which corresponds to an external input resistor between 0Ω (in Mode-1) and 22kΩ (in Mode-2, 3, 4), respectively.

$V_{IN, MAX}$ (V_{RMS})	R_{IN} (kΩ)	Operating Mode	Class-G Output	
			A_V (V/V)	A_V (dB)
0.35	3.3	Mode-1	18	25
0.50	14	Mode-1	13	22
	3.3	Mode-2	13	22
0.70	14	Mode-2	9	19
1.0	22	Mode-2	7	17

Table 4: Example Voltage Gain Settings for Various Audio Input Levels

The voltage gain can be also expressed in Equation 3. In the equation, $V_{IN, MAX}$ (in V_{RMS}) is the maximum input level of the audio source, PVDD (in volts) is the boosted supply voltage, and α is a design parameter that determines the ALC dynamic range (maximum attention) and typically ranges from 0.65 to 1.2. Higher α values result in wider ALC range (maximum attenuation) and higher average output power (loudness) with some degree of compression for high-level audio sounds. Conversely, lower α values result in narrower ALC range and lower average output power (loudness) with minimum or no compression for high-level audio sounds.

$$A_V = \frac{\alpha \times PVDD}{V_{IN, MAX}} \quad (3)$$

AUTOMATIC LEVEL CONTROL (ALC)

The automatic level control is to maintain the audio outputs for a maximum voltage swing without clipping distortion when an excessive input that may cause output clipping is applied. With ALC, the ft2815 lowers the voltage gain of the amplifier to an appropriate value such that output clipping is substantially eliminated.

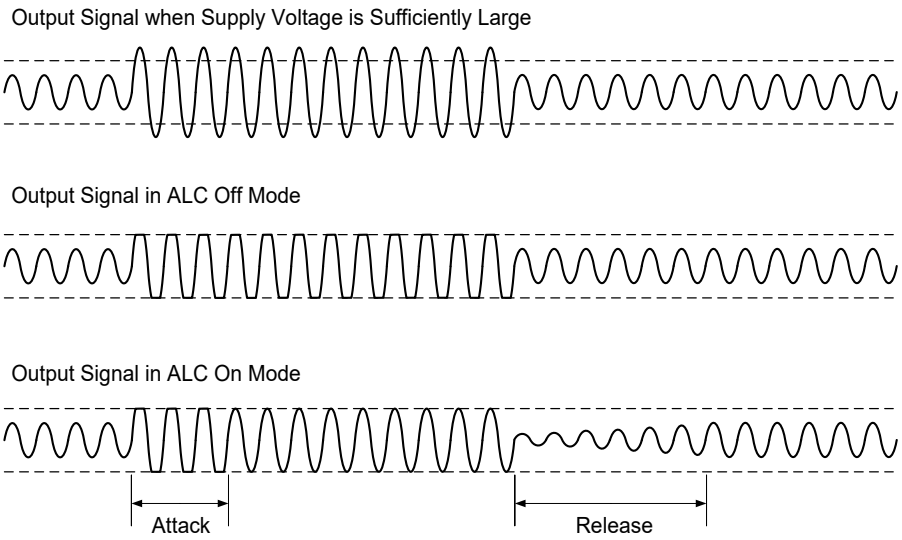


Figure 34: Automatic Level Control (ALC) Function Diagram

Attack is where the voltage gain of the audio amplifier decreases until output clipping is substantially eliminated. Release is where the voltage gain of the audio amplifier recovers (increases) until it reaches to a value that is maximally allowed without output clipping.

ALC MODE CONTROL

When operating in Mode-1, 2, or 3, the device can be configured in ALC or Non-ALC mode via the ALC pin, as described in Table 5. When the ALC pin is shorted to VDD through a 10kΩ resistor, the ft2815 operates in Non-ALC mode. The Non-ALC operation is typically chosen for applications where maximum audio loudness is much desired and the amount of output clipping distortions can be reliably controlled at the audio source. In other ALC pin configurations, the ft2815 operates in ALC mode with one of three audio dynamic characteristics. For most applications, the ALC mode of operation is preferred for its capability to substantially eliminate output clipping distortion, excessive power dissipation, and speaker over-load.

Three sets of ALC dynamic characteristics can be selected for specific sound effects, as described in Table 5. The ALC-3 mode (ALC pin unconnected) tends to play music in a most dynamic manner with some extent of clipping distortion and higher average output power (loudness). Conversely, the ALC-1 mode (ALC pin shorted to GND) tends to play music in a most mellow manner with negligible amount of clipping distortion and lower average output power.

The ALC pin and its associated control are activated only when the device operates in Mode-1, 2, or 3. In Mode-4, the ALC control is disabled, regardless of the ALC pin configuration.

ALC Pin Configuration	ALC Mode	Sound Effects	
		Loudness (Sound Pressure)	Output Clipping Distortion
10kΩ to VDD	Non-ALC	Potentially highest loudness	No control on output clipping
Unconnected	ALC-3	Most dynamic sound (Highest loudness under ALC)	Acceptable output clipping
51kΩ to GND	ALC-2	Medium loudness	Slight output clipping
Short to GND	ALC-1	Most mellow sound (Lowest loudness under ALC)	Minimum output clipping

Table 5: ALC Mode Control

SHUTDOWN AND STARTUP

The ft2815 employs CTRL pin to minimize power consumption while it is not in use. When the CTRL pin is pulled to ground for more than 0.25 milliseconds (T_{SHDN}, Shutdown Time), the ft2815 is forced into shutdown mode and initiates a process of shutdown. At the end of the shutdown process, all the analog circuitry is de-biased, the supply current is reduced to be less than 1μA, and the differential outputs are individually shorted to ground through internal resistors (2kΩ). Once in shutdown mode, the CTRL pin must remain low for at least 5

milliseconds (T_{SD}, Shutdown Settling Time) before it can be brought high. Once the CTRL pin is brought high again, the ft2815 exits out of shutdown mode and resumes normal operation after the startup time (T_{STUP}) of 40 milliseconds.

Note that an internal pulldown resistor of 300kΩ is included onto the CTRL pin. Thus, shutdown mode is the state when the power supply is first applied to the device.

It is recommended to assert CTRL high to exit the device out of shutdown mode only after the device is properly powered up. Also, place the amplifier in shutdown mode prior to removing the supply voltage.

CLICK-AND-POP SUPPRESSION

The audio power amplifier in ft2815 features comprehensive click-and-pop suppression. During startup, the click-and-pop suppression circuitry reduces audible transients internal to the device. When entering into shutdown mode, the differential audio outputs ramp down to ground quickly and simultaneously.

BYPASS PIN

A reference voltage is internally generated and provided to the BYP pin. Add a 0.1μF low-ESR ceramic capacitor to the pin.

PROTECTION MODES

Against various operating faults for safe and reliable operation, the ft2815 features comprehensive protection modes including Under-Voltage Lockout (UVLO), Over-Current Protection (OCP), and Over-Temperature Shutdown (OTSD).

Under-Voltage Lockout (UVLO)

The ft2815 incorporates circuitry to detect a low supply voltage. When the supply voltage is first applied, the ft2815 remains inactive until the supply voltage exceeds 2.2V (V_{UVLU}). When the supply voltage is removed and drops below 2.0V (V_{UVLD}), the ft2815 enters into shutdown mode immediately.

Over-Temperature Shutdown (OTSD)

When the die temperature exceeds a preset threshold (160°C), the device enters into over-temperature shutdown mode, where two differential outputs are pulled to ground through an internal resistor (2kΩ) individually. The device will resume a normal operation once the die temperature returns to a lower temperature, which is about 20°C lower than the threshold.

Over-Current Protection (OCP)

During operation, the ft2815 constantly monitors the output of Class-D audio amplifier for any over-current or short-circuit conditions. When a short-circuit condition between two differential outputs, differential output to PVDD or ground is detected, the output stage of the amplifier is immediately forced into high impedance state. Once the fault condition persists over a prescribed period, the ft2815 then enters into shutdown mode and remains in this mode for about 200 milliseconds. During shutdown, the power switches of the charge pump regulator are also turned off, and the PVDD is discharged through an internal resistor to ground.

When shutdown mode times out, the ft2815 will initiate another startup sequence and then check if the short-circuit condition has been removed. Meanwhile, the charge pump regulator tries to bring PVDD up to the preset voltage again. If the fault condition is still present, the ft2815 will repeat itself for the process of a startup followed by detection, qualification, and shutdown. It is the so-called hiccup mode of operation. Once the fault condition is removed, the ft2815 automatically restores to its normal mode of operation.

Although the output stage of the Class-D audio amplifier can withstand a short between VOP and VON, do not connect either output directly to GND, VDD, PVDD, or PVOUT as this might damage the device permanently.

CLASS-D AUDIO AMPLIFIER

The Class-D audio amplifier in ft2815 operates in much the same way as traditional Class-D amplifiers and similarly offers much higher power efficiency than Class-AB amplifiers. The high efficiency of Class-D operation is achieved by the switching operation of the output stage of the amplifier. The power loss associated with the output stage is limited to the conduction and switching loss of the power switches, which are much less than the power loss associated with a linear output stage in Class-AB amplifiers.

Fully Differential Amplifier

The ft2815 includes a fully differential amplifier with differential inputs and outputs. The fully differential amplifier ensures that the differential output voltage is equal to the differential input voltage times the amplifier gain. Although the ft2815 supports for a single-ended input, differential inputs are much preferred for applications where the environment can be noisy in order to ensure maximum SNR.

Low-EMI Filterless Output Stage

Traditional Class-D amplifiers require a LC output filter to recover the audio signal from the amplifier's output. The filter adds cost, increases the solution size of the amplifier, and can adversely affect efficiency and THD+N performance.

The ft2815 does not require an output filter. The device relies on the inherent inductance of the speaker coil and the natural filtering of both the speaker and the human ear to recover the audio component of the square-wave output. By eliminating the output filter, a smaller, less costly, and more efficient solution can be accomplished.

Because the frequency of the ft2815 output is well beyond the bandwidth of most speakers, voice coil movement due to the square-wave frequency is very small. Although this movement is small, a speaker not designed to handle the additional power can be damaged. For optimal performance, use a speaker with a series inductance greater than 10μH. Typical 4Ω speakers exhibit series inductances in the range from 10μH to 47μH.

Ferrite Bead EMI Filter

The ft2815 does not require LC output filters for connections from the amplifier to the speaker. However, EMI emission can be further suppressed by use of a simple ferrite bead filter comprising a ferrite bead and a capacitor, as shown in Figure 35. Choose a ferrite bead with low DC resistance (DCR) and high impedance (100Ω ~ 470Ω) at high frequencies (>100MHz). The current flowing through the ferrite bead must be also taken into consideration. The effectiveness of ferrites can be greatly aggravated at much lower than the rated current values. Choose a ferrite bead with a rated current value no less than 3A. The capacitor value varies based on the ferrite bead chosen and the actual speaker lead length. Choose a capacitor less than 1nF based on EMI performance. Place each ferrite bead filter tightly together and individually close to VOP and VON pins respectively.

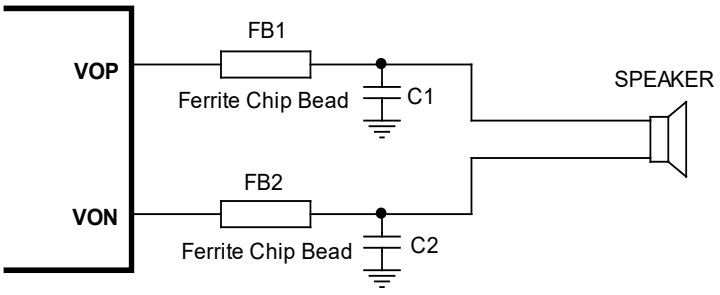


Figure 35: Ferrite Bead Filter to Reduce EMI

Class-D Output RC Snubber Circuit

For applications where speaker load resistances are 4Ω or less with long speaker wires, it may become necessary to add a snubber circuit across the two output pins, VOP and VON, to prevent the device from accelerated deterioration or abrupt destruction due to excessive inductive flybacks that are induced on fast output switching or by an over-current or short-circuit condition. The snubber circuit can also help lower EMI emission of Class-D outputs.

Figure 36 shows a simple RC snubber circuit with suggested values of R_3 in the range of 2.2Ω ~ 4.7Ω and C_3 in the range of 3.3nF ~ 4.7nF. Generally, a higher C_3 is more effective to lower the voltage spikes (overshoots and undershoots) at VOP and VON pins, however, at the expense of efficiency degradation. The actual R_3 and C_3 values used for the snubber circuit are specific to each individual design and must take into account the parasitic reactance of the system board to reach proper values of R_3 and C_3. As a good starting point, use R_3=3.3Ω and C_3=3.3nF for evaluation to ensure that the voltage spikes at VOP and VON pins on the actual system board are well within their absolute maximum ratings and that the aggravated degradation in efficiency is acceptable. Pay close attention to the layout of the RC snubber circuit to be tight and close to VOP and VON pins.

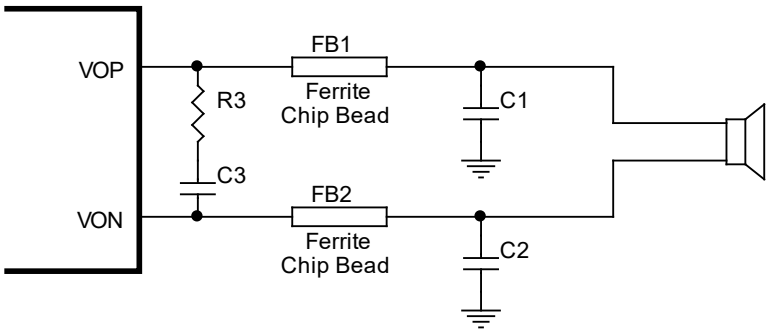


Figure 36: Class-D Output RC Snubber Circuit

Input Resistors (R_{IN})

In ft2815, a pair of 20kΩ input resistors is internally integrated onto INP and INN pins individually. Internal input resistors bring such benefits as fewer variations on PSRR and minimum turn-on pop noise since on-chip resistors tend to match well. Additional input resistors can be externally added onto INP and INN pins respectively to fine-adjust for a specific voltage gain. The value of external input resistors must be included in the calculation of overall voltage gain, as described in Equation 4, as well as the selection of proper input capacitors, as described in Equation 5. As shown in Equation 4, the external input resistors attenuate the original voltage gain by the ratio of [$R_{INTERNAL}$ / (R_{IN}+$R_{INTERNAL}$)], where $R_{INTERNAL}$=20kΩ.

$$A_V = A_{V0} \times [\, R_{INTERNAL} / (R_{IN} + R_{INTERNAL}) \,] \qquad (4)$$

where A_{V0} = 21X (26dB), for Mode-1

and A_{V0} = 15X (23dB), for Mode-2, 3, 4

Input Capacitors (C_{IN})

Input DC decoupling capacitors for audio inputs are recommended. The input DC decoupling capacitors will remove the DC bias from audio inputs. The input capacitor C_{IN} and input resistors (R_{IN} plus $R_{INTERNAL}$) form a highpass filter with the corner frequency, $f_{C,\,HPF}$ defined in Equation 5. In the equation, R_{IN} is the external input resistor and $R_{INTERNAL}$ is the internal input resistor of 20kΩ.

$$f_{C,\,HPF} = \frac{1}{2 \times \pi \times (R_{IN} + R_{INTERNAL}) \times C_{IN}} \qquad (5)$$

It is noted that variations of the external input resistance affect the voltage gain A_V as well as the corner frequency $f_{C,\,HPF}$. Choose R_{IN} with a tolerance of 2% or better, if possible.

Choose C_{IN} such that the f_C is well below the lowest frequency of interest. Setting f_C too high affects the low frequency response of the amplifier. Consider an example where the specification calls for A_V=23dB and a flat frequency response down to 10Hz. Assume that the device is configured in Mode-1 and R_{IN}=10kΩ, C_{IN} is calculated to be 0.53μF; thus 0.47μF, as a common choice of capacitances, can be chosen for C_{IN}.

Any mismatch in resistance or capacitance between two audio inputs will cause a mismatch in the corner frequencies. Severe mismatch of external components may also cause turn-on/off pop noise or PSRR, CMRR performance degradation. Choose C_{IN} with a tolerance of ±2% or better, if possible.

The impedance seen at two audio inputs shall be limited to an $R_{IN}C_{IN}$ time constant less than 5 milliseconds, thus allowing C_{IN} to be fully charged during the startup time of 40 milliseconds. If the input capacitors C_{IN} are not fully charged during the startup time, mismatch in resistance or capacitance between two audio inputs may cause pop noise.

For best noise performance, use differential inputs from the audio source. In single-ended input applications, the unused inputs of ft2815 must be AC-grounded to the ground at the audio source.

PRINTED CIRCUIT BOARD (PCB) LAYOUT CONSIDERATIONS

Ground Plane - It is required to use a solid metal plane with sufficiently wide area as a central ground connection (GND) for ft2815. The power ground pins, CGND and PGND, are directly shorted to the ground plane GND, which serves as a central “star” ground for ft2815. Use a single point of connection between the analog ground AGND and the ground plane to minimize the coupling of high-current switching noise onto audio signals.

Supply Decoupling Capacitors – Place a 10μF low-ESR ceramic capacitor C_{VDD1} as close as possible to the VDD pin. Also, in tandem, add a small low-ESR ceramic capacitor of 0.1μF for high-frequency decoupling. For higher audio output power (2W or greater) applications, place an additional bulk electrolytic capacitor C_{VDD2} (100μF or greater) in tandem with C_{VDD1}.

Boosted Supply Decoupling Capacitors – Place a 1μF, 16V low-ESR ceramic capacitor C_{PVDD} as close as possible to the PVDD pin. Also, in tandem, add a small low-ESR ceramic capacitor of 0.01μF for high-frequency decoupling.

Charge Pump Flying Capacitor – Place a 4.7μF low-ESR ceramic capacitor C_F as close as possible to CP and CN pins.

Charge Pump Output Capacitors - Place a 10μF, 16V low-ESR ceramic capacitor C_{PVOUT1} as close as possible to the PVOUT pin. In tandem, add a small low-ESR ceramic capacitor of 0.1μF for high-frequency decoupling. For higher audio output power (2W or greater) applications, place an additional bulk electrolytic capacitor C_{PVOUT2} (220μF or greater) in tandem with C_{PVOUT1}.

Ferrite Bead EMI Filter – The ferrite bead EMI filters should be placed tightly together and individually close to the audio output pins, VOP and VON respectively. For best EMI performance, keep the current loop, traversing from each of the audio outputs through the ferrite bead, the small filter capacitor, and back to PGND, as short as possible.

Class-D Output RC Snubber – Place the RC snubber circuit tightly together and close to VOP and VON pins.

Power Dissipation - The maximum output power of ft2815 can be severely limited by its thermal dissipation capability. To ensure the device operating properly and reliably at its maximum output power without incurring over-temperature shutdown, the following guidelines are given for optimum thermal dissipation capability:

- Fill both top and bottom layers of the system board with solid GND metal traces.
- Solder the thermal pad directly onto a grounded metal plane.
- Place lots of equally-spaced vias underneath the thermal pad connecting the top and bottom layers of GND. The vias are connected to a solid metal plane on the bottom layer of the board.
- Reserve wide and uninterrupted areas along the thermal flow on the top layer, i.e., no wires cutting through the GND layer and obstructing the thermal flow.
- Place the Input/output capacitors of the charge pump regulator tightly together and on the same layer of the board with ft2815.
- Avoid using vias for traces carrying high current.

TYPICAL APPLICATION CIRCUITS

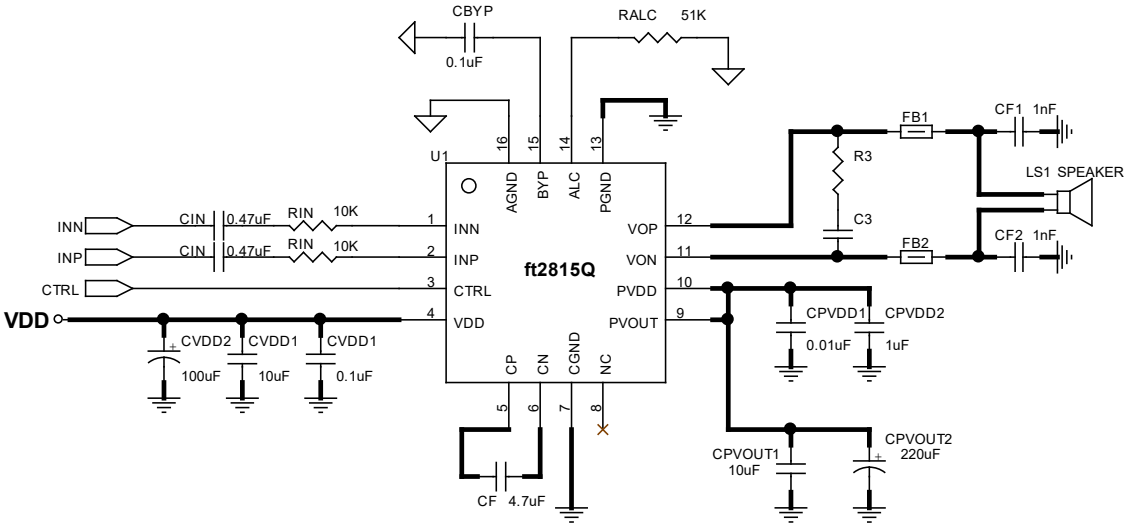


Figure 37: Differential Audio Inputs in ALC-2 Mode

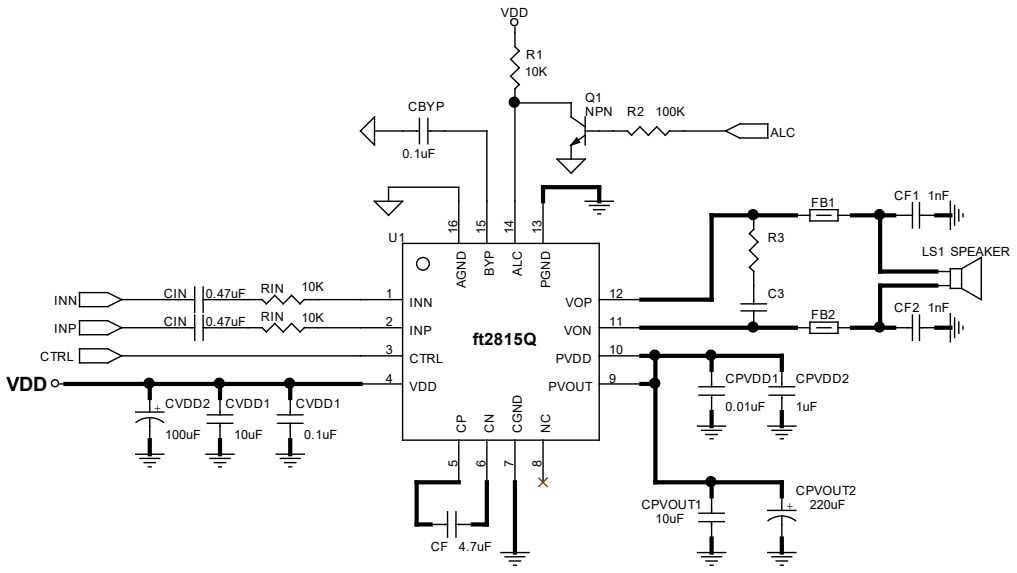
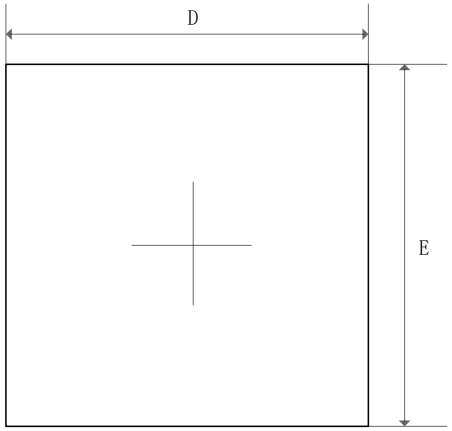


Figure 38: Differential Audio Inputs with Selectable Non-ALC/ALC-1 Mode

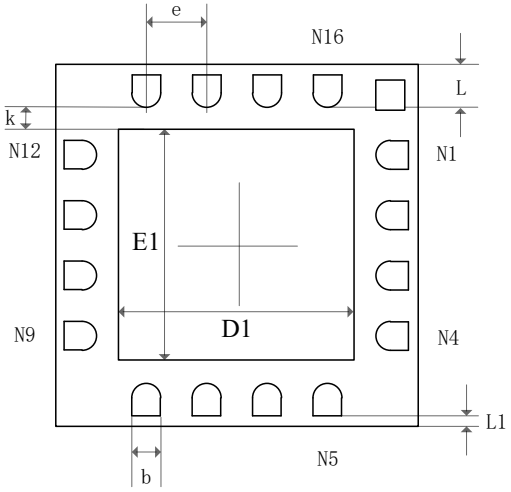
Note: The bold lines indicate high current paths and their respective traces are required to be as wide and short as possible on the system board for high power applications.

PHYSICAL DIMENSIONS

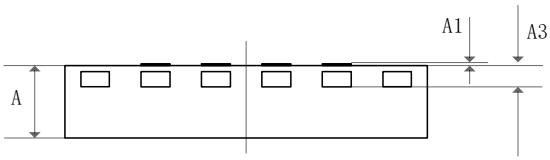
QFN3x3-16L PACKAGE OUTLINE DIMENSIONS



Top View



Bottom View



Side View

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	0.450/0.500/0.550	0.550/0.600/0.650	0.018/0.020/0.022	0.022/0.024/0.026
A1	0.000	0.050	0.000	0.002
A3	0.152REF.		0.006REF.	
D	2.924	3.076	0.115	0.121
E	2.924	3.076	0.115	0.121
D1	1.800	2.000	0.071	0.079
E1	1.800	2.000	0.071	0.079
k	0.200MIN.		0.008MIN.	
b	0.230	0.330	0.009	0.013
e	0.500TYP.		0.020TYP.	
L	0.250	0.350	0.010	0.014
L1	0.013	0.113	0.000	0.004

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CONTACT INFORMATION

Fangtek Electronics (Shanghai) Co., Ltd

Room 501A, No.10, Lane 198, Zhangheng Road

Zhangjiang Hi-tech Park, Pudong District

Shanghai, China, 201204

Tel: +86-21-61631978

Fax: +86-21-61631981

Website: www.fangtek.com.cn