

SCTH40N120G2V7AG-VB Datasheet
N-Channel 1200V (D-S) SiC Power MOSFET

PRODUCT SUMMARY		
V _{DS} (V) at T _J max.	1200	
R _{DS(on)} at 25 °C (Ω)	V _{GS} = 18 V	0.080
Q _g (nC)	78	

FEATURES

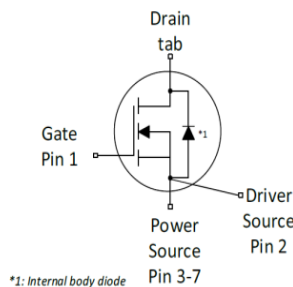
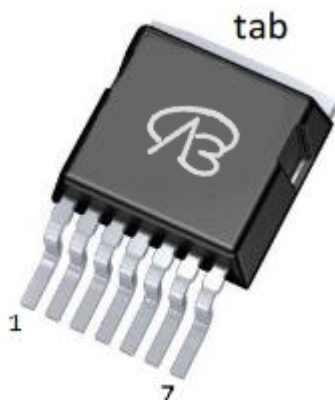
- Low figure-of-merit (FOM) R_{on} x Q_g
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)



APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- DC/DC converter

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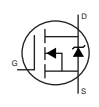


ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	V _{DS}	1200	V	
Gate-Source Voltage	V _{GS}	-10 / +22		
Continuous Drain Current (T _J = 150 °C)	V _{GS} at 18 V	T _C = 25 °C	30	A
		T _C = 100 °C	21	
Pulsed Drain Current ^a	I _{DM}	90		
Linear Derating Factor		2.1	W/°C	
Single Pulse Avalanche Energy ^b	E _{AS}	60	mJ	
Maximum Power Dissipation	P _D	150	W	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +175	°C	
Drain-Source Voltage Slope	dV/dt	T _J = 125 °C	50	V/ns
Reverse Diode dV/dt ^d		15		
Soldering Recommendations (Peak Temperature) ^c	for 10 s	260	°C	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- V_{DD} = 100 V, starting T_J = 25 °C, L = 30mH, R_g = 25 Ω, I_{AS} = 20A.
- 1.6 mm from case.
- I_{SD} ≤ I_D, dI/dt = 100 A/μs, starting T_J = 25 °C.

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.0	

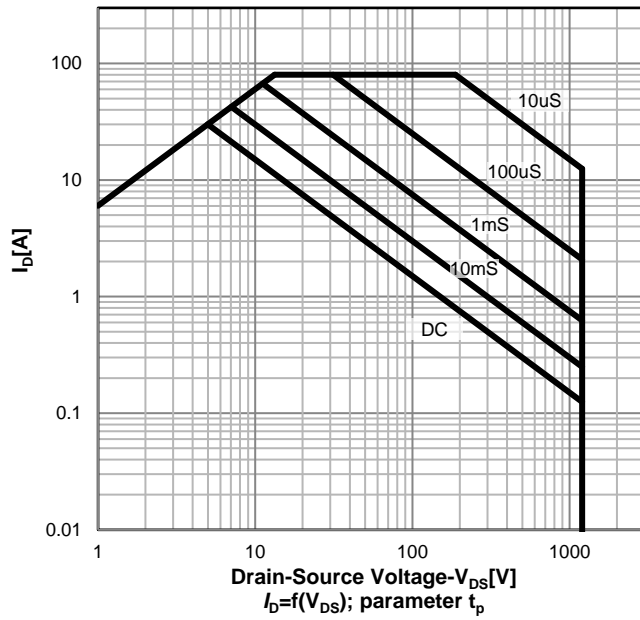
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$		1200	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$		-	0.70	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 10\text{ mA}$		2.5	-	4.5	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = +22\text{ V}$		-	-	100	nA
		$V_{GS} = -10\text{ V}$		-	-	100	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 1200\text{ V}, V_{GS} = 0\text{ V}$		-	10	-	μA
		$V_{DS} = 1200\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	100	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 18\text{ V}$	$I_D = 15\text{ A}$	-	0.080	-	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 0\text{ V}, I_D = 15\text{ A}$		-	16	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 800\text{ V}, f = 1\text{ MHz}$		-	2800	-	pF
Output Capacitance	C_{oss}			-	123	-	
Reverse Transfer Capacitance	C_{rss}			-	10	-	
Effective Output Capacitance, Energy Related ^a	$C_{o(er)}$	$V_{DS} = 0\text{ V to } 800\text{ V}, V_{GS} = 0\text{ V}$		-	156	-	
Effective Output Capacitance, Time Related ^b	$C_{o(tr)}$			-	268	-	
Total Gate Charge	Q_g	$V_{GS} = -5/18\text{ V}$	$I_D = 20\text{ A}, V_{DS} = 800\text{ V}$	-	78	-	nC
Gate-Source Charge	Q_{gs}			-	29	-	
Gate-Drain Charge	Q_{gd}			-	33	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 800\text{ V}, I_D = 20\text{ A}, V_{GS} = -5/18\text{ V}, R_g = 2\text{ }^\Omega$		-	18	25	ns
Rise Time	t_r			-	24	55	
Turn-Off Delay Time	$t_{d(off)}$			-	80	-	
Fall Time	t_f			-	12	-	
Gate Input Resistance	R_g	$f = 1\text{ MHz}, \text{ open drain}$		-	3.2	-	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	30	A
Pulsed Diode Forward Current	I_{SM}			-	-	90	
Diode Forward Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 30\text{ A}, V_{GS} = 0$		-	-	4.1	V
Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = I_S = 30\text{ A}, di/dt = 1000\text{ A}/\mu\text{s}, V_R = 800\text{ V}$		-	15	-	ns
Reverse Recovery Charge	Q_{rr}			-	120	-	μC
Reverse Recovery Current	I_{RRM}			-	60	-	A

Notes

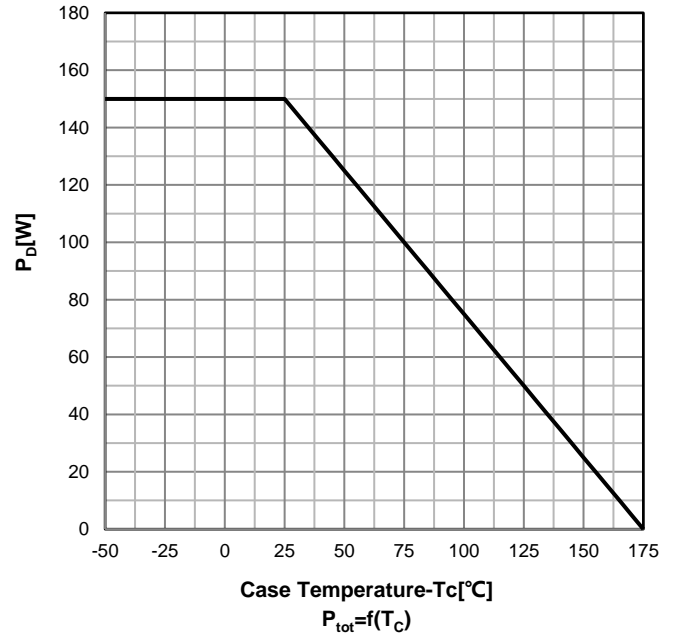
- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .
- b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .

Typical Performance Characteristics

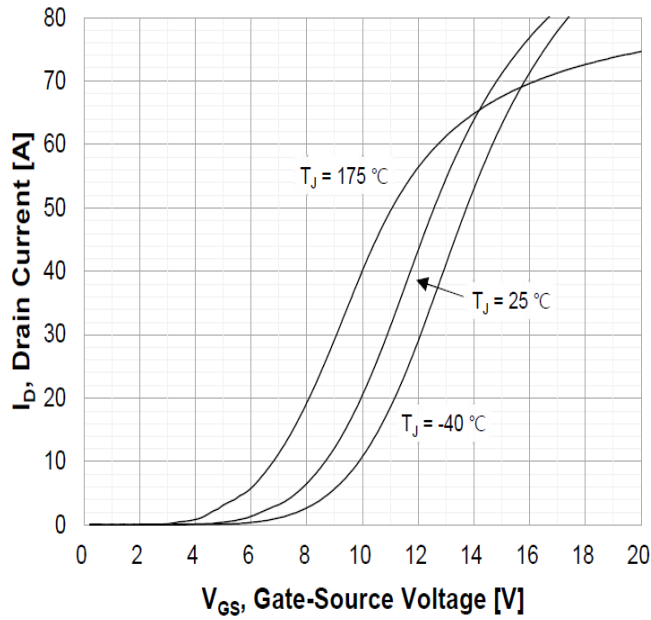
Safe operating area $T_c=25\text{ }^\circ\text{C}$



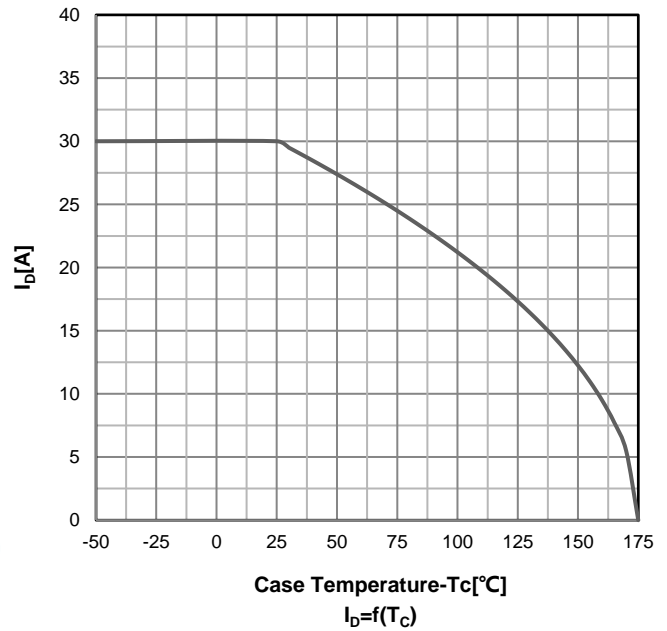
Power dissipation



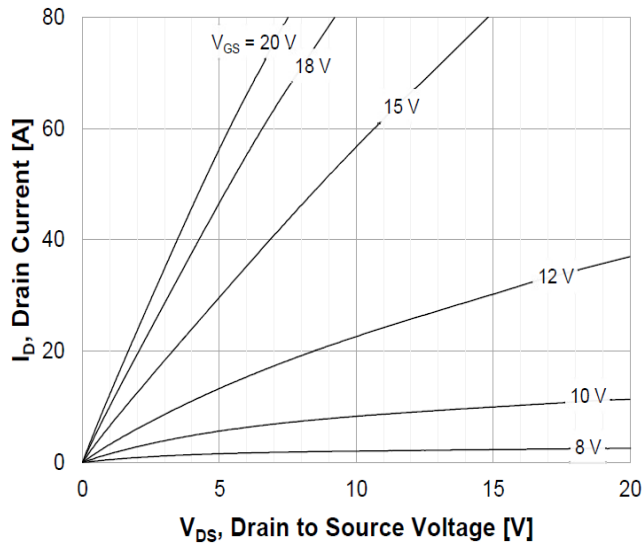
Transfer characteristics



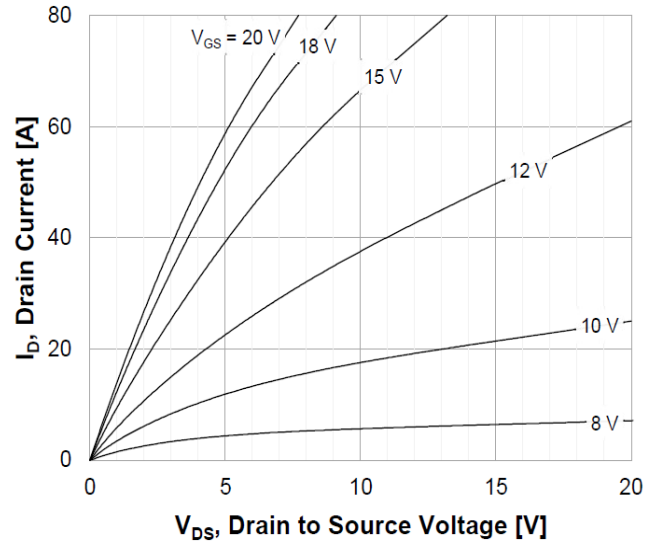
Drain current vs temperature



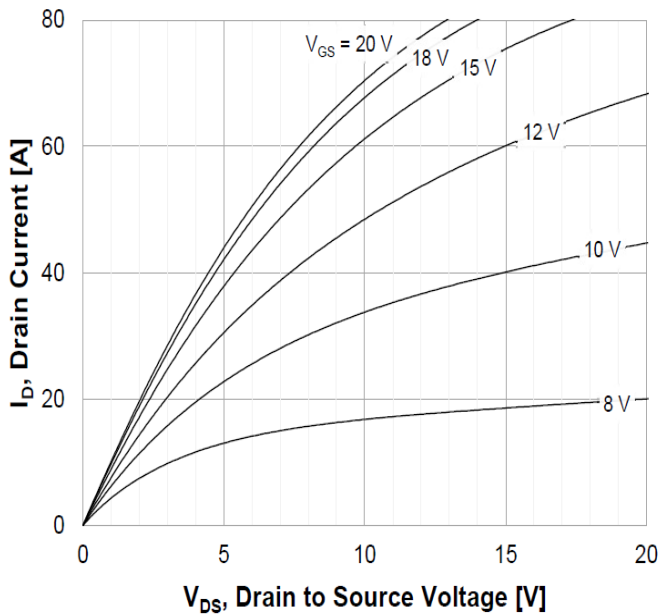
On-Region characteristics $T_j = -40\text{ }^\circ\text{C}$



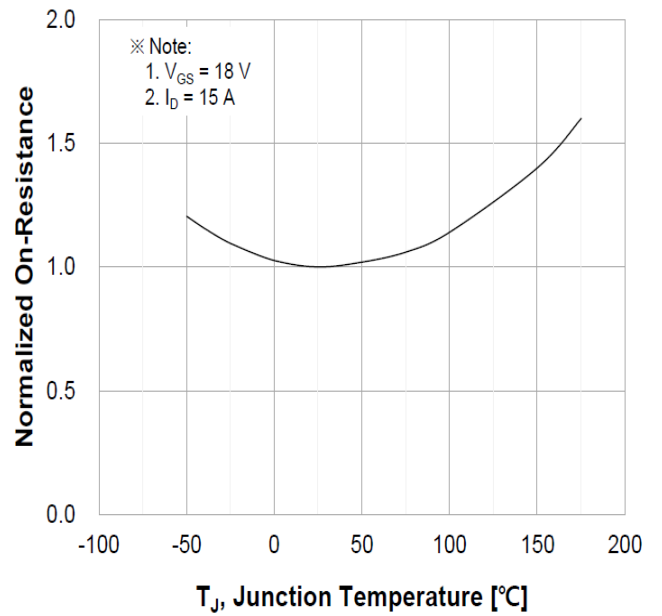
On-Region characteristics $T_j = 25\text{ }^\circ\text{C}$



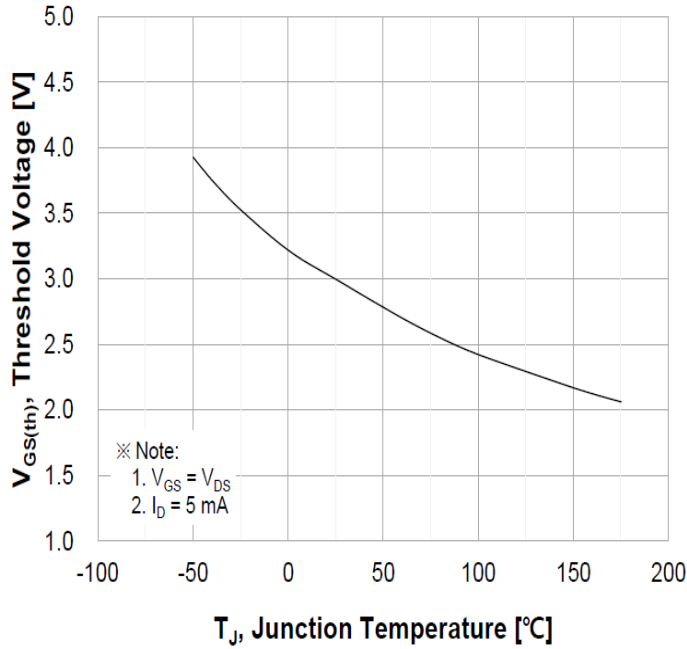
On-Region characteristics $T_j = 175\text{ }^\circ\text{C}$



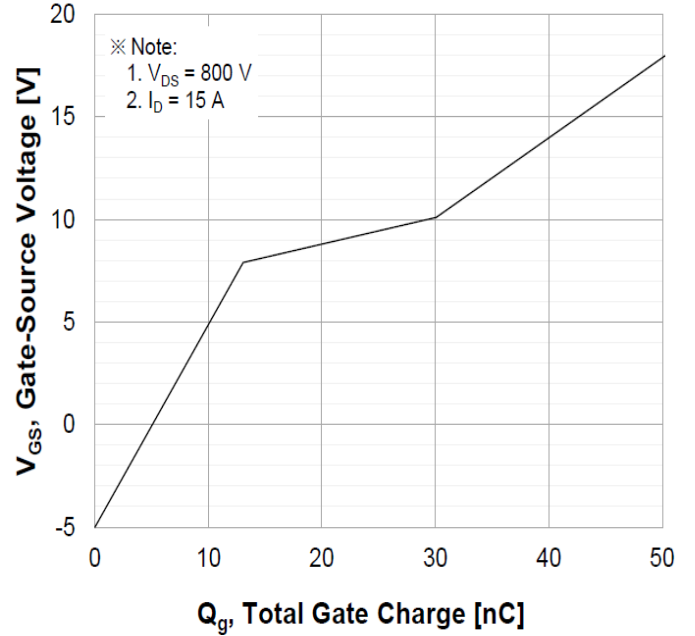
Normalized On-resistance vs temperature



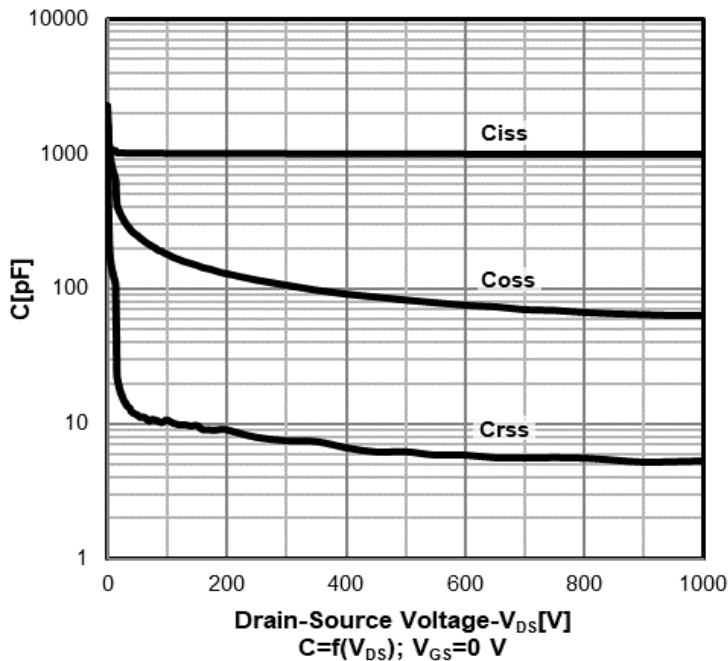
Threshold voltage vs temperature



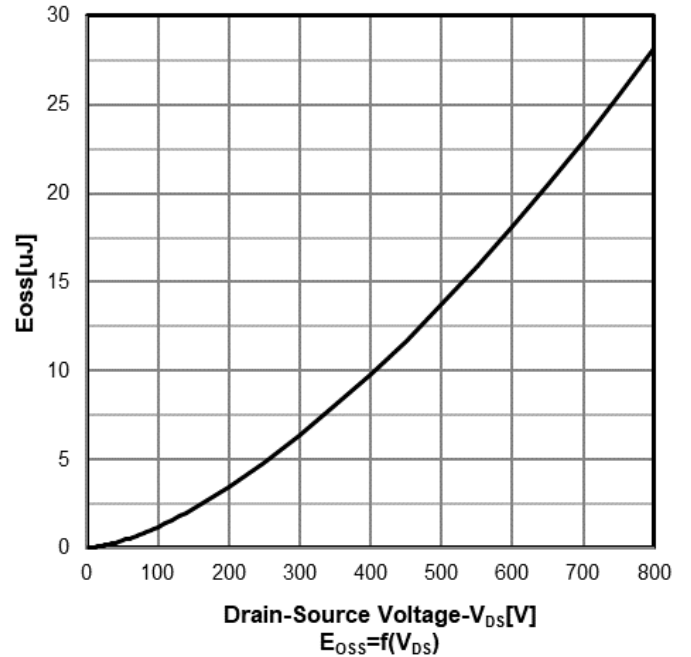
Typ. gate charge characteristics



Typ. capacitances

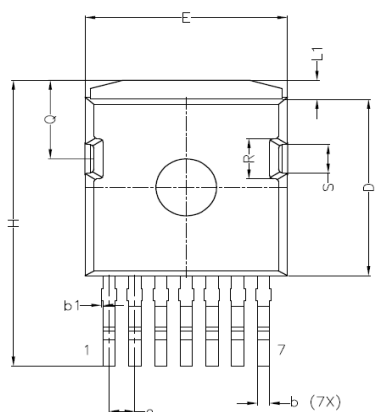


Coss stored energy

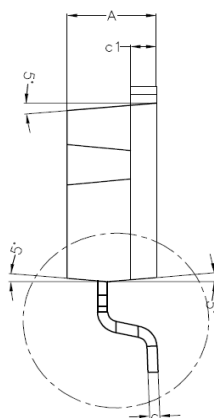


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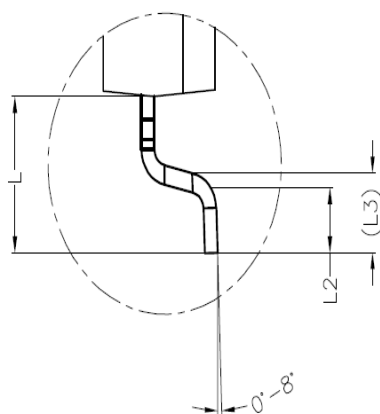
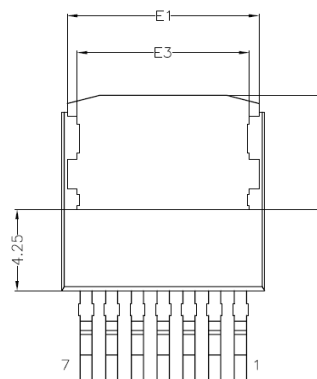
TOP VIEW



SIDE VIEW



BOTTOM VIEW



COMMON DIMENSIONS

SYMBOL	UNIT(mm)	
	MIN	MAX
A	4.30	4.50
b	0.5	0.7
b1	0.0	0.15
c	0.4	0.6
c1	1.17	1.37
D	9.05	9.45
D1	5.9	6.1
E	9.8	10.2
E1	9.36	9.56
E3	8.4	8.6
e	1.27BSC	
H	15.0BSC	
L	4.2	5.2
L1	0.7	1.3
L2	1.7	2.3
L3	2.70BSC	
Q	4.02	4.22
R	2.03	2.23
S	1.4	1.6

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