

**TM4100EAD9**  
**4 194 304 BY 9-BIT**  
**DYNAMIC RAM MODULE**

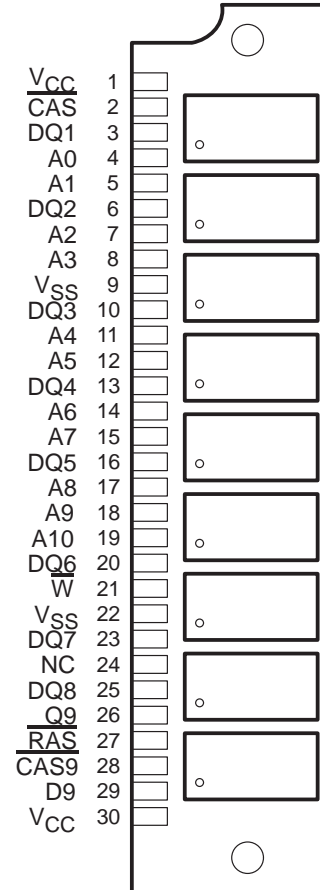
SMMS419C – NOVEMBER 1991 – REVISED JUNE 1995

- Organization . . . 4 194 304 × 9
- Single 5-V Power Supply ( $\pm 10\%$  Tolerance)
- 30-Pin Single In-Line Memory Module (SIMM) for Use With Sockets
- Utilizes Nine 4-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead Packages (SOJs)
- Long Refresh Period  
16 ms (1024 Cycles)
- All Inputs, Outputs, and Clocks Fully TTL Compatible
- 3-State Outputs
- Performance Ranges:

	ACCESS TIME (t <sub>RAC</sub> )  (MAX)	ACCESS TIME (t <sub>CAC</sub> )  (MAX)	ACCESS TIME (t <sub>AA</sub> )  (MAX)	READ OR WRITE CYCLE  (MIN)
'4100EAD9-60	60 ns	15 ns	30 ns	110 ns
'4100EAD9-70	70 ns	18 ns	35 ns	130 ns
'4100EAD9-80	80 ns	20 ns	40 ns	150 ns

- Common  $\overline{\text{CAS}}$  Control for Eight Common Data-In and Data-Out Lines
- Separate  $\overline{\text{CAS}}$  Control for One Separate Pair of Data-In and Data-Out Lines
- Low Power Dissipation
- Operating Free-Air Temperature Range  
0°C to 70°C

**SINGLE IN-LINE MODULE  
(TOP VIEW)**



**description**

The TM4100EAD9 is a dynamic random-access memory module organized as 4 194 304 × 9 [bit nine (D9, Q9) is generally used for parity and is controlled by  $\overline{\text{CAS9}}$ ] in a 30-pin leadless single in-line memory module (SIMM).

This module is composed of nine TMS44100DJ, 4 194 304 × 1-bit dynamic RAMs (DRAMs) each in a 20/26-lead plastic small-outline J-lead package (SOJ) mounted on a substrate with decoupling capacitors.

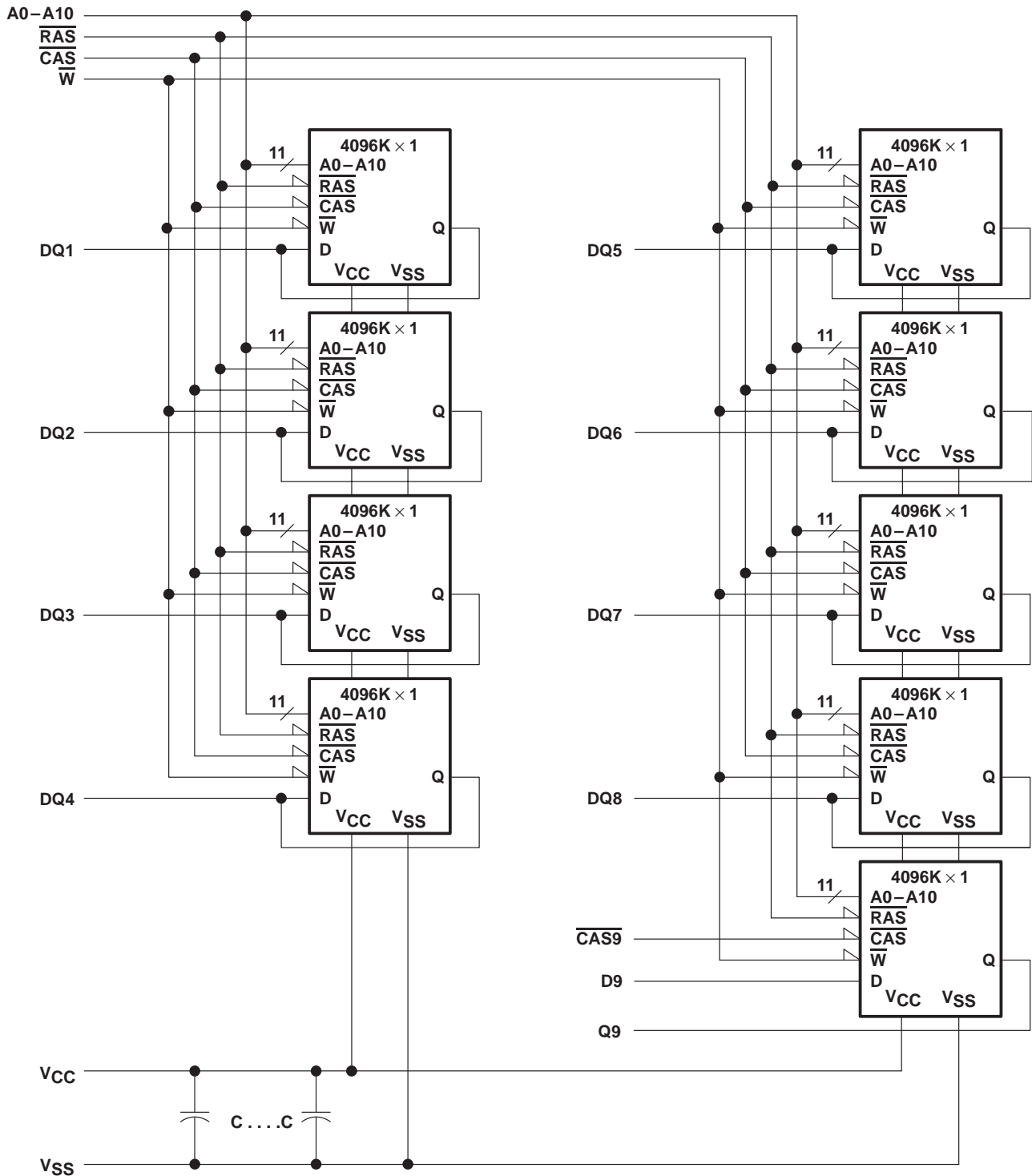
The TM4100EAD9 is characterized for operation from 0°C to 70°C and is available in the AD single-sided, leadless module for use with sockets.

PIN NOMENCLATURE	
A0–A10	Address Inputs
$\overline{\text{CAS}}$ , $\overline{\text{CAS9}}$	Column-Address Strobe
DQ1–DQ8	Data In/Data Out
D9	Data In
NC	No Internal Connection
Q9	Data Out
$\overline{\text{RAS}}$	Row-Address Strobe
V <sub>CC</sub>	5-V Supply
V <sub>SS</sub>	Ground
$\overline{\text{W}}$	Write Enable

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



**functional block diagram**



## operation

The TM4100EAD9 operates as nine TMS44100DJs connected as shown in the functional block diagram. Refer to the TMS44100 data sheet for details of its operation. The common I/O feature of the TM4100EAD9 dictates the use of early-write cycles to prevent contention on D and Q.

## single in-line memory module and components

PC substrate: 1,27 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage

Bypass capacitors: Multilayer ceramic

Contact area for socketable devices: Nickel plate and solder plate over copper

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Voltage range on any pin (see Note 1)	– 1 V to 7 V
Voltage range on V <sub>CC</sub> (see Note 1)	– 1 V to 7 V
Short-circuit output current	50 mA
Power dissipation	9 W
Operating free-air temperature range, T <sub>A</sub>	0°C to 70°C
Storage temperature range, T <sub>stg</sub>	– 55°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V<sub>SS</sub>.

**recommended operating conditions**

	MIN	NOM	MAX	UNIT
V <sub>CC</sub> Supply voltage	4.5	5	5.5	V
V <sub>IH</sub> High-level input voltage	2.4		6.5	V
V <sub>IL</sub> Low-level input voltage (see Note 2)	– 1		0.8	V
T <sub>A</sub> Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	'4100EAD9-60		'4100EAD9-70		'4100EAD9-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub> High-level output voltage	I <sub>OH</sub> = – 5 mA	2.4		2.4		2.4		V
V <sub>OL</sub> Low-level output voltage	I <sub>OL</sub> = 4.2 mA		0.4		0.4		0.4	V
I <sub>I</sub> Input current (leakage)	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0 V to 6.5 V, All others = 0 V to V <sub>CC</sub>		±10		±10		±10	µA
I <sub>O</sub> Output current (leakage)	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0 V to V <sub>CC</sub> , CAS high		±10		±10		±10	µA
I <sub>CC1</sub> Read- or write-cycle current (see Note 3)	V <sub>CC</sub> = 5.5 V, Minimum cycle		945		810		720	mA
I <sub>CC2</sub> Standby current	After 1 memory cycle, RAS and CAS high, V <sub>IH</sub> = 2.4 V (TTL)		18		18		18	mA
	After 1 memory cycle, RAS and CAS high, V <sub>IH</sub> = V <sub>CC</sub> – 0.2 V (CMOS)		9		9		9	mA
I <sub>CC3</sub> Average refresh current (RAS only or CBR) (see Note 3)	V <sub>CC</sub> = 5.5 V, Minimum cycle, RAS cycling, CAS high (RAS only), RAS low after CAS low (CBR)		945		810		720	mA
I <sub>CC4</sub> Average page current (see Note 4)	V <sub>CC</sub> = 5.5 V, t <sub>PC</sub> = minimum, RAS low, CAS cycling		810		720		630	mA

NOTES: 3. Measured with a maximum of one address change while  $\overline{RAS} = V_{IL}$   
 4. Measured with a maximum of one address change while  $\overline{CAS} = V_{IH}$



capacitance over recommended ranges of supply voltage and operating free-air temperature,  $f = 1 \text{ MHz}$  (see Note 5)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0–A10		45	pF
$C_{i(D)}$	Input capacitance, data input (pin D9)		5	pF
$C_{i(RC)}$	Input capacitance, $\overline{\text{CAS}}$ and $\overline{\text{RAS}}$		63	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		63	pF
$C_{o(DQ)}$	Output capacitance, DQ1–Q8		12	pF
$C_o$	Output capacitance, Q9		7	pF

NOTE 5:  $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	'4100EAD9-60		'4100EAD9-70		'4100EAD9-80		UNIT		
	MIN	MAX	MIN	MAX	MIN	MAX			
$t_{AA}$	Access time from column address		30		35		40	ns	
$t_{CAC}$	Access time from $\overline{\text{CAS}}$ low		15		18		20	ns	
$t_{CPA}$	Access time from column precharge		35		40		45	ns	
$t_{RAC}$	Access time from $\overline{\text{RAS}}$ low		60		70		80	ns	
$t_{CLZ}$	$\overline{\text{CAS}}$ to output in low-impedance		0		0		0	ns	
$t_{OFF}$	Output disable time after $\overline{\text{CAS}}$ high (see Note 6)		0		15		0	15	ns

NOTE 6:  $t_{OFF}$  is specified when the output is no longer driven.

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**timing requirements over recommended ranges of supply voltage and operating free-air temperature**

	'4100EAD9-60		'4100EAD9-70		'4100EAD9-80		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>RC</sub> Cycle time, random read or write (see Note 7)	110		130		150		ns
t <sub>PC</sub> Cycle time, page-mode read or write (see Note 8)	40		45		50		ns
t <sub>RASP</sub> Pulse duration, page mode $\overline{\text{RAS}}$ low (see Note 9)	60	100 000	70	100 000	80	100 000	ns
t <sub>RAS</sub> Pulse duration, nonpage mode, $\overline{\text{RAS}}$ low (see Note 9)	60	10 000	70	10 000	80	10 000	ns
t <sub>CAS</sub> Pulse duration, $\overline{\text{CAS}}$ low (see Note 10)	15	10 000	18	10 000	20	10 000	ns
t <sub>CP</sub> Pulse duration, $\overline{\text{CAS}}$ high	10		10		10		ns
t <sub>RP</sub> Pulse duration, $\overline{\text{RAS}}$ high (precharge)	40		50		60		ns
t <sub>WP</sub> Pulse duration, write	15		15		15		ns
t <sub>ASC</sub> Setup time, column address before $\overline{\text{CAS}}$ low	0		0		0		ns
t <sub>ASR</sub> Setup time, row address before $\overline{\text{RAS}}$ low	0		0		0		ns
t <sub>DS</sub> Setup time, data (see Note 11)	0		0		0		ns
t <sub>RCS</sub> Setup time, read before $\overline{\text{CAS}}$ low	0		0		0		ns
t <sub>CWL</sub> Setup time, $\overline{\text{W}}$ low before $\overline{\text{CAS}}$ high	15		18		20		ns
t <sub>RWL</sub> Setup time, $\overline{\text{W}}$ low before $\overline{\text{RAS}}$ high	15		18		20		ns
t <sub>WCS</sub> Setup time, $\overline{\text{W}}$ low before $\overline{\text{CAS}}$ low (early-write operation only)	0		0		0		ns
t <sub>WSR</sub> Setup time, $\overline{\text{W}}$ high (CBR refresh only)	10		10		10		ns
t <sub>WTS</sub> Setup time, $\overline{\text{W}}$ low (test mode only)	10		10		10		ns
t <sub>CAH</sub> Hold time, column address after $\overline{\text{CAS}}$ low	10		15		15		ns
t <sub>DHR</sub> Hold time, data after $\overline{\text{RAS}}$ low (see Note 12)	50		55		60		ns
t <sub>DH</sub> Hold time, data (see Note 10)	10		15		15		ns
t <sub>AR</sub> Hold time, column address after $\overline{\text{RAS}}$ low (see Note 12)	50		55		60		ns
t <sub>RAH</sub> Hold time, row address after $\overline{\text{RAS}}$ low	10		10		10		ns
t <sub>RCH</sub> Hold time, read after $\overline{\text{CAS}}$ high (see Note 13)	0		0		0		ns
t <sub>RRH</sub> Hold time, read after $\overline{\text{RAS}}$ high (see Note 13)	0		0		0		ns
t <sub>WCH</sub> Hold time, write after $\overline{\text{CAS}}$ low (early-write operation only)	15		15		15		ns
t <sub>WCR</sub> Hold time, write after $\overline{\text{RAS}}$ low (see Note 12)	50		55		60		ns
t <sub>WHR</sub> Hold time, $\overline{\text{W}}$ high (CBR refresh only)	10		10		10		ns
t <sub>WTH</sub> Hold time, $\overline{\text{W}}$ low (test mode only)	10		10		10		ns
t <sub>CHR</sub> Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ high (CBR refresh only)	15		15		20		ns
t <sub>CRP</sub> Delay time, $\overline{\text{CAS}}$ high to $\overline{\text{RAS}}$ low	0		0		0		ns
t <sub>CSH</sub> Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ high	60		70		80		ns
t <sub>CSR</sub> Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{RAS}}$ low (CBR refresh only)	10		10		10		ns

- NOTES: 7. All cycle times assume  $t_T = 5$  ns.  
8. To assure  $t_{PC}$  min,  $t_{ASC}$  should be  $\geq 5$  ns.  
9. In a read-write cycle,  $t_{RWD}$  and  $t_{RWL}$  must be observed.  
10. In a read-write cycle,  $t_{CWD}$  and  $t_{CWL}$  must be observed.  
11. Referenced to the later of CAS or W in write operations  
12. The minimum value is measured when  $t_{RCD}$  is set to  $t_{RCD}$  min as a reference.  
13. Either  $t_{RRH}$  or  $t_{RCH}$  must be satisfied for a read cycle.

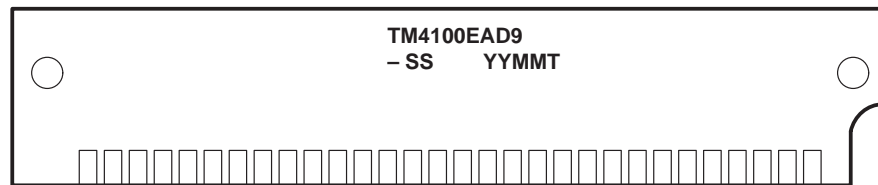


**timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)**

		'4100EAD9-60		'4100EAD9-70		'4100EAD9-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>RAD</sub>	Delay time, $\overline{\text{RAS}}$ low to column address (see Note 14)	15	30	15	35	15	40	ns
t <sub>RAL</sub>	Delay time, column address to $\overline{\text{RAS}}$ high	30		35		40		ns
t <sub>CAL</sub>	Delay time, column address to $\overline{\text{CAS}}$ high	30		35		40		ns
t <sub>RCD</sub>	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ low (see Note 14)	20	45	20	52	20	60	ns
t <sub>RPC</sub>	Delay time, $\overline{\text{RAS}}$ high to $\overline{\text{CAS}}$ low	0		0		0		ns
t <sub>RS</sub>	Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{RAS}}$ high	15		18		20		ns
t <sub>TAA</sub>	Access time from address (test mode)	35		40		45		ns
t <sub>TCPA</sub>	Access time from column precharge (test mode)	40		45		50		ns
t <sub>TRAC</sub>	Access time from $\overline{\text{RAS}}$ (test mode)	65		75		85		ns
t <sub>REF</sub>	Refresh time interval		16		16		16	ms
t <sub>T</sub>	Transition time	2	50	2	50	2	50	ns

NOTE 14: The maximum value is specified only to assure access time.

**device symbolization**



YY = Year Code  
MM = Month Code  
T = Assembly Site Code  
-SS = Speed

NOTE: The location of symbolization may vary.





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