National Semiconductor

ADVANCE INFORMATION
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LMX2360/LMX2362 PLLatinum™ Fractional-N RF/Integer-N IF Dual Low Power Frequency Synthesizer

LMX2360 2.5 GHz/550 MHz
LMX2362 1.2 GHz/550 MHz

General Description

The LMX2360/2362 family of monolithic, integrated fractional-N/Integer-N frequency synthesizers, is designed to be used in a local oscillator subsystem for a RF transceiver. It is fabricated using National's ABiC V silicon BiCMOS 0.5µ process. The LMX2360/2362 family contains quadruple modulus RF and dual modulus IF prescalers, along with modulo 1 through 16 fractional compensation circuitry in the RF divider. A combination of 16/17/20/21 prescale ratios is used for the 2.5 GHz LMX2360 and 8/9/12/13 prescale ratios for the 1.2 GHz LMX2362. The IF circuitry for both the LMX2360 and LMX2362 contains an 8/9 prescaler that is programmable. Using a fractional-N phase locked loop technique, the LMX2360/62 can generate very stable, low noise control signals for UHF and VHF voltage controlled oscillators (VCOs). The RF PLL charge pump has 0.6 mA or 4.8 mA selectable current levels while the IF PLL charge pump has 100 µA or 800 µA selectable current levels. Two uncommitted CMOS outputs can be used to provide external control signals, or configured to FastLock™ mode. An 8-bit DAC can also be multiplexed to one of the CMOS output pins. Serial data is transferred into the LMX2360/62 via a 3-wire interface (Data, LE, Clock). Supply voltage can range from 2.7V to 5.5V. The LMX2360/2362 family draws very minimal current; typically LMX2360 (2.5 GHz) - 8.0 mA, LMX2362 (1.2 GHz) - 6.5 mA at 3.0V. The LMX2360/2362 is available in a 24-pin TSSOP surface mount plastic package.

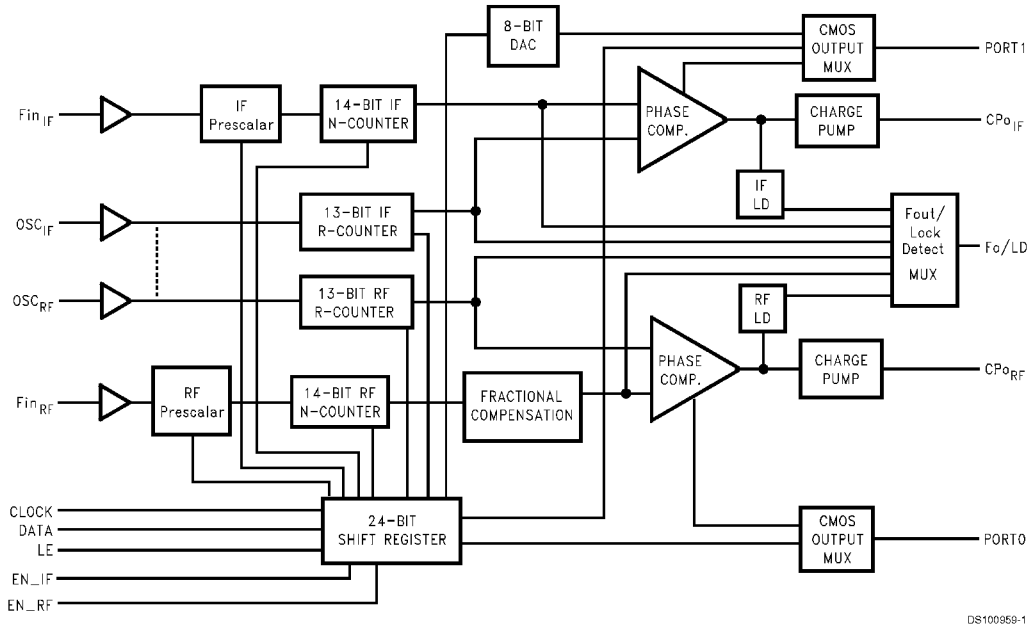
Features

- 2.7V to 5.5V operation
- Low current consumption
  LMX2360: I_{CC} = 8.0 mA typ. at 3V
  LMX2362: I_{CC} = 6.5 mA typ. at 3V
- Programmable or logical power down mode:
  I_{CC} = 10 µA max. at 3V
- Modulo 1 through 16 fractional RF N divider:
  Supports ratios of 1, 2, 3, ... ,15,16
- Programmable charge pump current levels
  RF: 0.6 mA or 4.8 mA, IF: 100 µA or 800 µA
- Digital filtered lock detect
- 8-bit voltage DAC output

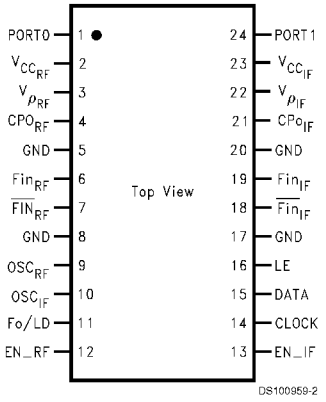
Applications

- Portable wireless communications (PCS/PCN, cordless)
- Dual mode cellular telephone systems
- Zero blind slot TDMA systems
- Spread spectrum communication systems (CDMA)
- Cable TV Tuners (CATV)

Functional Block Diagram



Pin Configuration



Pin Description

Pin No.	Pin Name	I/O	Description
1	PORT0	O	Programmable CMOS output. Output logic level controlled by programming the bit 23 of RF_N register.
2	$V_{CC_{RF}}$	—	RF PLL power supply voltage input. May range from 2.7V to 5.5V. Bypass capacitors should be placed as close possible to this pin and be connected directly to the ground plane.
3	$V_{P_{RF}}$	—	Power supply for RF charge pump.
4	$CP_{O_{RF}}$	O	RF charge pump output. Connected to a loop filter for driving the input of an external VCO.
5	GND	—	Ground for RF PLL digital circuitry.
6	$F_{IN_{RF}}$	I	RF prescaler input. Small signal input from the VCO. A bypass capacitor is required for AC coupling purpose.
7	$\overline{F_{IN_{RF}}}$	I	RF prescaler complimentary input. A bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane.
8	GND	—	Ground for RF PLL analog circuitry.
9	OSC_{RF}	I	RF PLL reference input which has a $V_{CC}/2$ input threshold and can be driven from an external CMOS or TTL logic gate.
10	OSC_{IF}	I	IF PLL reference input which can be configured to drive both the IF and RF R counter inputs or only the IF R counter depending on the state of the OSC programming bit. OSC_{IF} has a $V_{CC}/2$ input threshold and can be driven from an external CMOS or TTL logic gate.
11	F_O/LD	O	Multiplexed output of the RF/IF programmable or reference dividers and RF/IF lock detect. CMOS output.
12	EN_RF	I	EN_RF asynchronously powers down the RF PLL when LOW. (RF N- and R- counters, prescaler, and tristates charge pump output). Bringing EN_RF high powers up the RF PLL depending on the state of RF_CTL_WORD.
13	EN_IF	I	EN_IF asynchronously powers down the IF PLL when LOW. (IF N- and R- counters, prescaler, and tristates charge pump output). Bringing EN_IF high powers up the IF PLL depending on the state of IF_CTL_WORD.
14	CLOCK	I	High impedance CMOS Clock input. Data for the various counters is clocked in on the rising edge, into the 24-bit shift register.
15	DATA	I	Binary serial data input. Data entered MSB first. The last three bits are the control bits. High impedance CMOS input.
16	LE	I	Latch Enable CMOS input. When LE goes HIGH, data stored in the shift registers is loaded into one of the 6 internal latches.
17	GND	—	Ground for IF analog circuitry.
18	$\overline{F_{IN_{IF}}}$	I	IF prescaler complimentary input. A bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane.
19	$F_{IN_{IF}}$	I	IF prescaler input. Small signal input from the VCO.
20	GND	—	Ground for IF digital circuitry.
21	$CP_{O_{IF}}$	O	IF charge pump output. Connected to a loop filter for driving the input of an external VCO.
22	$V_{P_{IF}}$	—	Power supply for IF charge pump.
23	$V_{CC_{RF}}$	—	IF power supply voltage input. May range from 2.7V to 5.5V. Bypass capacitors should be placed as close possible to this pin and be connected directly to the ground plane.
24	PORT1	O	Programmable CMOS output. Output logic level controlled by programming the bit 23 of IF_CNTL register. Can be configured as 8-bit DAC output.

Absolute Maximum Ratings (Notes 1, 2)

Power Supply Voltage	
$V_{CC_{RF}}$	−0.3V to 6.5V
$V_{CC_{IF}}$	−0.3V to 6.5V
$V_{P_{RF}}$	−0.3V to 6.5V
$V_{P_{IF}}$	−0.3V to 6.5V
Voltage on any pin with	
GND = 0V (V_I)	−0.3V to V_{CC} +0.3V
Storage Temperature Range (T_S)	−65°C to +150°C
Lead Temperature (solder 4 seconds) (T_L)	+260°C
ESD - human body model (Note 2)	2 kV

Recommended Operating Ratings

Power Supply Voltage	
$V_{CC_{RF}}$	2.7V to 5.5V
$V_{CC_{IF}}$	$V_{CC_{RF}}$ to $V_{CC_{RF}}$
$V_{P_{RF}}$	V_{CC} to 5.5V
$V_{P_{IF}}$	V_{CC} to 5.5V
Operating Temperature (T_A)	−40°C to +85°C

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: This device is a high performance RF integrated circuit and is ESD sensitive. Handling and assembly of this device should only be done at ESD free worstations.

Electrical Characteristics ($V_{CC_{RF}} = V_{CC_{IF}} = V_{P_{RF}} = V_{P_{IF}} = 3.3V$; $-40°C < T_A < 85°C$ except as specified).

General				Value			Unit
Symbol	Parameter		Conditions	Min	Typ	Max	
I_{CC}	Power Supply Current	LMX2360	RF = On, IF = On, DAC = On		8.0	11	mA
		LMX2362	RF = On, IF = On, DAC = On		6.5	8.5	mA
		LMX2360/62	IF Only		1.5	2.0	mA
		LMX2360/62	DAC Only		0.65	1.0	mA
I_{CP}	$V_{P_{RF}}$ Power Supply Current		fref = 6.9 MHz, I_{CPO} = 4.8 mA		1.5	2.0	mA
$I_{CC\text{-}PWDN}$	Power Down Current		µWire inputs = 2.4V, EN_IF, EN_RF = LOW			50	µA
			µWire inputs, EN_IF, EN_RF = LOW			10	µA
f_{IN} RF	RF Operating Temperature	LMX2360		1.2		2.5	GHz
		LMX2362		0.5		1.2	GHz
f_{IN} IF	IF Operating Temperature			45		550	MHz
Zf_{IN} RF	RF Input Impedance		RF on, f_{IN} = 1890 MHz		40–j80		Ω
			RF off, f_{IN} = 1890 MHz		39–j77		Ω
Zf_{IN} IF	IF Input Impedance		f_{IN} = 120 MHz		190–j240		Ω
OSC_{RF}, OSC_{IF}	Reference Oscillator Input Operating Frequency			2		50	MHz
Z_{IN} OSC	OSC Input Impedance		OSC on, freq = 10 MHz		11–j6		kΩ
			OSC off, freq = 10 MHz		7.5–j16		kΩ
$f_{\phi\ RF}$	Phase Detector Frequency		RF Phase Detector			20	MHz
$f_{\phi\ IF}$	Phase Detector Frequency		IF Phase Detector			10	MHz
Pf_{IN} RF	RF Input Sensitivity		2.7 ≤ V_{CC} ≤ 3.6V	−15		+0	dBm
			3.6 ≤ V_{CC} ≤ 5.5V	−10		+0	dBm
Pf_{IN} IF	IF Input Sensitivity		2.7 ≤ V_{CC} ≤ 5.5V	−10		+0	dBm
V_{OSC}	Oscillator Input Sensitivity		OSC_{RF}, OSC_{IF}	0.5		V_{CC}	V_{PP}

Charge Pump			Value			Unit
Symbol	Parameter	Conditions	Min	Typ	Max	
$ICP_{O\text{-source RF}}$	RF Charge Pump Output Current	$VCP_O = V_P/2$, **RF_ICP$_O$** = 0		0.6		mA
$ICP_{O\text{-sink RF}}$		$VCP_O = V_P/2$, **RF_ICP$_O$** = 0		−0.6		mA
$ICP_{O\text{-source RF}}$		$VCP_O = V_P/2$, **RF_ICP$_O$** = 1		4.8		mA
$ICP_{O\text{-sink RF}}$		$VCP_O = V_P/2$, **RF_ICP$_O$** = 1		−4.8		mA

Electrical Characteristics ($V_{CC_{RF}} = V_{CC_{IF}} = V_{P_{RF}} = V_{P_{IF}} = 3.3V$; $-40^{\circ}C < T_A < 85^{\circ}C$ except as specified). (Continued)

Charge Pump			Value			Unit
Symbol	Parameter	Conditions	Min	Typ	Max	
$ICP_{O\text{-source IF}}$	IF Charge Pump Output Current	$VCP_O = V_P/2$, **IF_ICP$_O$** = 0		100		µA
$ICP_{O\text{-sink IF}}$		$VCP_O = V_P/2$, **IF_ICP$_O$** = 0		−100		µA
$ICP_{O\text{-source IF}}$		$VCP_O = V_P/2$, **IF_ICP$_O$** = 1		800		µA
$ICP_{O\text{-sink IF}}$		$VCP_O = V_P/2$, **IF_ICP$_O$** = 1		−800		µA
$ICP_{O\text{-TRI}}$	Charge Pump TRI-STATE® Current	$0.5 \le VCP_O \le V_P - 0.5$, $-40^{\circ}C < T_A < 85^{\circ}C$		500		pA
$ICP_{O\text{-sink}}$ vs. $ICP_{O\text{-source}}$	CP Sink vs. Source Mismatch	$VCP_O = V_P/2$, $T_A = 25^{\circ}C$		3		%
ICP_O vs. VCP_O	CP Current vs. Voltage	$0.5 \le VCP_O \le V_P - 0.5$, $T_A = 25^{\circ}C$		8		%
ICP_O vs. T_A	CP Current vs. Temperature	$VCP_O = V_P/2$, $-40^{\circ}C < T_A < 85^{\circ}C$		8		%

8-Bit Digital to Analog Converter			Value			Unit
Symbol	Parameter	Conditions	Min	Typ	Max	
V_{DAC} (255)	Output Voltage, Full Scale		2.8	3.0	3.2	V
V_{DAC} (0)	Output Voltage, Zero Scale		0.0	0.1	0.2	V
LIN_{DAC}	Linearity Error		−1		+1	LSB
ΔN_{DAC}	Step Difference Between Consecutive Codes		0.5	1.0	1.5	LSB
$PSRR_{DAC}$	Power Supply Rejection Ratio	GND+200 mV < V_{DAC} < V_{CC}− 200 mV in 50 Hz to 10 kHz range	40			dB
$I\text{-}DAC_{OUT}$	Output Drive Current		100			µA
$\tau_{DAC,\ STEP}$	Full Scale Step Response Time	C_{LOAD} = 10 pF (Note 4)			2	µs
$\tau_{DAC,\ EN}$	DAC Enable Time	C_{LOAD} = 10 pF (Note 4)			10	µs
$VREG_{DAC}$	Output Voltage Regulation	$-40^{\circ}C < T_A < 85^{\circ}C$			1	mV/ °C

Digital Interface (DATA, CLOCK, LE, EN_RF, EN_IF, POR0, PORT1)			Value			Unit
Symbol	Parameter	Conditions	Min	Typ	Max	
V_{IH}	High-Level Input Voltage	V_{CC} = 2.7V to 5.5V	2.4			V
V_{IL}	Low-Level Input Voltage	V_{CC} = 2.7V to 5.5V			0.2 V_{CC}	V
I_{IH}	High-Level Input Current	$V_{IH} = V_{CC}$ = 5.5V	−1.0		1.0	µA
I_{IL}	Low-Level Input Current	V_{IL} = 0, V_{CC} = 5.5V	−1.0		1.0	µA
I_{IH}	OSC_{RF}, OSC_{IF} Input Current	$V_{IH} = V_{CC}$ = 5.5V (Note 3)			100	µA
I_{IL}	OSC_{RF}, OSC_{IF} Input Current	V_{IL} = 0, V_{CC} = 5.5V (Note 3)	−100			µA
V_{OH}	High-Level Output Voltage	I_{OH} = −500 µA	V_{CC}−0.4			V
$V_{)L}$	Low-Level Output Voltage	I_{OL} = 500 µA			0.4	V

MICROWIRE Timing			Value			Unit
Symbol	Parameter	Conditions	Min	Typ	Max	
t_{CS}	Data to Clock Set Up Time	See Data Input Timing	50			ns
t_{CH}	Data to Clock Hold Time	See Data Input Timing	20			ns
t_{CWH}	Clock Pulse Width High	See Data Input Timing	50			ns
t_{CWL}	Clock Pulse Width Low	See Data Input Timing	50			ns
t_{ES}	Clock to Load Enable Set Up Time	See Data Input Timing	50			ns
t_{EW}	Load Enable Pulse Width	See Data Input Timing	50			ns

Note 3: OSC_{RF}, OSC_{IF} Input pins only.

Note 4: Measured from 50% of the rising edge of Load Enable to within 1/2 LSB of the final decode state.

1.0 Functional Description

The basic phase-lock-loop (PLL) configuration consists of a high-stability crystal reference oscillator, a frequency synthesizer such as the National Semiconductor LMX2360/2362, a voltage controlled oscillator (VCO), and a passive loop filter. The frequency synthesizer includes a phase detector, a current mode charge pump, as well as programmable reference [R] and feedback [N] frequency dividers. The VCO frequency is established by dividing the crystal reference signal down via the R-counter to obtain a comparison reference frequency. This reference signal (f_R) is then presented to the input of a phase/frequency detector and compared with the feedback signal (f_N), which is obtained by dividing the VCO frequency down by way of the N-counter, and fractional circuitry if present. The phase/frequency detector's current source output pumps charge into the loop filter, which then converts into the VCO's control voltage. The function of phase/frequency comparator is to adjust the voltage presented to the VCO until the feedback signal frequency and phase match that of the reference signal. When this "Phase-Locked" condition exists, the VCO frequency will be N + F times that of the comparison frequency, where N is the integer divide ratio, and F is the fractional component if applied. The fractional synthesis allows the phase detector frequency to be increased while maintaining the same frequency step size for channel selection. The divider ratio N is thereby reduced giving a lower phase noise referred to the phase detector input, and the comparison frequency is increased allowing faster switching time.

1.1 REFERENCE OSCILLATOR INPUTS

The reference oscillator frequency for the RF and IF PLLs are provided from the external references through the OSC_{RF} and OSC_{IF} pins. OSC inputs can operate up to 50 MHz with input sensitivity of 0.5 V_{PP}. The OSC pins can be configured as separated inputs to IF/RF PLL block: the OSC_{IF} pin drives the IF R-counter while the OSC_{RF} drives the RF R-counter. The **REF_OSC_SEL** bit selects whether the RF and IF R-counters are driven by oscillator input pins OSC_{RF} and OSC_{IF} separately or by sharing a common OSC_{IF} input signal. Both inputs have a $V_{CC}/2$ input threshold that can be driven from an external CMOS or TTL logic gate. Typically, the OSC pins are connected to the output of a crystal oscillator.

1.2 REFERENCE DIVIDERS (R-COUNTERS)

The RF and IF R-counters are clocked through the oscillator block either separately or in common. The maximum frequency is 50 MHz. Both R-counters are CMOS design and 13-bit in length with programmable divider ratio from 1 to 8,191.

1.3 PRESCALERS

The complimentary F_{IN} and $\overline{F_{IN}}$ inputs drive a differential-pair amplifier which feeds to the RF/IF prescaler. The LMX2360 has a quadruple modulus with selectable modulo 16/17/20/21 and the LMX2362 with selectable modulo 8/9/12/13 for RF section. The IF prescaler for both devices is dual modulus having 8/9 modulus ratio. The complementary F_{IN} and $\overline{F_{IN}}$ inputs can be driven differentially, or the negative input can be AC coupled to ground through an external capacitor for single ended configuration. Both RF/IF prescalers' outputs drive the subsequent CMOS flip-flop chain comprising the programmable N feedback counters.

1.4 FEEDBACK DIVIDERS (N-COUNTERS)

The RF and IF N-counters are clocked by the output of RF and IF prescalers respectively. The RF N-counter is composed of two parts: an integer divider and a fractional component. The integer portion is a 14-bit divisor, fully programmable from 80 to 16,383 for LMX2360, and 40 to 8192 for LMX2362. The LMX2360 is capable of operating from 1.2 GHz to 2.5 GHz with a 16/17/20/21 prescaler while the LMX2362 from 0.5 GHz to 1.2 GHz with a 8/9/12/13 prescaler. The fractional portion of the RF counter comprises of a 4-bit numerator register (**FRAC_N**) and a 4-bit denominator register (**FRAC_D**). The fraction can be programmed by writing into this register pair. The IF N-counter is a 14-bit integer divisor, fully programmable from 56 to 16,383 over the frequency range from 45 MHz to 550 MHz. The IF N-counter does not include fractional compensation.

1.5 FRACTIONAL COMPENSATION

The fractional compensation circuitry of the LMX2360/2362 RF divider allows the user to adjust the VCO tuning resolution in 1/2 through 1/16th increments of the phase detector comparison frequency. A 4-bit numerator register (**FRAC_N**) is programmed with the desired fractional numerator, while another 4-bit denominator register (**FRAC_D**) selects the fractional modulo base. The integer averaging is accomplished by using a 4-bit accumulator. A variable phase delay stage compensates for the accumulated integer phase error, minimizes the charge pump duty cycle and reduces the spurious levels. This technique eliminates the need for compensation current injection into the loop filter. Overflow signal generated by the accumulator is equivalent to 1 full VCO cycle, and results in a pulse swallow. The fractional calibration register (**FRAC_C**) are used to adjust the input center frequency of the compensation circuitry.

1.6 PHASE/FREQUENCY DETECTORS

The RF and IF phase/frequency detectors are driven from their respective N- and R-counter outputs. The maximum frequency at the phase detector inputs is 20 MHz unless limited by the minimum continuous divide ratio of the multi-modulus prescaler. The phase detector output controls the charge pump. The polarity of the pump-up or pump-down control is programmed using **RF_PD_POL** or **IF_PD_POL**, depending on whether RF or IF VCO characteristics is positive or negative. The phase detector also receives a feedback signal from the charge pump in order to eliminate dead zone.

1.7 CHARGE PUMPS

The phase detector's current source output pumps charge into an external loop filter, which then converts into the VCO's control voltage. The charge pump steers the charge pump output CPo to V_{CC} (pump-up) or Ground (pump-down). When locked, CPo is primarily in a TRI-STATE mode with small corrections. The RF charge pump output current magnitude can be selected as 0.6 mA or 4.8 mA by programming **RF_ICPo** bit. The IF charge pump can be set to either 100 µA or 800 µA levels by programming **IF_ICPo** bit.

1.8 MICROWIRE SERIAL INTERFACE

The programmable register set is accessed through the Microwire serial interface. The interface is comprised of three signal pins: clock, data and latch enable (LE). Serial data is clocked into the 24-bit shift register upon the rising edge of

1.0 Functional Description (Continued)

clock. The MSB bit of data shifts first. The last three bits decode the internal register address. On the rising edge of LE, data stored in the shift register is loaded into one of the 6 latches according to the address bits. The synthesizer can be programmed even in power down state. A complete programming description is followed in the coming sections.

1.9 MULTIFUNCTION OUTPUTS

The LMX2360/LMX2362 output pins (PORT0, PORT1 and Fo/LD) can be configured as the DAC output, Fast-Lock output or CMOS programmed output, analog/digital lock detects as well as showing the internal block status such as the counter outputs.

1.9.1 Lock Detect Ouputs

A digital filtered lock detect status is generated from the phase detector after passing through an internal digital filter and it is available on the Fo/LD output pin, if selected. The lock detect output goes high when the error between the phase detector inputs is less than 15 ns for 5 consecutive comparison cycles. It goes low when the error between the phase detector outputs is more than 30 ns for one comparison cycle. An analog lock detect signal can also be selected. When a PLL is in power down mode, the respective lock detect output is always high.

1.9.2 CMOS Outputs

The CMOS output pins, PORT0 and PORT1, can be configured as CMOS programmed outputs and the logic level is controlled by programming bit 23 of RF_N register and bit 23 of RF_CNTL register respectively. When the DAC is enabled, the DAC output is present on PORT1 pin. When configured as Fast-Lock mode, the current can be increased 8x while maintaining loop stability by synchronously switching a parallel loop filter resistor to ground, resulting in a ~3x change in loop bandwidth.

1.9.3 Digital to Analog Output

The LMX2360/2362 has an internal 8-bit DAC built-in for tuning external components. The DAC is monotonic, with a voltage output capable of sourcing 100 µA. When the DAC is enabled, it overrides the PORT1 pin function, and it drives the output to the level corresponding to the setting in the DAC register.

1.9.4 FastlLock Outputs

When configured as Fastlock mode, the current can be increased 8x while maintaining loop stability by synchronously switching a parallel loop filter resistor to ground, resulting in a ~3x change in loop bandwidth. The zero gain crossover point of the open loop gain, or the loop bandwidth is effectively shifted up in frequency by a factor of $\sqrt{8} = 2.83$ during Fastlock mode. For $\omega' = 2.83\ \omega$, the phase margin during Fastlock will also remain constant. The charge pump current is programmed via MICROWIRE™ interface. When the charge pump circuit receives an input to deliver 4 times the normal current per unit phase error, an open drain NMOS on chip device (PORT0 or PORT1) switches in a second resistor element to ground. The user calculates the loop filter component values for the normal steady state considerations. The device configuration ensures that as long as a second resistor equal to 1/2 the primary resistor value is wired in appropriately, the loop will lock faster without any additional stability considerations to account for.

1.10 POWER CONTROL

Each PLL is individually power controlled by device enable (EN) pins or power-down (**PWDN**) bits. The EN pins override the **PWDN** bits. The EN_RF pin controls the RF PLL and the EN_IF pin controls the IF PLL. When both pins are active HIGH, the **RF_PWDN** and **IF_PWDN** bits determine the state of power control.

When the EN_IF or EN_RF pins are taken inactive LOW, the respective loop is asynchronously powered down irrespective of the state of the **PWDN** bits. Activation of any PLL power-down condition results in the disabling of the respective N-counter and de-biasing of its respective F_{IN} input (to a high impedance state). The R-counter functionality also becomes disabled under this condition.

The reference oscillator input block is powered down when both EN_RF and EN_IF pins, or **RF_PWDN** and **IF_PWDN** bits are asserted. The OSC_{IF} and OSC_{RF} pins revert to a high impedance state when this condition exists. Power down forces the respective charge pump and phase comparator logic to a TRI-STATE condition. During the power down condition, both N- and R-counters are held at reset. Upon powering up, the N-counter resumes counting in "close" alignment with the R-counter. The maximum error is at most one prescaler cycle. The MICROWIRE interface remains active and it is capable of loading and latching in data during all of the power down modes.

2.0 Programming Description

2.1 MICROWIRE INTERFACE

The LMX2360/2362 register set can be accessed through the MICROWIRE interface. A 24-bit shift register is used as a temporary register to indirectly program the on-chip registers. The shift register consists of a 21-bit DATA[20:0] field and a 3-bit ADDRESS[2:0] field as shown below. The address field is used to decode the internal register address. Data is shifted into the shift register in the direction from MSB to LSB, when the CLOCK signal goes high. On the rising edge of Latch Enable (LE) signal, data stored in the shift register is loaded into the addressed latch.

MSB		LSB
DATA[20:0]		ADDRESS[2:0]
23	3	2 0

2.1.1 Registers' Address Map

When Latch Enable (LE) is transitioned high, data is transferred from the 24-bit shift register into the appropriate latch depending on the state of the ADDRESS[2:0] bits. These address bits point to the internal register to be written.

ADDRESS[2:0] FIELD			REGISTER ADDRESSED	DATA STREAM BIT LENGTH
0	0	0	IF_R Register	16
0	0	1	IF_N Register	24
0	1	0	IF_CNTL Register	24
1	0	0	RF_R Register	16
1	0	1	RF_N Register	24
1	1	0	RF_CNTL Register	24

2.1.2 Registers' Truth Table

	Most Significant Bit								SHIFT REGISTER BIT LOCATION												Least Significant Bit		
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data Field																					ADDRESS FIELD		
IF_R	DON'T CARE								IF_R_CNTR [12:0]													0	0	0
	X	X	X	X	X	X	X	X	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0			
IF_N	IF_PWDN_WORD			IF_N_CNTR [13:0]														RESERVED				0	0	1
	RE-SER-VED	REF_OSC_SEL	IF_PWDN	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0	0	0	0	0			
IF_CNTL	DAC_REGISTER [7:0]								IF_CP_WORD				FRAC_C		RESERVED							0	1	0
	D7	D6	D5	D4	D3	D2	D1	D0	IF_PWDN_MODE	IF_ICPO	IF_PD_POL	IF_SYNC_PWDN	FC1	FC0	0	0	0	0	0	0	0			
RF_R	DON'T CARE								RF_R_CNTR [12:0]													1	0	0
	X	X	X	X	X	X	X	X	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0			
RF_N	RF_PWDN_WORD			RF_N_CNTR [13:0]														FRAC_N [3:0]				1	0	1
	OUT_0	DAC_EN	RF_PWDN	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0	FN3	FN2	FN1	FN0			
RF_CNTL	CMOSout_WORD				FoLD [3:0]				RF_CP_WORD				FRAC_D [3:0]				RESERVED					1	1	0
	OUT_1	RE-SER-VED	FAST LOCK_1	FAST LOCK_0	F3	F2	F1	F0	RF_PWDN_MODE	RF_ICPO	RF_PD_POL	RF_SYNC_PWDN	FD3	FD2	FD1	FD0	0	0	0	0	0			

Note: X denotes a Don't Care condition and RESERVED field/bit should be filled all "0".

2.0 Programming Description

(Continued)

(LE) signal goes high. The divide ratio is put into the IF_R_CNTR[12:0] field. The divider ratio must be ≥ 1.

2.2 PROGRAMMABLE REFERENCE [R] DIVIDERS

2.2.1 IF_R Register

If the ADDRESS[2:0] field are set to 0 0 0, data is transferred from the 24-bit shift register into the IF_R register which sets the IF PLL's 13-bit R-counter divide ratio when Latch Enable

	MSB																					LSB
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IF_R	DON'T CARE								IF_R_CNTR [12:0]													0	0	0
	X	X	X	X	X	X	X	X	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0			

Note: X denotes a Don't Care condition.

2.2.2 RF_R Register

If the ADDRESS[2:0] field are set to 1 0 0, data is transferred from the 24-bit shift register into the RF_R register which sets the RF PLL's 13-bit R-counter divide ratio when Latch Enable (LE) signal goes high. The divide ratio is put into the RF_R_CNTR[12:0] field. The divider ratio must be ≥ 1.

	MSB																					LSB
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RF_R	DON'T CARE								RF_R_CNTR [12:0]													1	0	0
	X	X	X	X	X	X	X	X	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0			

Note: X denotes a Don't Care condition.

2.2.3 Reference Divide Ratio (R-counter)

	IF_R_CNTR [12:0] or RF_R_CNTR [12:0]												
Divide Ratio	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
1	0	0	0	0	0	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	0	0	0	0	0	1	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•
8,191	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: R-counter divide ratio must be from 1 to 8,191.

2.3 PROGRAMMABLE FEEDBACK [N] DIVIDERS

2.3.1 IF_N Register

If the ADDRESS[2:0] field are set to 0 0 1, data is transferred from the 24-bit shift register into the IF_N register which sets the IF PLL' s 14-bit N-counter and power-down features. The IF_N_CNTR[13:0] divide ratio must be ≥ 56 for a continuous divide range.

	MSB																					LSB
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IF_N	IF_PWDN_WORD			IF_N_CNTR [13:0]														RESERVED				0	0	1
	RE-SER-VED	REF_ OSC_ SEL	IF_ PWDN	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0	0	0	0	0			

Note: X denotes a Don't Care condition and RESERVED field is recommended to be filled all "0".

2.0 Programming Description (Continued)

2.3.1.1 IF Feedback Divide Ratio (IF N-counter)

	IF_N_CNTR [13:0]													
Divide Ratio	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0
56	0	0	0	0	0	0	0	0	1	1	1	0	0	0
57	0	0	0	0	0	0	0	0	1	1	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16,383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: IF N-counter divide ratio must be from 56 to 16,383.

2.3.1.2 IF PLL Power-Down Word (IF_PWDN_WORD)

These bits are used to access the IF PLL' s power-down features and to select the reference oscillator input mode.

IF_N[23]	IF_N[22]	IF_N[21]
IF_PWDN_WORD		
RESERVED	**REF_OSC_SEL**	**IF_PWDN**

IF PLL Power-Down Control (IF_PWDN)

The IF_PWDN bit is used to power down either the IF PLL' s charge pump portion, or the entire IF PLL block depending on the setting of IF_PWDN_MODE bit in IF_CNTRL register. The power-down mechanism is described fully in Section 2.6.

Reference Oscillator Select (REF_OSC_SEL)

The **REF_OSC_SEL** bit is used to select whether the RF and IF R-counters are driven by the oscillator OSC_{RF} and OSC_{IF} inputs separately, or by a common OSC_{IF} input.

When REF_OSC_REL is set to 1, the IF and RF R-counters are both driven from the OSC_{IF} input pin.

When REF_OSC_REL is set to 0, the IF and RF R-counters are driven by OSC_{IF} and OSC_{RF} inputs separately.

2.3.2 RF_N Register

If the ADDRESS[2:0] field are set to 1 0 1, data is transferred from the 24-bit shift register into the RF_N register which sets the RF PLL' s 14-bit programmable N-counter, 4-bit fractional numerator and power-down features. To obtain a continuous divide range, the RF_N_CNTR[13:0] divide ratio must be ≥ 80 for LMX2360 or must be ≥ 40 for LMX2362.

	MSB			SHIFT REGISTER BIT LOCATION																		LSB
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RF_N	RF_PWDN_WORD			RF_N_CNTR[13:0]														FRAC_N[3:0]				1	0	1
	OUT_0	DAC_EN	RF_PWDN	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0	FN3	FN2	FN1	FN0			

2.3.2.1 RF Feedback Divide Ratio (RF N-counter)

LMX2360 N-counter Divide Ratio Table

	RF_N_CNTR[13:0]													
Divide Ratio	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0
80	0	0	0	0	0	0	0	1	0	1	0	0	0	0
81	0	0	0	0	0	0	0	1	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16,383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: RF N-counter divide ratio must be from 80 to 16,383.

LMX2362 N-counter Divide Ratio Table

	RF_N_CNTR[13:0]													
Divide Ratio	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0
40	0	0	0	0	0	0	0	1	0	1	0	0	0	0
41	0	0	0	0	0	0	0	1	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
8,191	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: RF N-counter divide ratio must be from 40 to 8,191.

2.0 Programming Description (Continued)

2.3.2.2 Fractional Accumulator Modulus Numerator (FRAC_N)

	RF_N[6]	RF_N[5]	RF_N[4]	RF_N[3]
	FRAC_N[3:0]			
Modulus Numerator	FN3	FN2	FN1	FN0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
•	•	•	•	•
14	1	1	1	0
15	1	1	1	1

Note: Modulus numerator must be less than modulus denominator, i.e. FRAC_N < FRAC_D.

2.3.2.3 RF PLL Frequency Multiplication Equation

fvco = [N + F] x [fosc/R]

where F = FRAC_N/FRAC_D

fvco :output frequency of external voltage controlled oscillator (VCO)

fosc :output frequency of the external reference frequency oscillator

N :preset divide ratio of binary 14-bit programmable feedback counter

(LMX2360: 80 to 16,383 and LMX2362: 40 to 8191)

F :fractional ratio (contents of nominator FRAC_N divided by denominator FRAC_D)

R :preset divide ratio of binary 13-bit programmable reference counter (1 to 8,191)

2.3.2.4 RF PLL Power-down Word (RF_PWDN_WORD)

These bits are used to access RF PLL' s power-down features, the programmed PORT0 output and Digital-to-Analog Converter (DAC).

RF_N[23]	RF_N[22]	RF_N[21]
RF_PWDN_WORD		
OUT_0	DAC_EN	RF_PWDN

RF PLL Power-Down Control (RF_PWDN)

The RF_PWDN bit is used to power-down either the RF PLL' s charge pump portion or the entire RF PLL block depending on the setting of RF_PWDN_MODE bit in RF_CNTRL register. The power-down mechanism is described fully in Section 2.6.

Digital-to-Analog Converter Control (DAC_EN)

The DAC_EN bit is used to enable the Digital-to-Analog converter and multiplex its output signal to PORT1 pin. When it is brought HIGH, the DAC block is turned on and PORT1 pin is switched to DAC output that gives a voltage level corresponding to the setting in the DAC register. When it is set to LOW, the PORT1 pin reverts to the logic level set by the OUT_1 bit in RF_CNTL register and the DAC block is powered down.

PORT 0 Programmed output (OUT_0)

The OUT_0 bit is used to control the logic level of PORT0 pin, when it is configured as a programmable output pin. Section 2.5.2 details how to configure the PORT0 and PORT1 pins for different functions.

2.4 IF_CNTL REGISTER

If the ADDRESS[2:0] field are set to 0 1 0, data is transferred from the 24-bit shift register into the IF_CNTL register which sets the state of the IF charge pump and the 8-bit Digital-to-Analog (DAC) converter.

	MSB								SHIFT REGISTER BIT LOCATION														LSB
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IF_CNTL	DAC_REGISTER [7:0]								IF_CP_WORD				FRAC_C		RESERVED							0	1	0
	D7	D6	D5	D4	D3	D2	D1	D0	IF_PWDN_MODE	IF_ICP$_O$	IF_PD_POL	IF_SYNC_PWDN	FC1	FC0	0	0	0	0	0	0	0			

Note: RESERVED field is recommended to be filled all "0".

2.4.1 IF Charge Pump Control Word (IF_CP_WORD)

IF_CNTL[15]	IF_CNTL[14]	IF_CNTL[13]	IF_CNTL[12]
IF_CP_WORD			
IF_PWDN_MODE	IF_ICP$_O$	IF_PD_POL	IF_SYNC_PWDN

IF Charge Pump TRI-STATE/Power-down Select (IF_PWDN_MODE)

The IF_PWDN_MODE bit is used to determine the functionality of IF_PWDN bit in IF_N register to power-down either the entire IF PLL block, or the charge pump portion. When it is set to HIGH, IF charge pump power-down mode is selected in which the CP_{ORF} pin is put to a high impedance state. When it is set to LOW, the normal IF PLL block power-down is selected. The power-down mechanism is fully described in Section 2.6.

2.0 Programming Description

(Continued)

IF Charge Pump Current Gain Select (IF_ICP$_O$)

The IF_ICP$_O$ bit is used to select the IF charge pump current magnitude either 1x mode (typical 100 µA) or 8x mode (typical 800 µA).

IF Phase Detector Polarity Select (IF_PD_POL)

The IF_PD_POL bit is set to HIGH when IF VCO characteristics is positive, i.e. its frequency increases with increasing control voltage, and set to LOW otherwise.

IF PLL Synchronization Power-Down Select (IF_SYNC_PWDN)

The IF_SYNC_PWDN bit is used to set whether the power-down sequence is synchronized with the completion of charge pump pulse event. The power-down mechanism is fully described in Section 2.6.

	Bit	FUNCTION	0	1
IF_PWDN_MODE	IF_CNTL[15]	IF Charge Pump TRI-STATE Power-Down Select	Power-Down	TRI-STATE
IF_ICP$_O$	IF_CNTL[14]	IF Charge Pump Current Gain Select	1x	8x
IF_PD_POL	IF_CNTL[13]	IF Phase Detector Polarity Select	Negative	Positive
IF_SYNC_PWDN	IF_CNTL[12]	IF PLL Synchronization Power-Down Select	Async. Mode	Sync. Mode

2.4.2 Digital-to-Analog Converter Register (DAC_REGISTER)

The DAC_REGISTER[7:0] field are used to program the voltage output of Digital-to-Analog Converter (DAC).

	MSB			IF_CNTL Register				LSB
	23	22	21	20	19	18	17	16
	DAC_REGISTER [7:0]							
Programmed Value	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	1
•	•	•	•	•	•	•	•	•
255	1	1	1	1	1	1	1	1

Note: Typical output voltage = (DAC_REGISTER[7:0]/256) x 3.0V, provided that $V_{CC} \geq 3.3V$.

2.4.3 Fractional Accumulator Frequency Calibration (FRAC_C)

The FRAC_C[1:0] field is used to optimize the fractional circuitry for the operating frequency range of VCO. When FRAC_C is set to 0 0, the fractional center frequency is set to minimum. The recommended settings are shown as below:

		IF_CNTL[11]	IF_CNTL[10]
Input Frequency Range (in GHz)		FRAC_C [1:0]	
LMX2360	**LMX2362**	C1	C0
< 1.4	< 0.65	0	0
1.4–1.7	0.65–0.8	0	1
1.7–2.1	0.8–1.0	1	0
2.1–2.5	1.0–1.2	1	1

2.5 RF_CNTL REGISTER

If the ADDRESS[2:0] field are set to 1 1 0, data is transferred from the 24-bit shift register into the RF_CNTL register which sets the state of the RF charge pump, the configuration of PORT0 and PORT1 output pins, and the fractional denominator.

2.0 Programming Description (Continued)

	MSB								SHIFT REGISTER BIT LOCATION												LSB
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RF_CNTL	CMOSout_WORD				FoLD [3:0]				RF_CP_WORD				FRAC_D [3:0]				RESERVED					1	1	0
	OUT_1	RE-SER-VED	FAST LOCK _1	FAST LOCK _0	F3	F2	F1	F0	RF_PWDN_MODE	RF_ICPO	RF_PD_POL	RF_SYNC_PWDN	FD3	FD2	FD1	FD0	0	0	0	0	0			

Note: X denotes a Don't Care condition and RESERVED field is recommended to be filled all "0".

2.5.1 RF Charge Pump Control Word (RF_CP_WORD)

RF_CNTL[15]	RF_CNTL[14]	RF_CNTL[13]	RF_CNTL[12]
RF_CP_WORD			
RF_PWDN	**RF_ICPO**	**RF_PD_POL**	**RF_SYNC_PWDN**

RF Charge Pump TRI-STATE/Power-down Select (RF_PWDN_MODE)

The RF_PWDN_MODE bit is used to determine the functionality of RF_PWDN bit in RF_N register to power-down either the entire RF PLL block, or the charge pump portion. When it is set to HIGH, RF charge pump power-down mode is selected in which the $CP_{O_{RF}}$ pin is put to a high impedance state. When it is set to LOW, the normal RF PLL block power-down is selected.

RF Charge Pump Current Gain Select (RF_ICP_O)

The RF_ICPo bit is used to select the RF charge pump current magnitude either 1x mode (typical 600 µA) or 8x mode (typical 4.8 mA).

RF Phase Detector Polarity Select (RF_PD_POL)

The RF_PD_POL bit is set to HIGH when RF VCO characteristics is positive, i.e. its frequency increases with increasing control voltage, and set to LOW otherwise.

RF PLL Synchronization Power-Down Select (RF_SYNC_PWDN)

The RF_SYNC_PWDN bit is used to set whether the power-down sequence is synchronized with the completion of charge pump pulse event. The power-down mechanism is fully described in Section 2.6.

	Bit	FUNCTION	0	1
RF_PWDN_MODE	RF_CNTL[15]	RF Charge Pump TRI-STATE Power-Down Select	Power-Down	TRI-STATE
RF_ICP_O	RF_CNTL[14]	RF Charge Pump Current Gain Select	1x	8x
RF_PD_POL	RF_CNTL[13]	RF Phase Detector Polarity Select	Negative	Positive
RF_SYNC_PWDN	RF_CNTL[12]	RF PLL Synchronization Power-Down Select	Async. Mode	Sync. Mode

2.5.2 Programmable CMOS Output Port Configuration (CMOSout_WORD)

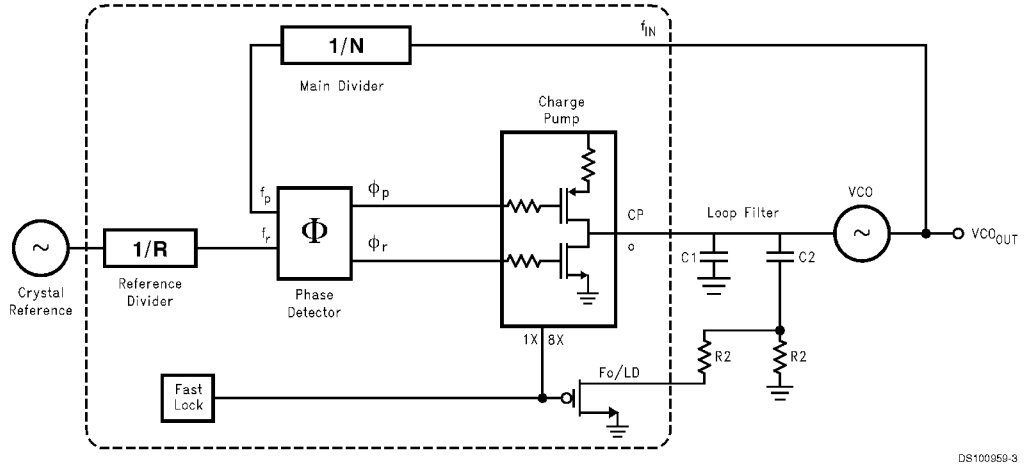
The FASTLOCK_0 and FASTLOCK_1 bits are used to configure the PORT0 and PORT1 pins to output FASTLOCK signals of IF and RF PLL respectively.

RF_CNTL[23]	RF_CNTL[22]	RF_CNTL[21]	RF_CNTL[20]
CMOSout_WORD			
OUT_1	RESERVED	FASTLOCK_1	FASTLOCK_0

When the FASTLOCK_1 is set to high, PORT1 pin is configured as the IF PLL' s FastLock signal instead of programmed output. In FastLock configuration, when the new frequency is loaded and the IF_ICP_O bit is set high, the IF charge pump circuit receives an input to deliver 8 times the normal current per unit phase error while an open drain NMOS on-chip device switches in an external resistor element to ground as shown below. Once locked on the correct frequency, the IF PLL can be returned to the standard low noise operation by setting IF_ICP_O bit to low. This transition does not affect the charge on the loop filter capacitors and is enacted synchronous with the charge pump output. This creates a nearly seamless change between FastLock and standard mode.

When the FASTLOCK_0 is set to high, PORT0 pin is configured as the RF PLL's FastLock signal instead of programmed output. The RF_ICP_O bit is used to control the RF PLL's switching between FastLock and standard mode.

2.0 Programming Description (Continued)



The DAC_EN bit (bit 22 in RF_N register) has the highest priority in using the PORT1 pin as DAC output. If the DAC_EN bit is set to high, the PORT1 output function is override to output a voltage level corresponding to the settings of the DAC register.

Bit	FUNCTION	0	1
DAC_EN	DAC output to PORT1	DAC disabled	DACout → PORT1
FASTLOCK_1	When DAC_EN = 0 PORT1 IF FastLock mode select	CMOS output	IF FastLock → PORT1
OUT_1	When DAC_EN = 0 and FASTLOCK_1 = 0 PORT1 CMOS output pin level set	LOW	HIGH
FASTLOCK_0	PORT0 RF FastLock mode select	CMOS output	RF FastLock → PORT0
OUT_0	When FASTLOCK_0 = 0 PORT0 CMOS output pin level set	LOW	HIGH

2.5.3 Fractional Accumulator Modulus Denominator (FRAC_D)

The FRAC_D[3:0] field is used to set the fractional denominator from 1/2 to 1/16 resolution. When the FRAC_D field is set to 0 0 0 0, the fractional modulus is set to 1/16 resolution.

The fractional denominator from 1 to 8 is not available as the factional number set can be completely represented by just using fractional denominator from 9 to 16 in conjunction with fractional numerator as shown in next section.

	RF_CNTL[11]	RF_CNTL[10]	RF_CNTL[9]	RF_CNTL[8]
	FRAC_D[3:0]			
Modulus Denominator	FD3	FD2	FD1	FD0
1–8	Not Allowed			
9	1	0	0	1
10–14	•	•	•	•
15	1	1	1	1
16	0	0	0	0

2.0 Programming Description (Continued)

2.5.3.1 Modulus Numerator (FRAC_N) and Denominator (FRAC_D) Programming

Fractional Numerator (FRAC_N) RF_N[6:3]	Fractional Denominator, FRAC_D RF_CNTL[11:8]															
	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111	8 1000	9 1001	10 1010	11 1011	12 1100	13 1101	14 1110	15 1111	16 0000
0=0000	Functions like an integer-N PLL as factional component is set to 0.															
1=0001		*(8/16)	*(5/15)	*(4/16)	*(3/15)	*(2/12)	*(2/14)	*(2/16)	1/9	1/10	1/11	1/12	1/13	1/14	1/15	1/16
2=0010			*(10/15)	*(8/16)	*(6/15)	*(4/12)	*(4/14)	*(4/16)	2/9	2/10	2/11	2/12	2/13	2/14	2/15	2/16
3=0011				*(12/16)	*(9/15)	*(6/12)	*(6/14)	*(6/16)	3/9	3/10	3/11	3/12	3/13	3/14	3/15	3/16
4=0100					*(12/15)	*(8/12)	*(8/14)	*(8/16)	4/9	4/10	4/11	4/12	4/13	4/14	4/15	4/16
5=0101						*(10/12)	*(10/14)	*(10/16)	5/9	5/10	5/11	5/12	5/13	5/14	5/15	5/16
6=0110							*(12/14)	*(12/16)	6/9	6/10	6/11	6/12	6/13	6/14	6/15	6/16
7=0111								*(14/16)	7/9	7/10	7/11	7/12	7/13	7/14	7/15	7/16
8=1000									8/9	8/10	8/11	8/12	8/13	8/14	8/15	8/16
9=1001										9/10	9/11	9/12	9/13	9/14	9/15	9/16
10=1010											10/11	10/12	10/13	10/14	10/15	10/16
11=1011												11/12	11/13	11/14	11/15	11/16
12=1100	IT IS NOT RECOMMENDED TO USE AS IT WILL CAUSE UNEXPECTED RESULT.												12/13	12/14	12/15	12/16
13=1101														13/14	13/15	13/16
14=1110															14/15	14/16
15=1111																15/16

Remark: The *(FRAC_N/FRAC_D) notation denotes that the fraction number can be represented by (FRAC_N/FRAC_D) as indicated.

2.5.4 Fout/Lock Detect Truth Table (FoLD)

The FoLD[3:0] field is used to select the multiplexing scheme to output the expected signal on the Fo/LD pin.

RF_CNTL[19:16] FoLD[3:0]	FoLD Output State
0 0 0 0	RF and IF Analog Lock Detect
0 0 0 1	IF Digital Lock Detect
0 0 1 0	RF Digital Lock Detect
0 0 1 1	IF and RF Digital Lock Detect
0 1 0 0	IF R counter
0 1 0 1	IF N counter
0 1 1 0	RF R counter
0 1 1 1	RF N counter
1 x x x	RESERVED

2.6 IF/RF PLL POWER-DOWN MECHANISM

By programming the IF_PWDN_MODE/RF_PWDN_MODE bit, the IF PLL/RF PLL blocks can be power-down completely or just the charge pump portion. When the PWDN_MODE bit is set to LOW, the power-down mode of the entire PLL block is selected.

The IF_PWDN_MODE/RF_PWDN_MODE bit works also in conjunction with IF_PWDN/RF_PWDN bit respectively. The PWDN bit acts as an On/Off switch for entering into, or exiting from the specified power-down state.

When the PWDN_MODE bit is set to HIGH and then the PWDN bit is brought HIGH, only the charge pump section of the respective PLL is disabled. The corresponding CP_O output is put into high impedance state.

When the PWDN_MODE bit is set to LOW, setting the PWDN bit to HIGH results in entering full power-down mode through disabling of the respective N-counter and R-counter, de-biasing of the respective F_{IN} input to a high impedance state. In addition, the respective charge pump and phase comparator logic are forced to a TRI-STATE condition and the bandgap reference block is disabled. Power-up occurs immediately when the PWDN_MODE bit is brought low.

There are two methods to power-down the PLL block, either synchronous or asynchronous. Both power-down modes are available in LMX2360/2362 in order to adapt to different types of applications. The IF_SYNC_PWDN and RF_SYNC_PWDN bits are used to select between synchronous and asynchronous power-down for IF PLL and RF PLL block respectively.

Synchronous Power-down Mode

Either of the PLL loops can be synchronously powered down by first setting the PWDN_MODE bit LOW and the SYNC_PWDN bit HIGH, and then asserting its PWDN bit HIGH. The power-down control is gated by the charge pump. Once the PWDN bit is loaded, the part will go into power-down mode upon the completion of a charge pump pulse event that allows the VCO to coast on frequency. The counters are held at reset or load state. Upon powering up, the N-counter resumes counting in "close" alignment with the R-counter. The maximum error is kept below one prescaler cycle.

Asynchronous Power-down Mode

Either of the PLL loops can be asynchronously powered down by first setting both the PWDN_MODE and SYNC_PWDN bits LOW, and then asserting its PWDN bit HIGH. The power-down control is NOT gated by the charge pump. Once the power-down bit is loaded, the respective PLL block goes into power-down mode immediately.

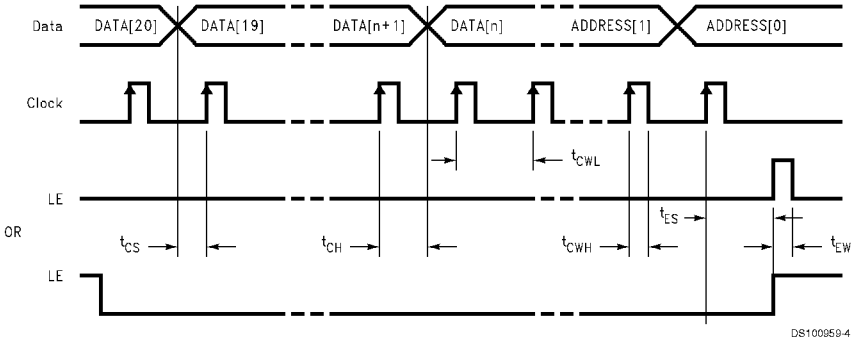
The MICROWIRE interface remains functional in power-down mode and the register content can be changed at will. Programming the internal registers is possible no matter what the operating mode is.

2.0 Programming Description

(Continued)

2.7 SERIAL DATA INPUT TIMING

TEST CONDITIONS: The Serial Data Input Timing is tested using a symmetrical waveform around $V_{CC}/2$ threshold. The test waveform has a skew rate of 0.6V/ns with amplitudes of 2.2V @ V_{CC}=2.7V, and 2.6V @ V_{CC}=5.5V.



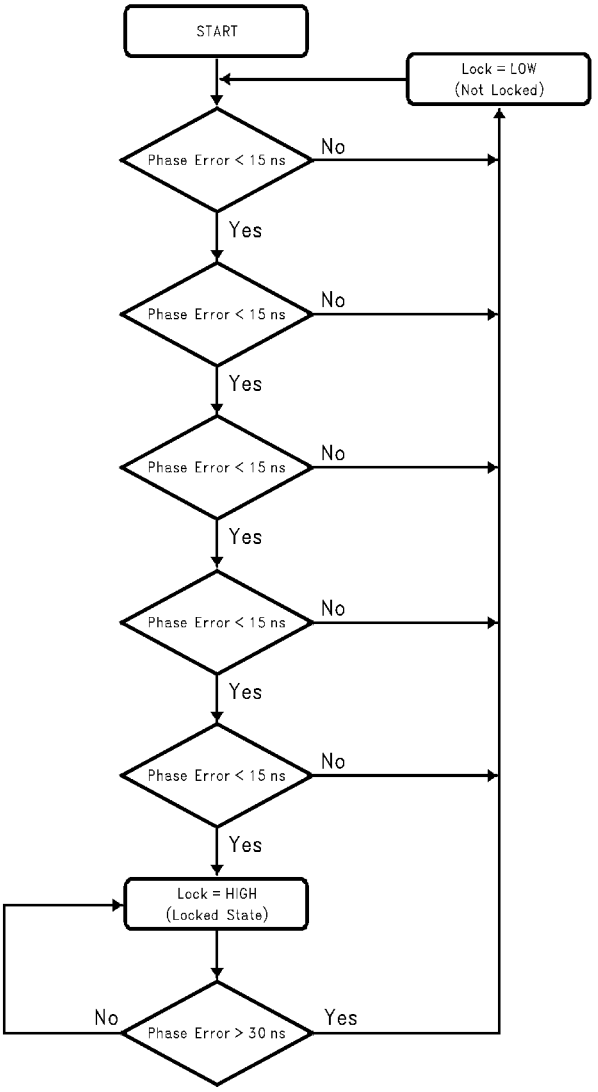
Note: Data is shifted from MSB to LSB and it is clocked into register on clock rising edge.

2.0 Programming Description

(Continued)

2.8 LOCK DETECT DIGITAL FILTER

The Lock Detect Digital Filter compares the phase difference of the inputs from the phase detector to a RC generated delay of approximately 15 ns. To enter the locked state (LOCK = High), the phase error must be less than the 15 ns RC delay for 5 consecutive reference cycles. Once in lock, the RC delay is changed to approximately 30 ns. To exit the locked state, the phase error must be greater than the 30 ns RC delay. When the PLL is in power-down mode, LOCK is forced to High state. A flow chart of the digital filter is shown as below:



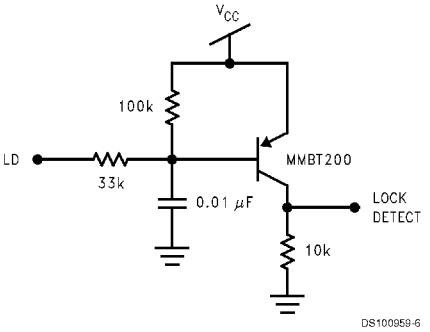
DS100959-5

2.0 Programming Description

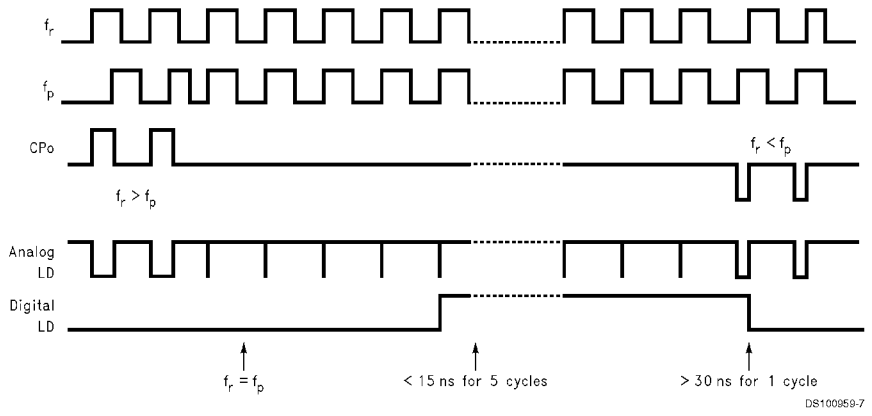
(Continued)

2.9 ANALOG LOCK DETECT FILTER

When the Fo/LD output is configured as analog lock detect output, an external lock detect circuit is needed in order to provide a steady LOW signal when the PLL is in the locked state. A typical circuit is shown below. It is noticed that Fo/LD is an "active low" open drain output.



2.10 TYPICAL LOCK DETECT TIMING

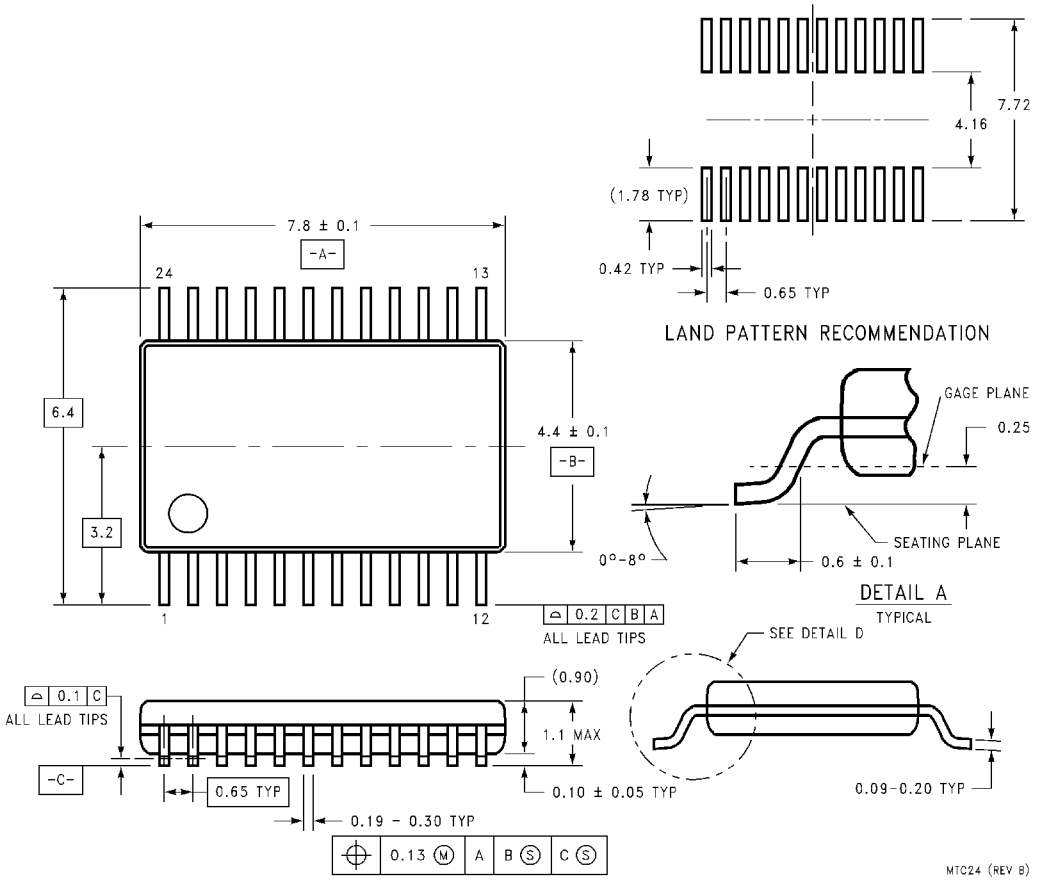


Attachment 1 - Performance Measurement for DECT Application

Test Condition: Closed loop performance values are guaranteed on NSC evaluation board at T_A = 25°C only.

			Value			
Symbol	**Parameter**	**Condition**	**Min**	**Typ**	**Max**	**Unit**
$RF\phi_n$	RF PLL Closed Loop Single Sideband Phase Noise	Offset Frequency = 144 kHz			–25	dBc/Hz
		Offset Frequency = 288 kHz			–45	dBc/Hz
		Offset Frequency = 576 kHz			–65	dBc/Hz
		Offset Frequency = 1152 kHz			–94	dBc/Hz
		Offset Frequency = 2880 kHz			–116	dBc/Hz
		Offset Frequency = 4608 kHz			–130	dBc/Hz
		Offset Frequency ≥ 6336 kHz			–135	dBc/Hz
$IF\phi_n$	IF PLL Closed Loop Single Sideband Phase Noise	Offset Frequency = 144 kHz			–25	dBc/Hz
		Offset Frequency = 288 kHz			–45	dBc/Hz
		Offset Frequency = 576 kHz			–65	dBc/Hz
		Offset Frequency = 1152 kHz			–83	dBc/Hz
		Offset Frequency = 2880 kHz			–104	dBc/Hz
		Offset Frequency = 4608 kHz			–110	dBc/Hz
		Offset Frequency ≥ 6336 kHz			–110	dBc/Hz
SPUR	RF PLL Fractional Spurious Noise	Offset Frequency ± 1728 kHz			–35	dBc
		Offset Frequency ± 3456 kHz			–57	dBc
		Offset Frequency ± 5184 kHz			–71	dBc
		Offset Frequency > 6912 kHz			–74	dBc
Tlock	RF PLL Frequency Switching Lock Time	fjump = fmin to fmax, Δf = ±15 kHz			10	µs

Physical Dimensions inches (millimeters) unless otherwise noted



LMX2360/LM362 Frequency Synthesizer IC (24 pin TSSOP package)
For Tube LMX2360TM, LMX2362TM
For Tape/Reel LMX2360TMX, LMX2362TMX
xx units per Tube, xx Tubes per Shipment Box.
xxxx units per Tape/Reel, 1 Reel per Shipment Box.

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